ON Semiconductor

FINAL PRODUCT/PROCESS CHANGE NOTIFICATION
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11-Apr-2006

SUBJECT: ON Semiconductor Final Product/Process Change Notification #15507

TITLE: Qualification of OSPI for Assembly/Test of 8/14/16 Lead SOIC Narrow Packages

EFFECTIVE DATE: 11-Jun-2006

AFFECTED CHANGE CATEGORY(S): ON Semiconductor Assembly and Test

AFFECTED PRODUCT DIVISION(S): Analog Power Management

ADDITIONAL RELIABILITY DATA: Available
Contact your local ON Semiconductor Sales Office or Matt Kas <fft7yg@onsemi.com>

SAMPLES: Contact your local ON Semiconductor Sales Office

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:
Contact your local ON Semiconductor Sales Office or Alan Garlington<rpr180@onsemi.com>

NOTIFICATION TYPE:

Final Product/Process Change Notification (FPCN)

Final change notification sent to customers. FPCNs are issued at least 60 days prior to implementation of the change.

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact your local ON Semiconductor Sales Office.

DESCRIPTION AND PURPOSE:

Final Process Change Notice to notify customers of the capacity expansion of the ON Semiconductor assembly/test location at Carmona, Philippines (OSPI) for 8/14/16 lead narrow SOIC packages. The devices listed on this FPCN have historically been assembled/tested at the ASE assembly/test facility located in Chung Li, Taiwan. At the expiration of this Initial PCN and subsequent Final PCN, these devices may be processed at either location. The ON Semiconductor facility at Carmona, Philippines is fully qualified and has been producing the SOIC narrow body products for many years. The capacity expansion will involve duplication of the existing equipment set currently in production.

Please refer to Initial PCN notice number 15335 and Update Notice 15453 which are both related to this change.

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RELIABILITY DATA SUMMARY:

Standard equipment set certification procedures will be followed prior to being placed into production.

Reliability qualification is through qualification by similarity with existing production.

ELECTRICAL CHARACTERISTIC SUMMARY:

Electrical performance will not change. Device parameters will continue to meet all data sheet specifications, and reliability will continue to meet or exceed ON Semiconductor standards.

CHANGED PART IDENTIFICATION:

Assembly lot traceability codes can be used to determine the assembly factory

AFFECTED DEVICE LIST:

PARTS

MC1403D
MC1403DR2
MC26LS30D
MC26LS30DR2
MC33232D
MC33232DG
MC33232DR2
MC33232DR2G
MC33260D
MC33260DG
MC33260DR2
MC33260DR2G
MC33364D
MC33364D1
MC33364D1R2
MC33364D2
MC33364D2R2
MC33364DG
MC33364DR2
MC33364DR2G
MC33368D
MC33368DG
MC33368DR2
MC33368DR2G
MC33567D-1R2G
NCP1603D100R2
SC33262DR2
SC33262DR2G
SC78L12ABDR2
UAA2016AD
UAA2016D

Select Report Type
Select Qualification Type

Date: October 23, 2001 **PCN: 11634**

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1) Introduction:

This reliability study was used to qualify the ON Semiconductor Carmona, Philippines assembly site (OSPI) for Pure tin(Sn) metal finish to be applied to it's existing SOIC packages using SOIC 16, and 8 leads lead package as qualification vehicle.

2) Device Descriptions:

Qual Lot ID	1804	**Wafer Fab Site**			
Device	MC78L05ACD	**Assembly Site**	OSPI CARMONA		
Line Source	TEMC78L05D	**Final Test Site**	OSPI CARMONA		
Parent Tech	Linear Voltage Regulator	**Reliability Lab**	OSPI CARMONA		
Technology	Bipolar	**Max. Current**	40mA	**Max. Voltage**	30v
Package	SOIC 8	**Die Size**	1.17 x 1.22mm	**Flag Size**	1.778 x 2.286mm
Polarity					

Qual Lot ID	1805	**Wafer Fab Site**			
Device	MC1413D	**Assembly Site**	OSPI CARMONA		
Line Source	D100P7KQ	**Final Test Site**	OSPI CARMONA		
Parent Tech	Darlington Transistor	**Reliability Lab**	OSPI CARMONA		
Technology	Bipolar	**Max. Current**	500mA	**Max. Voltage**	30v
Package	SOIC 16	**Die Size**	1.727 x 2.515mm	**Flag Size**	2.286 x 3.302mm
Polarity					

Related Qualification Report(s):

The SOIC 16, and 8 lead packages are chosen as qual vehicles for pure tin plating of SOIC packages. SOIC 14 leads, ar intermediate leadcount, is qualified by similarity

3) Qualification Results Analysis:

Environmental Stress Test Results Summary:
ZERO REJECTS achieved for the following tests:
Preconditioning: Mositure Level 1 (MSL1)
HTOL: Ta = +145°C, Tj = +150°C to 504 Hrs
HAST-PC: Ta = +130°C, RH = 85%, P = 18 PSIG to 96 Hrs
TC-PC: Ta = -65°C to +150°C to 1000 cycles
HTB: Ta = 175°C to 504 Hr
AC-PC: Ta = +121°C, RH = 100%, P = 15 PSIG to 96 Hrs

The complete test results are listed in the Test Summary section. The **bold** lettering in the Test Summary interval column indicates qualification point. The hours or cycles after the bold lettering are extended readout points.

4) Conclusion:

The reliability test results reported herein qualify the pure Sn plating for use in SOIC 8, 14, and 16 lead packages at ON Semiconductor Carmona, Philippines (OSPI). The pure Sn plating for these products meets or exceeds ON Semiconductor's requirements for Product Reliability as set forth in “Product Reliability Qualification Process,” specification 12MSB17722C Issue G.

5) Test Description & Condition:

Auto-PC	Autoclave - PC	**AUTOCLAVE + MOISTURE LEVEL PRECONDITIONING** Autoclave is an environmental test which measures device resistance to moisture penetration and the resultant effects of galvanic corrosion. Autoclave is a highly accelerated and destructive test. **Typical Test Conditions:** TA = 121°C, rh = 100%, p = 15 psig **Common Failure Modes:** Parametric shifts, high leakage and/or catastrophic **Common Failure Mechanisms:** Die corrosion or contaminants such as foreign material on or within the package materials. Poor package sealing
HAST-PC	Highly Accelerated Stress Test - PC	**HIGHLY ACCELERATED STRESS TEST + MOISTURE LEVEL PRECONDITIONING** HAST uses a pressurized environment to produce extremely severe temperature, humidity and bias conditions. HAST accelerates the same failure mechanisms as High Humidity High Temperature Bias. **Test Conditions:** TA = 131°C, rh = 85%, p = 18 psig **Common Failure Modes:** Parametric shifts, high leakage and/or catastrophic **Common Failure Mechanisms:** Die corrosion or contaminants such as foreign material on or within the package materials. Poor package sealing
HTB	High Temperature Bake	**HIGH TEMPERATURE BAKE** High temperature storage life testing is performed to accelerate failure mechanisms which are thermally activated through the application of extreme temperatures. **Test Conditions:** TA = 175°C **Common Failure Modes:** Parametric shifts in leakage and gain **Common Failure Mechanisms:** Bulk die and diffusion defects
HTOL	High Temperature Operating Life	**HIGH TEMPERATURE OPERATING LIF**E The purpose of this test is to evaluate the bulk stability of the die and to generate defects resulting from manufacturing aberrations that are manifested as time and stress-dependent failures. **Test Conditions:** TA = 145°C **Common Failure Modes:** Parametric shifts and catastrophic **Common Failure Mechanisms:** Foreign material, crack die, bulk die, metallization, wire and die bond defects
TC-PC	Temperature Cycling - PC	**TEMPERATURE CYCLING + MOISTURE LEVEL PRECONDITIONING** The purpose of this test is to evaluate the ability of the device to withstand both exposure to extreme temperatures and transitions between temperature extremes. This testing will also expose excessive thermal mismatch between materials. **Test Conditions:** TA = -65°C to 150°C, air to air **Common Failure Modes:** Parametric shifts and catastrophic **Common Failure Mechanisms:** Wire bond, cracked or lifted die and package failure
MSL-1	Moisture Level 1	**MOISTURE LEVEL PRECONDITIONING** These tests are performed to simulate the board mounting process where parts are subjected to a high temperature for a short duration. These tests detect mold compound delamination from the die and leadframe. The failure mechanisms are corrosion, fractured wirebonds and passivation cracks. 10TC + 24Hr Bake@125°C + 168Hr 85/85 + 3 IR@260°C + 1X Flux Immersion + DI Rinse

Test Summary

Test Name	Test Conditions & Bias	Lot ID	Interval	SS	Rej	Comment
Auto-PC	TA = +121°C, RH = 100%, PSIG = 15	1804A		77	0	

				77	0	
				77	0	
		1804B		77	0	
				77	0	
				77	0	
		1804C		77	0	
				77	0	
				77	0	
		1805A		77	0	
				77	0	
				77	0	
		1805B		77	0	
				77	0	
				77	0	
		1805C		77	0	
				77	0	
				77	0	
HTB	TA = 175^{0}C	1804A		77	0	
				77	0	
				77	0	
		1804B		77	0	
				77	0	
				77	0	
		1804C		77	0	
				77	0	
				77	0	

Test Name	Test Conditions & Bias	Lot ID	Interval	SS	Rej	Comment

		1805A	0 hour	77	0	
			504 hours	77	0	
			1008 hours	77	0	
		1805B	0 hour	77	0	
			504 hours	77	0	
			1008 hours	77	0	
		1805C	0 hour	77	0	
			504 hours	77	0	
			1008 hours	77	0	
HTOL	T_A=145°C, V_{CC}=40V	1804A	0 hour	77	0	
			250 hours	77	0	
			504 hours	77	0	
		1804B	0 hour	77	0	
			250 hours	77	0	
			504 hours	77	0	
		1804C	0 hour	77	0	
			250 hours	77	0	
			504 hours	77	0	
		1805A	0 hour	77	0	
			250 hours	77	0	
			504 hours	77	0	
		1805B	0 hour	77	0	
			250 hours	77	0	
			504 hours	77	0	
		1805C	0 hour	77	0	
			250 hours	77	0	
			504 hours	77	0	

Test Name	Test Conditions & Bias	Lot ID	Interval	SS	Rej	Comment

~~HAST - PC~~	~~TA = +131°C, RH = 85%, PSIG = 18, VCC=40V~~	~~1804A~~	~~0 hour~~	~~77~~	~~0~~	
			96 hours	77	0	
			192 hours	77	0	
		1804B	0 hour	77	0	
			96 hours	77	0	
			192 hours	77	0	
		1804C	0 hour	77	0	
			96 hours	77	0	
			192 hours	77	0	
		1805A	0 hour	77	0	
			96 hours	77	0	
			192 hours	77	0	
		1805B	0 hour	77	0	
			96 hours	77	0	
			192 hours	77	0	
		1805C	0 hour	77	0	
			96 hours	77	0	
			192 hours	77	0	
TC - PC	Air to Air; -65°C to +150°C	1804A	0 cycles	77	0	
			500 cycles	77	0	
			1000 cycles	77	0	
		1804B	0 cycles	77	0	
			500 cycles	77	0	
			1000 cycles	77	0	
		1804C	0 cycles	77	0	
			500 cycles	77	0	
			1000 cycles	77	0	

Test Name	Test Conditions & Bias	Lot ID	Interval	SS	Rej	Comment

		1805A	0 cycles	77	0	
			500 cycles	77	0	
			1000 cycles	77	0	
		1805B	0 cycles	77	0	
			500 cycles	77	0	
			1000 cycles	77	0	
		1805C	0 cycles	77	0	
			500 cycles	77	0	
			1000 cycles	77	0	
MSL1-260	10TC + 24Hr Bake@125°C + 168Hr 85/85 + 3x IR@260°C + 1X Flux Immersion + DI Rinse + Visual	1804A	0 hour	231	0	
			Readout	231	0	
		1804B	0 hour	231	0	
			Readout	231	0	
		1804C	0 hour	231	0	
			Readout	231	0	
		1805A	0 hour	231	0	
			Readout	231	0	
		1805B	0 hour	231	0	
			Readout	231	0	
		1805C	0 hour	231	0	
			Readout	231	0	