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**INITIAL PRODUCT/PROCESS CHANGE NOTIFICATION**  
Generic Copy

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**04-Apr-2006**

**SUBJECT: ON Semiconductor Initial Product/Process Change Notification #15504**

**TITLE: Initial PCN for Assembly Transfer of NLAS4599 in SC88 from SBN to Leshan.**

**EFFECTIVE DATE: 23-Sep-2006**

**AFFECTED CHANGE CATEGORY: ON Semiconductor Assembly**

**AFFECTED PRODUCT DIVISION: Logic**

**FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:**  
Contact Sales Office or Edwin Soto < FFTN7B @onsemi.com >

**NOTIFICATION TYPE:**

Initial Product/Process Change Notification (IPCN)

First change notification sent to customers. IPCNs are issued at least 120 days prior to implementation of the change. An IPCN is advance notification about an upcoming change and contains general information regarding the change details and devices affected. It also contains the preliminary reliability qualification plan.

The completed qualification and characterization data will be included in the Final Product/Process Change Notification (FPCN).

This IPCN notification will be followed by a Final Product/Process Change Notification (FPCN) at least 60 days prior to implementation of the change.

**DESCRIPTION AND PURPOSE:**

This is an Initial Product Change Notice to make customers aware that the ON Semiconductor facility in Leshan, China is being qualified as a manufacturing source for the NLAS4599 in SC88 (SOT363) package. Leshan is a ISO-9001/QS9000 certified factory.

NLAS4599 Die was re-designed to accommodate going from Epoxy to Eutectic die attach. No changes to performance or data sheet will occur.



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**QUALIFICATION PLAN:**

- Test Name Test Conditions End Point Requirement SS x No. Lots  
Prep Sample Preparation and initial part testing Various Room and Hot All Lab
- 2 Initial Electrical Prior to PC --- Room and Hot All Electrical
  - 3 PC MSL1 Preconditioning JEDEC PC Flow at IR = 260°C --- 250 x 3 Lots
  - 4 AC+PC Autoclave + PC Ta=121°C, RH=100%, c = 0, Room and Hot 80 x 3 Lots 14.7 PSIG
  - 5 HAST + Highly Accelerated Stress Test + PC Ta=131C, RH=85%, c = 0, Room and Hot 80 x 3 Lots  
PC ~18.8 PSIG bias per schematic
  - 6 TC+PC Temp Cycle +PC Ta=-65 to 150C c = 0, Room & Hot 85 x 3 lots
  - 7 HTOL High Temp Operating Life Ta=150C, bias per schematic c = 0, Room & Hot 80 x 3 lots
  - 8 ESD Electrostatic Discharge HBM 5 x 1 lot
  - 9 HTSL High Temp Storage TA=150C no bias c = 0, Room & Hot 80 x 3 lots
  - 10 DPA DeProcessing Analysis post 500 cycles TC 2 x 3 lots
  - 11 SAT Delamination Pre and Post MSL 5 x 3 lots
  - 12 TTC Tri Temp Characterization per 48A 25 x 3 lots
  - 13 ESD HBM, MM 1 lot
  - 14 Latchup 1 lot
  - 15 WP Wirepull 3 lots
  - 16 BS Ballshear 3 lots

**AFFECTED DEVICE LIST:**

NLAS4599DFT2  
NLAS4599DFT2G