ON Semiconductor

FINAL PRODUCT/PROCESS CHANGE NOTIFICATION
Generic Copy

13-May-2004

SUBJECT: ON Semiconductor Final Product/Process Change Notification #13466

TITLE: Final Notification for IPCN # 13259, Wafer Capacity Addition for MOS9 Technology: Group 1

EFFECTIVE DATE: 13-Jul-2004

AFFECTED CHANGE CATEGORY: Subcontractor Fab Site

AFFECTED PRODUCT DIVISION: ECL Products

ADDITIONAL RELIABILITY DATA: Available
Contact your local ON Semiconductor Sales Representative or Don Warring <RRGA60@onsemi.com>

SAMPLES: Contact your local ON Semiconductor Sales Representative

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:
Contact Sales Representative or Clarence Rebello <FFBWPN@onsemi.com>

NOTIFICATION TYPE:

Final Product/Process Change Notification (FPCN)

Final change notification sent to customers. FPCNs are issued at least 60 days prior to implementation of the change.

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact your local ON Semiconductor Sales Office.

DESCRIPTION AND PURPOSE:
This is the Final PCN for IPCN 13259 located at www.onsemi.com, for the listed devices. During the next several quarters, additional devices will be released, after completion of qualification.
A Final PCN will be announced for each group of parts as samples and electrical characterization data become available.

ON Semiconductor will be transferring 85% BiCMOS products formerly produced at the Freescale semiconductor MOS 16 facility to MOS 9 located on the Freescale Semiconductor site in Glasgow, Scotland. MOS9 is an ISO9001 certified facility and currently manufactures the 85% BiCMOS product family. The MOS 9 85% BiCMOS technology is identical to the MOS16 85% BiCMOS technology. This process will be identified as MOS 9 85% BiCMOS technologies and will provide for improved process consistency and enhanced manufacturing controls.

Device reliability will continue to meet or exceed ON Semiconductor standards.

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In the course of reviewing the electrical data, Test Methodology improvements indicate prior limits were imprecisely set. The following changes will be made in the Data Sheet:

MC100EPT23:
Change ESD HBM Upper Limit to 1500 (was 1200) V
Change ESD MM Upper Limit to 100 (was 150) V
Change IEE Upper Limit at All Temperatures to 36 (was 33) mA
Change VCMR Upper Limit at all Temperatures to VCC (was 3.3 V)
Change Tpd++ Upper Limit at 85 C to 2400 (was 2200) ps
Change Tpd-- Lower Limit at 25 C and 85 C to 1100 (was 1200) ps
Change WD_Skew++ Upper Limit at 25 C to 70 (was 60) ps
Change WD_Skew++ Upper Limit at 85 C to 125 (was 60) ps
Change WD_Skew-- Upper Limit at all Temperatures to to 80 (was 25) ps
Change Jitter_RMS Upper Limit at all Temperatures to 10 (was 1) ps

MC100LVELT23:
Change ESD HBM Upper Limit to 1500 (was 1200) V
Change ESD MM Upper Limit to 100 (was 150) V
Add ESD CDM Upper Limit of 2000 V (Was not Specified)
Change IEE Upper Limit at All Temperatures to 36 (was 33) mA
Change IIL Lower Limit at All Temperatures to -150 mA (Delete Max 0.5) mA
Change VCMR Upper Limit at all Temperatures to VCC (was 3.3 V)
Change WD_Skew++ at 25 C to 70 (was 60) ps
Change WD_Skew++ at 85 C to 125 (was 60) ps
Change WD_Skew-- at all Temperatures to to 80 (was 25) ps
Add Jitter_RMS at all Temperatures to 10 ps (was not Specified)

MC100EPT26:
Change ESD HBM Upper Limit to 1500 (was 2000) V
Change VBB Limits at All Temperatures to 1910 to 2160 (was 1775 to 1975) mV
Change IIL Lower Limit at All Temperatures to -150 mA (was 0.5) mA.
Change VCMR Upper Limit at all Temperatures to VCC (was 3.3 V)
Change Tpd++ Upper Limit at -40 C and 25 C to 2000 (was 1800) ps
Change WD_Skew++ Upper Limit at 85 C to 85 (was 60) ps
Change WD_Skew-- Upper Limit at all Temperatures to to 85 (was 25) ps
Change Tr and Tf Upper Limit at all Temperatures to 950 (was 900) ps
Add Jitter_RMS Upper Limit at all Temperatures to 30 ps up to 200 MHz
and 275 ps above 200 MHz (was not Specified)

Changes reflect typographical errors and Family Specifications, which match MOS16 devices' performance. There were no changes to the actual design or function of the parts.

RELIABILITY DATA SUMMARY:
Reliability Test Results:
Below is a summary of the interim reliability results.
A more detailed reliability report is available upon request.

Test	Conditions	Results
High Temp Op Life(HTOL)	Tj =150DegC for 1008 hours	0/231
Preconditioning (PC)	MSL1 IR at 240DegC MSL2 IR at 260DegC	0/462 0/770
HAST-PC after preconditioning	130DegC/85% RH/18.8 PSIG for 96 hrs	0/693

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Temp Cycling after preconditioning (TC-PC)	-65DegC to +150DegC; for 1000 cycles	0/693
ESD per JEDEC Standard	Human Body Model(HBM)	1500V
	Machine Model (MM)	100V
	Charge Device Model(CDM)	2000V

Qualification Vehicle Justification

Technology	Qualification Device	Reason Chosen
85% BiCMOS	Three different Motorola cellular transceivers	Large Die

Reliability Test Conclusions:
Reliability test data is consistent with passing ON Semiconductor requirements.

ELECTRICAL CHARACTERISTIC SUMMARY:
Available upon request. Electrical Performance has not changed.

CHANGED PART IDENTIFICATION:
Devices with Date Code WW29, 2004 and forward may be manufactured at Motorola MOS9 facility.

AFFECTED DEVICE LIST(WITHOUT SPECIALS):

PART
MC100EPT23D
MC100EPT23DG
MC100EPT23DR2
MC100EPT23DR2G
MC100EPT23DT
MC100EPT23DTR2
MC100EPT26D
MC100EPT26DR2
MC100EPT26DR2G
MC100EPT26DT
MC100EPT26DTR2
MC100LVELT23D
MC100LVELT23DR2
MC100LVELT23DR2G
MC100LVELT23DT
MC100LVELT23DTR2
MC100LVELT23DTRG