

FINAL PRODUCT/PROCESS CHANGE NOTIFICATION Generic Copy

21-JAN-2004

SUBJECT: ON Semiconductor Final Product/Process Change Notification #13295

TITLE: Final Notification for IPCN#11335, Wafer Capacity Addition for MOSAIC5

Technology - Group 5

EFFECTIVE DATE: 21-Mar-2004

AFFECTED CHANGE CATEGORY: ON Semiconductor Fab Site

AFFECTED PRODUCT DIVISION: ECL Products

ADDITIONAL RELIABILITY DATA: Available

Contact your local ON Semiconductor Sales Office or Keith Stapley <RXNN90@onsemi.com>

SAMPLES: Contact your local ON Semiconductor Sales Office or Mike Radhanauth <JTM4QH@onsemi.com>

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:

Contact Sales Office or Clarence Rebello <FFBWPN@onsemi.com>

NOTIFICATION TYPE:

Final Product/Process Change Notification (FPCN)

Final change notification sent to customers. FPCNs are issued at least 60 days prior to implementation of the change.

ON Semiconductor will consider this change approved unless specific conditions of acceptance are provided in writing within 30 days of receipt of this notice. To do so, contact your local ON Semiconductor Sales Office.

DESCRIPTION AND PURPOSE:

This is the Final Notification for Group 5 of devices related to IPCN 11335. ON Semiconductor is pleased to announce the Qualification and Process Certification of the COM1 wafer fabrication facility located in Phoenix, Arizona to manufacture MOSAIC5 Bipolar technology products. MOSAIC5 products were previously fabricated in the Motorola MOS6 wafer fabrication facility in Mesa, Arizona. This is the Final PCN only for the selected devices. Additional notifications will be issued separately for subsequent products when they have completed all qualification testing. Device parameters will continue to meet all Data Book specifications, except where noted below. Reliability will continue to meet or exceed ON Semiconductor standards.

In the course of reviewing the electrical data for the parts released in group 5, test methodology improvements indicate prior limits were imprecisely set. A more accurate set of Minimum and Maximum limits will be corrected on the next revision of the datasheet to reflect these changes.

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MC100EP01:

Tr, Tf Lower Limit at -40DegC changed to 50 (was 70) ps.

Tr, Tf Lower Limit at 25DegC changed to 60 (was 80) ps.

Tr, Tf Lower Limit at 85DegC changed to 70 (was 100) ps.

MC100EP139:

tJitter Upper Limit at 85DegC changed to 1.5 (was 1.0) ps.

MC10LVEP11

VOL NECL at -40 C, Upper Limit changed to -1635 (was -1685) mV.

VOL NECL at 25 C, Upper Limit changed to -1570 (was -1620) mV.

VOL NECL at 85 C, Upper Limit changed to -1510 (was -1560) mV.

RELIABILITY DATA SUMMARY:

RELIABILITY WILL CONTINUE TO MEET OR EXCEED ON SEMICONDUCTOR STANDARDS.

Test	Conditions	Results
High Temp Op Life (HTOL)	Tj =150DegC for 504 hours	0/479
High Temp Bake (HTB)	150DegC for 1008 hours	0/480
	175DegC for 504 hours	0/480
Preconditioning for MSL-1 (PC)	IR at 235DegC, TC, HAST, AC (Only for EP16 device)	0/957
Preconditioning for MSL-2 (PC)	IR at 235DegC, TC, THB, AC (Only for EP111 device)	0/720
PC-HAST	130DegC/85% RH/18.8 PSIG for 96 Hrs (Only for EP16 device)	0/240
PC-THB	85DegC/85% RH/18.8 PSIG for 1008 Hrs (Only for EP111 device)	0/240
PC-Autoclave (AC)	121DegC/100% RH/15 PSIG for 96 hours	0/480
PC-Temp Cycling (TC)	-65DegC to +150DegC; for 500 cycles	0/635
Bond Pull Strength (BPS)	Per Factory Testing with CpK>= 1.33	MEETS OR EXCEEDS CRITERIA
Bond Shear Test (BS)	Per Factory Testing with CpK>= 1.33	MEETS OR EXCEEDS CRITERIA
ESD per JEDEC Standard	Human Body Model (HBM) Machine Model (MM) Charge Device Model (CDM)	MEETS OR EXCEEDS CRITERIA
Destructive Physical Analysis (DPA)	Analysis done after PC-Temp Cycling	MEETS OR EXCEEDS CRITERIA

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Intrinsic Reliability (IR)	Compare to MOS6 results for Stress migration, Electromigration & Hot Carrier Injection	MEETS OR EXCEEDS CRITERIA
Critical Parameter Shifts Analysis (CPA)	Datalog units and examine VOH and VOL before and after test on all HTOL and Temp cycled units	MEETS OR EXCEEDS CRITERIA
Skew Analysis (SA)	Examine 5 units from each group for tskew before and after HTOL and Temp Cycle tests	MEETS OR EXCEEDS CRITERIA
Construction Analysis (CA)	Compare to MOS6 results	MEETS OR EXCEEDS CRITERIA
Parameter Verification	Electrical Characterization/distribution summary of Critical Parameters	AVAIL

Qualification Vehicle Justification

Technology	Qualification Device	Reason Chosen
MOSAIC5	MC10EP16DT	Smallest Array Base, TSOP8
	MC100LVEP111FA	Largest Array Base, 32 pin TQFP

ELECTRICAL CHARACTERISTIC SUMMARY:

Available upon request. Electrical Performance has not changed.

CHANGED PART IDENTIFICATION:

Devices with date code of WW10, 2004 and forward may be manufactured in COM1.

AFFECTED DEVICE LIST(WITHOUT SPECIALS):

PART MC100EP01D

MC100EP01DR2

MC100EP01DT

MC100EP01DTR2

MC100EP139DT

MC100EP139DTR2

MC100EP139DW

MC100EP139DWR2

MC10LVEP11D

MC10LVEP11DR2

MC10LVEP11DT

MC10LVEP11DTR2

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