

UPDATE NOTIFICATION Generic Copy

13-SEP-2002

SUBJECT: ON Semiconductor Update Notification #12556

TITLE: Update to FPCN#12449 - Assembly Transfer of Wide Body SOIC Packaged Analog Devices to ASE CHUNG LI (ASECL)

EFFECTIVE DATE: 12-Nov-2002

AFFECTED CHANGE CATEGORY:

On Semiconductor Assembly Site Subcontractor Assembly Site On Semiconductor Test Site

AFFECTED PRODUCT DIVISION: Analog Products Div

ADDITIONAL RELIABILITY DATA: Available

Contact your local ON Semiconductor Sales Office or Bob Marquis <FC88FC@onsemi.com>

SAMPLES: Contact your local ON Semiconductor Sales Office or Bill Fontes <<u>FC8HYB@onsemi.com</u>>

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:

Contact Sales Office or Bill Fontes < FC8HYB@onsemi.com>

DISCLAIMER:

Initial Product/Process Change Notification (IPCN) - First Notification distributed to customers. Distributed at least 120 days from the effective date of the change.

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DESCRIPTION AND PURPOSE:

This is an update notification to FPCN#12449 - Assembly Transfer of Wide Body SOIC Packaged Analog Devices to ASE CHUNG LI (ASECL) that went out on 3-Sep-2002, adding devices.

FPCN#12449 Verbage:

This is the final PCN for the qualification of the listed wide body SO-packaged part types for assembly at ASE in Chung Li, Taiwan (ASECL). Devices will be transferred from Carsem-S in Malaysia, and Amkor sites in both Korea and the Philippines. Devices will also be transferred from Orient Semiconductor Engineering (OSE) in the Philippines; however, OSE will remain as an alternate site to ensure no capacity limitations. The consolidation of assembly sites creates greater process control ensuring timely delivery of reliable products. An improved moisture sensitivity level of one (MSL-1) has been achieved for all devices transferred to ASECL. MSL 1 packages will no longer require drypack. The devices will be tested at ON Semiconductor's Carmona, Philippines facility for final electrical.

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ASECL and Carmona are both certified QS-9000 factories qualified for the assembly and test of automotive products. ASECL is also certified ISO-9002, and Carmona is also certified ISO-9001.

RELIABILITY DATA SUMMARY: Reliability Test Summary: Package SOIC WB 16 ld Device = CS41077DWR16 Test Conditions Interval SS THB +PC Ta=85 degC, RH=85%, bias 500 hours 0/231 Ta=121degC,P=15psig,RH=100% A/clave +PC 96 hours 0/231 Temp Cyc +PC Ta = -65 to +150 deg C500 cycles 0/231 Ta = 150 deg C.500 hours 0/231 HTB Ta = 125 deg C, bias HTOL 504 hours 0/231 MSL1 24 hr bake@125degC +168 hr 85/85 Readout 0/231 +3IR (a) 235 deg C + 1x Flux immersion + DI rinse + visual Solderability In-line data 0/45n/a Bond Pull* In-line data 0/30 n/a *after 500 Temp Cycles Ball Shear In-line data n/a 0/10 Physical Dim In-line data n/a 0/10 Ta = 125 deg C, bias ELFR 48 hours 0/2400

Reliability Test Summary: Package SOIC WB 20 ld

Device = CS2001YDWF20

Test	Conditions	Interval	SS		
THB +PC	Ta=85 degC, RH=85%, bias	500 hours	0/231		
A/clave +PC	Ta=121degC,P=15psig,RH=100%	96 hours	0/231		
Temp Cyc +PC	Ta = -65 to +150 deg C	500 cycles	0/231		
HTB	Ta = 150 deg C.	500 hours	0/231		
HTOL	Ta = 125 deg C, bias	504 hours	0/231		
MSL1	24 hr bake@125degC +168 hr 85/8	5 Readout	0/231		
	+3IR @ 235 deg C + 1x Flux imme	rsion			
	+ DI rinse + visual				
Solderability	In-line data	n/a	0/45		
Bond Pull*	In-line data	n/a	0/30		
*after 500 Temp Cycles					
Ball Shear	In-line data	n/a	0/10		
Physical Dim	In-line data	n/a	0/10		

Reliability Test Summary: Package SOIC WB 24 ld Device = CS43141XDWFR24

Test	Conditions	Interval	SS
THB +PC	Ta=85 degC, RH=85%, bias	500 hours	0/231
A/clave +PC	Ta=121degC,P=15psig,RH=100%	96 hours	0/231
Temp Cyc +PC	Ta = -65 to +150 deg C	500 cycles	0/231
HTB	Ta = 150 deg C.	500 hours	0/231
HTOL	Ta = 125 deg C, bias	504 hours	0/231
MSL1	24 hr bake@125degC +168 hr 85/8	S Readout	0/231
	+3IR @ 235 deg C + 1x Flux imme	ersion	
	+ DI rinse + visual		
Solderability	In-line data	n/a	0/45
Bond Pull*	In-line data	n/a	0/30
*after 500 Temp	Cycles		
Ball Shear	In-line data	n/a	0/10
Physical Dim	In-line data	n/a	0/10
ELFR	Ta = 125 deg C, bias	48 hours	0/2400

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Reliability Test Summary: Package SOIC WB 28 ld Device = CS68140DWFR28

Test	Conditions	Interval	SS	
THB +PC	Ta=85 degC, RH=85%, bias	500 hours	0/231	
A/clave +PC	Ta=121degC,P=15psig,RH=100%	96 hours	0/231	
Temp Cyc +PC	Ta = -65 to +150 deg C	500 cycles	0/231	
HTB	Ta = 150 deg C.	500 hours	0/231	
HTOL	Ta = 125 deg C, bias	504 hours	0/231	
MSL1	24 hr bake@125degC +168 hr 85/8	S Readout	0/231	
	+3IR @ 235 deg C + 1x Flux immersion			
	+ DI rinse + visual			
Solderability	In-line data	n/a	0/45	
Bond Pull*	In-line data	n/a	0/30	
*after 500 Temp	Cycles			
Ball Shear	In-line data	n/a	0/10	
Physical Dim	In-line data	n/a	0/10	

ELECTRICAL CHARACTERISTIC SUMMARY:

The electrical performance, specifications, and designs of the devices being transferred are unchanged. Device specific comparison data is available upon request.

CHANGED PART IDENTIFICATION:

Material with datecode marking 0244 or later may be sourced from ASECL. ASECL assembly code marking is "X"

AFFECTED DEVICE LIST (WITHOUT SPECIALS):

PART

CS2082EDW20, CS2082EDWR20, CS3524AGDW16, CS3524AGDWR16 CS4192XDWF16, CS4192XDWFR16, CS5111YDWF24, CS5111YDWFR24 CS5112YDWF24, CS5112YDWFR24, CS5165AGDW16, CS5165AGDWR16 CS5165GDW16, CS5165GDWR16, CS5165HGDW16, CS5165HGDWR16 CS5166GDW16, CS5166GDWR16, CS5166HGDW16, CS5166HGDWR16 CS7054YDWR16, CS8101YDWF20, CS8101YDWFR20, CS8129YDW16 CS8129YDWR16, CS8151YDWF16, CS8151YDWFR16, CS8183YDWF20 CS8183YDWFR20, CS8190EDWF20, CS8190EDWFR20, CS8191XDWF20 CS8191XDWFR20, CS8361YDWF16, CS8361YDWFR16, CS9001DW16