ON Semiconductor

PRODUCT BULLETIN
Generic Copy

29-MAR-2001

SUBJECT: Product Bulletin #11103

TITLE: Update for PCN#10399 Wafer Fab Technology Change for selected ECLINPS devices

EFFECTIVE DATE: 29-Mar-2001

AFFECTED CHANGE CATEGORY: Wafer Process

AFFECTED PRODUCT DIVISION: Broadband Products

ADDITIONAL RELIABILITY DATA: Available
Contact your local ON Semiconductor Sales Office.
or Keith Stapley <RXNN90@onsemi.com>

SAMPLES: Contact Below
Contact your local ON Semiconductor Sales Office.
or Eric Glatfelter <R23606@onsemi.com>

FOR ANY QUESTIONS CONCERNING THIS NOTIFICATION:
Contact Sales Office or Tim Gurnett <R13617@onsemi.com>

DISCLAIMER:
ON Semiconductor considers this change approved unless specific conditions of acceptance are
provided in writing. To do so, contact your local ON Semiconductor sales office.

DESCRIPTION AND PURPOSE:
This update to PCN 10399 is to add devices to the original PCN and to modify the implementation
dates for some of the devices. Only devices listed at the end of this PCN are affected by the change.
The original 10399 PCN expiration date of April 27, 2001 will apply only for then
MC100LVE111FN/FNR2 and MC100E111FN/FNR2 devices. This update to PCN 10399 extends the
expiration date to May 14, 2001 for the MC10E111FN/FNR2, MC10EL16D/DR2/DT/DTR2 and the
MC100EL16D/DR2/DT/DTR2 devices. MC10EL11, MC100EL11, MC100LVEL11, MC100EL14,
MC100LVEL14, and MC100LVEL16 are not part of the change at this time.

 Samples are currently available on most of the parts. Contact the (TIC) Technical Information Center
at 1-800-282-9855 regarding sample dates for each of the device types listed above.

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Original Text of PCN #10399 "Wafer Fab Technology Change for selected ECLINPS devices"
In order to better serve our customers, ON Semiconductor will increase wafer capacity by redesigning selected ECLinPS and ECLinPS-Lite devices from MOSAIC3 to MOSAIC5. The devices will continue to meet the same data sheet specifications. MOSAIC5 is a more advanced wafer fabrication process technology on which all EC LinPS Plus devices are currently produced. MOSAIC5 is a trench isolated, double epi, double poly, multi-layer metal, bipolar process similar to MOSAIC3 but has a minimum photolithography feature size of 0.7 um as compared to MOSAIC3 which has a minimum photolithography feature size of 2 um. Additionally, MOSAIC5 utilizes an industry standard inorganic interlayer dielectric layer as compared to MOSAIC3 which has an organic polyimide interlayer dielectric layer MOS6, located in Phoenix, Arizona, has been qualified to run ECLinPS Plus devices using the same arrays on the MOSAIC5 process for approximately 2 years.

The MOSAIC5 process at MOS6 has been qualified to run production wafers since 1994. The device parameters will continue to meet all data book specifications. Device reliability will continue to meet ON Semiconductor standards. These device types will be available on MOSAIC 3 during the transition period in order to provide customers an opportunity to evaluate the MOSAIC5 devices in their applications. The MOSAIC5 device types will be denoted with an additional letter, "F", as the first character of the datecode marking while MOSAIC3 devices will continue to be marked with the current marking code. Customers are invited to request samples to examine for any performance variations in their applications.

RELIABILITY DATA SUMMARY:
The Mosaic 5 Qual reports available are:

  MC100EP139DW 0143 2000
  MC10EP01D PJJA001 1999
  MC10EP05D PJJA002 1999
  MC10EP56DT 0178 2000

Reliability Test data results are consistent with passing ON Semiconductor qualification requirements. These devices are fully qualified. A copy of the full Reliability Report is available upon request.

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ELECTRICAL CHARACTERISTIC SUMMARY:
MS3 to MS5 2nd Pass Design - AC/DC Summary at Nominal (-5.2 Volts)
MC10EL16 - Differential Line Receiver
Voltage -5.2 V   UPDATED TG 2/5/01
Temp   25 C
Measurement Info
   MOSAIC 3 LOT

Characteristic	Symbol	Units	Mean	S
Power Supply Current	IEE	mA	15.3	0.2
Output Ref. Voltage	VBB	mV	-1297	8
Input LOW Current	IIL	uA	35.1	1.6
Input HIGH Current	IIH	uA	35.2	1.6
Output LOW Voltage	VOL	mV	-1725	11
Output HIGH Voltage	VOH	mV	-882	11
Prop Delay to Output (DIFF)	tPLH	Ps	231	6
Prop Delay to Output (DIFF)	tPHL	Ps	243	6
Prop Delay to Output (SE)	tPLH	Ps	255	8
Prop Delay to Output (SE)	tPHL	Ps	262	6
Rise Time Q	tR	Ps	153	4
Rise Time Qbar	tR	Ps	154	7
Fall Time Q	tF	Ps	147	5
Fall Time Qbar	tF	Ps	143	5
Minimum Input Swing	VPP	mV	100	0

   MOSAIC 5 (2nd) LOT

Mean	S	LIMITS Lo limit	Hi Limit	VARIATION Mean	Sigma
16	0.1	DNC	22	4.6%	50.0%
-1285	3	-1350	-1250	0.9%	62.5%
47.5	0.5	0.5	DNC	35.3%	68.8%
67.4	0.6	DNC	150	91.5%	62.5%
-1777	7	-1950	-1630	3.0%	36.4%
-906	2	-980	-810	2.7%	81.8%
244	3	175	325	5.6%	50.0%
242	4	175	325	0.4%	33.3%
288	5	125	375	12.9%	37.5%
259	4	125	375	1.1%	33.3%
156	5	100	350	2.0%	25.0%
132	6	100	350	14.3%	14.3%
158	5	100	350	7.5%	0.0%
135	4	100	350	5.6%	20.0%
100	0	150	DNC	0.0%	0.0%

Definitions/Comments:
S stands fir Sigma.
DNC stands for Do Not Care.
DIFF means Differential inputs.
SE means Single ended inputs.
Variance Calculation is ABS((X-Y)/X,
where x and y are the mean values from the Eval summary.

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Update Summary: The 2nd pass 10EL16 evaluation results look very good. The major AC issues did not change from 1st to 2nd pass design tweak. IEE and VOL levels are closer to the MOSAIC 3 part on the 2nd pass design. The current drawn by the device, IIL and IIH, are higher than the Mosaic 3 Process same as the 10EL16.

CHANGED PART IDENTIFICATION:

The MOSAIC5 device types will be denoted with an additional letter, "F", as the first character of the datecode marking while MOSAIC3 devices will continue to be marked with the current marking code.

AFFECTED DEVICE LIST:

PART
MC100E111FN
MC100E111FNR2
MC100E111SFN
MC100E111SFNR2
MC100EL16D
MC100EL16DR2
MC100EL16DT
MC100EL16DTR2
MC100LVE111FN
MC100LVE111FNR2
MC10E111FN
MC10E111FNR2
MC10E111SFN
MC10E111SFNR2
MC10EL16D
MC10EL16DR2
MC10EL16DT
MC10EL16DTR2