# Quad 2-Channel Multiplexer with 3-State Outputs

# MC74VHCT257A

The MC74VHCT257A is an advanced high speed CMOS quad 2−channel multiplexer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

It consists of four 2−input digital multiplexers with common select (S) and enable ($\overline{OE}$) inputs. When ($\overline{OE}$) is held High, selection of data is inhibited and all the outputs go Low.

The select decoding determines whether the A or B inputs get routed to the corresponding Y outputs.

The VHCT inputs are compatible with TTL levels. This device can be used as a level converter for interfacing 3.3 V to 5.0 V because it has full 5.0 V CMOS level output swings.

The VHCT257A input structures provide protection when voltages between 0 V and 5.5 V are applied, regardless of the supply voltage. The output structures also provide protection when $V_{CC}$ = 0 V. These input and output structures help prevent device destruction caused by supply voltage−input/output voltage mismatch, battery backup, hot insertion, etc.

The internal circuit is composed of three stages, including a buffered output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

- High Speed: $t_{PD}$ = 4.1 ns (Typ) at $V_{CC}$ = 5.0 V
- Low Power Dissipation: $I_{CC}$ = 4.0 μA (Max) at $T_A$ = 25°C
- TTL−Compatible Inputs: $V_{IL}$ = 0.8 V; $V_{IH}$ = 2.0 V
- Power Down Protection Provided on Inputs and Outputs
- Balanced Propagation Delays
- Designed for 2.0 V to 5.5 V Operating Range
- Low Noise: $V_{OLP}$ = 0.8 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance:
  Human Body Model > 2000 V;
  Machine Model > 200 V
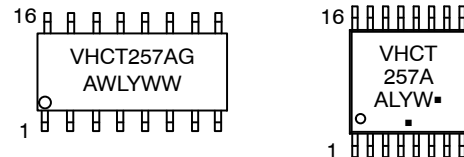- These Devices are Pb−Free and are RoHS Compliant
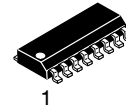


**SOIC−16**
**D SUFFIX**
**CASE 751B**
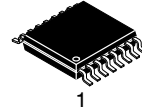
**TSSOP−16**
**DT SUFFIX**
**CASE 948F**

## MARKING DIAGRAM



| | |
|---|---|
| A | = Assembly Location |
| WL, L | = Wafer Lot |
| Y | = Year |
| WW, W | = Work Week |
| G or ▪ | = Pb−Free Package |

(Note: Microdot may be in either location)

## FUNCTION TABLE

| Inputs | | Outputs |
|---|---|---|
| $\overline{OE}$ | S | Y0 – Y3 |
| H | X | Z |
| L | L | A0 – A3 |
| L | H | B0 – B3 |

A0 – A3, B0 – B3 = the levels of the respective Data−Word Inputs.

## ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.
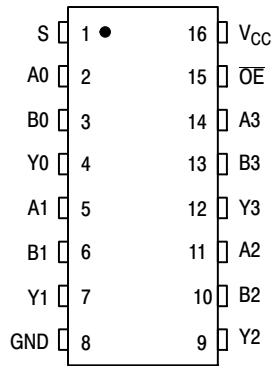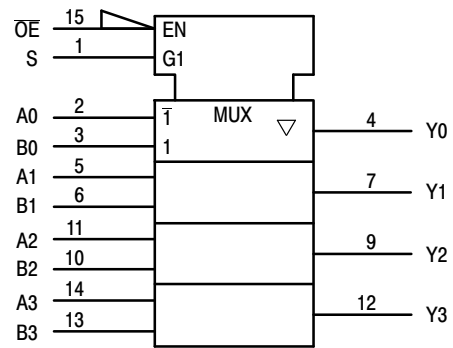
# MC74VHCT257A



**Figure 1. Pin Assignment**

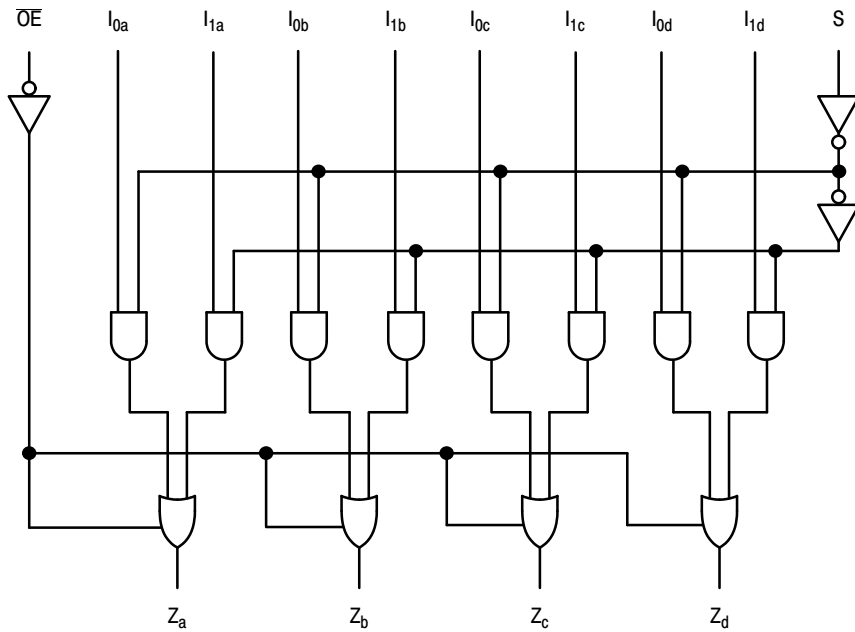| | | | |
|---|---|---|---|
| S | 1 ● | 16 | $V_{CC}$ |
| A0 | 2 | 15 | $\overline{OE}$ |
| B0 | 3 | 14 | A3 |
| Y0 | 4 | 13 | B3 |
| A1 | 5 | 12 | Y3 |
| B1 | 6 | 11 | A2 |
| Y1 | 7 | 10 | B2 |
| GND | 8 | 9 | Y2 |



**Figure 2. IEC Logic Symbol**



**Figure 3. Expanded Logic Diagram**

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND $\leq$ ($V_{in}$ or $V_{out}$) $\leq V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

**MAXIMUM RATINGS**

| Symbol | Parameter | | Value | Unit |
|---|---|---|---|---|
| $V_{CC}$ | Positive DC Supply Voltage | | −0.5 to +7.0 | V |
| $V_{IN}$ | Digital Input Voltage | | −0.5 to +7.0 | V |
| $V_{OUT}$ | DC Output Voltage | Output in 3−State<br>High or Low State | −0.5 to +7.0<br>−0.5 to $V_{CC}$ +0.5 | V |
| $I_{IK}$ | Input Diode Current | | −20 | mA |
| $I_{OK}$ | Output Diode Current | | ± 20 | mA |
| $I_{OUT}$ | DC Output Current, per Pin | | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | | ± 75 | mA |
| $P_D$ | Power Dissipation in Still Air | SOIC<br>TSSOP | 200<br>180 | mW |
| $T_{STG}$ | Storage Temperature Range | | −65 to +150 | °C |
| $V_{ESD}$ | ESD Withstand Voltage | Human Body Model (Note 1)<br>Machine Model (Note 2)<br>Charged Device Model (Note 3) | >2000<br>>200<br>>2000 | V |
| $I_{LATCHUP}$ | Latchup Performance | Above $V_{CC}$ and Below GND at 125°C (Note 4) | ± 300 | mA |
| $\theta_{JA}$ | Thermal Resistance, Junction−to−Ambient | SOIC<br>TSSOP | 143<br>164 | °C/W |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Tested to EIA/JESD22−A114−A
2. Tested to EIA/JESD22−A115−A
3. Tested to JESD22−C101−A
4. Tested to EIA/JESD78

**RECOMMENDED OPERATING CONDITIONS**

| Symbol | Characteristics | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage | | 4.5 | 5.5 | V |
| $V_{IN}$ | DC Input Voltage | | 0 | 5.5 | V |
| $V_{OUT}$ | DC Output Voltage | | 0 | 5.5 | V |
| $T_A$ | Operating Temperature Range, all Package Types | | −55 | 125 | °C |
| $t_r$, $t_f$ | Input Rise or Fall Time | $V_{CC}$ = 5.0 V ± 0.5 V | 0 | 20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES**

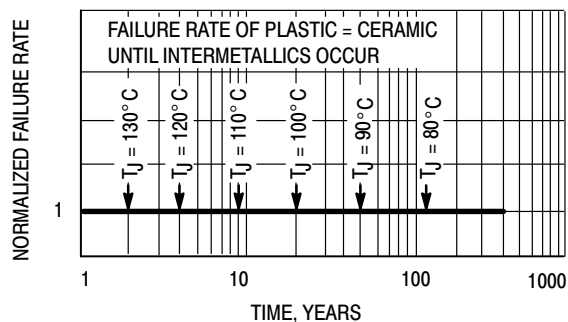| Junction Temperature °C | Time, Hours | Time, Years |
|---|---|---|
| 80 | 1,032,200 | 117.8 |
| 90 | 419,300 | 47.9 |
| 100 | 178,700 | 20.4 |
| 110 | 79,600 | 9.4 |
| 120 | 37,000 | 4.2 |
| 130 | 17,800 | 2.0 |
| 140 | 8,900 | 1.0 |



**Figure 4. Failure Rate vs. Time Junction Temperature**

# MC74VHCT257A

## DC CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Condition | $V_{CC}$ (V) | $T_A = 25°C$ Min | Typ | Max | $T_A \leq 85°C$ Min | Max | $-55°C \leq T_A \leq 125°C$ Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum High–Level Input Voltage | | 4.5 to 5.5 | 2 | | | 2 | | 2 | | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | | 4.5 to 5.5 | | | 0.8 | | 0.8 | | 0.8 | V |
| $V_{OH}$ | Maximum High–Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50\ \mu A$ | 4.5 | 3.94 | | | 3.8 | | 3.66 | | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -8\ mA$ | 4.5 | 3.94 | | | 3.8 | | 3.66 | | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50\ \mu A$ | 4.5 | | 0 | 0.1 | | 0.1 | | 0.1 | V |
| | | $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = 8\ mA$ | 4.5 | | | 0.36 | | 0.44 | | 0.52 | |
| $I_{IN}$ | Input Leakage Current | $V_{IN} = 5.5$ V or GND | 0 to 5.5 | | | ±0.1 | | ±1.0 | | ±1.0 | $\mu A$ |
| $I_{OZ}$ | Maximum 3–State Leakage Current | $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND | 5.5 | | | ±0.25 | | ±2.5 | | ±2.5 | $\mu A$ |
| $I_{CCT}$ | Maximum Quiescent Supply Current | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 1.35 | | 1.5 | | 1.65 | mA |
| $I_{CC}$ | Additional Quiescent Supply Current (per pin) | $V_{IN} = V_{CC}$ or GND | 5.5 | | | 4.0 | | 40 | | 40 | $\mu A$ |
| $I_{OPD}$ | Output Leakage Current | $V_{OUT} = 5.5$ V | 0 | | | 0.5 | | 5 | | 5 | $\mu A$ |

## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ns)

| Symbol | Parameter | Test Conditions | | $T_A = 25°C$ Min | Typ | Max | $T_A = \leq 85°C$ Min | Max | $-55°C \leq T_A \leq 125°C$ Min | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, A or B to Y | $V_{CC} = 3.3 \pm 0.3$ V | $C_L = 15$ pF $C_L = 50$ pF | | 5.8 8.3 | 9.3 12.8 | 1.0 1.0 | 11.0 14.5 | 1.0 1.0 | 11.0 14.5 | ns |
| | | $V_{CC} = 5.0 \pm 0.5$ V | $C_L = 15$ pF $C_L = 50$ pF | | 3.6 5.1 | 5.9 7.9 | 1.0 1.0 | 7.0 9.0 | 1.0 1.0 | 7.0 9.0 | |
| $t_{PLH}$, $t_{PHL}$ | Maximum Propagation Delay, S to Y | $V_{CC} = 3.3 \pm 0.3$ V | $C_L = 15$ pF $C_L = 50$ pF | | 7.0 9.5 | 11.0 14.5 | 1.0 1.0 | 13.0 16.5 | 1.0 1.0 | 13.0 16.5 | ns |
| | | $V_{CC} = 5.0 \pm 0.5$ V | $C_L = 15$ pF $C_L = 50$ pF | | 4.0 5.5 | 6.8 8.8 | 1.0 1.0 | 8.0 10.0 | 1.0 1.0 | 8.0 10.0 | |
| $t_{PZL}$, $t_{PZH}$ | Maximum Output Enable, Time, $\overline{OE}$ to Y | $V_{CC} = 3.3 \pm 0.3$ V $R_L = 1$ kΩ | $C_L = 15$ pF $C_L = 50$ pF | | 6.7 9.2 | 10.5 14.0 | 1.0 1.0 | 12.5 16.0 | 1.0 1.0 | 12.5 16.0 | ns |
| | | $V_{CC} = 5.0 \pm 0.5$ V $R_L = 1$ kΩ | $C_L = 15$ pF $C_L = 50$ pF | | 3.6 5.1 | 6.8 11.0 | 1.0 12.0 | 8.0 10.0 | 1.0 1.0 | 8.0 12.0 | |
| $t_{PLZ}$, $t_{PHZ}$ | Maximum Output Disable, Time, $\overline{OE}$ to Y | $V_{CC} = 3.3 \pm 0.3$ V $R_L = 1$ kΩ | $C_L = 50$ pF | | 10.5 | 14.0 | 1.0 | 15.0 | 1.0 | 15.0 | ns |
| | | $V_{CC} = 5.0 \pm 0.5$ V $R_L = 1$ kΩ | $C_L = 50$ pF | | 9.5 | 12.0 | 1.0 | 13.0 | 1.0 | 13.0 | |
| $C_{IN}$ | Maximum Input Capacitance | | | | 4 | 10 | | 10 | | 10 | pF |

| | | | **Typical @ 25°C, $V_{CC}$ = 5.0 V** | |
|---|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Note 5) | | 20 | pF |

5. $C_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. $C_{PD}$ is used to determine the no–load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 5.0$ V)

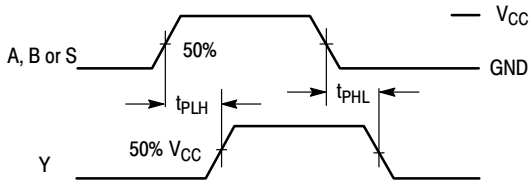| Symbol | Characteristic | $T_A = 25°C$ Typ | Max | Unit |
|---|---|---|---|---|
| $V_{OLP}$ | Quiet Output Maximum Dynamic $V_{OL}$ | 0.3 | 0.8 | V |
| $V_{OLV}$ | Quiet Output Minimum Dynamic $V_{OL}$ | − 0.3 | − 0.8 | V |
| $V_{IHD}$ | Minimum High Level Dynamic Input Voltage | | 2.0 | V |
| $V_{ILD}$ | Maximum Low Level Dynamic Input Voltage | | 0.8 | V |

# MC74VHCT257A
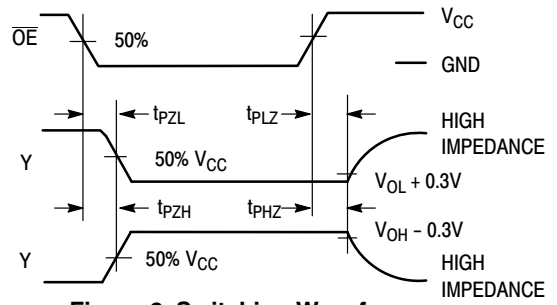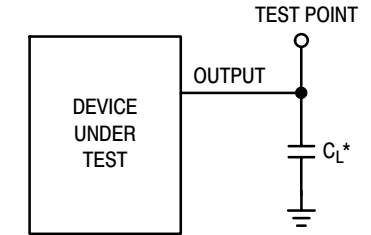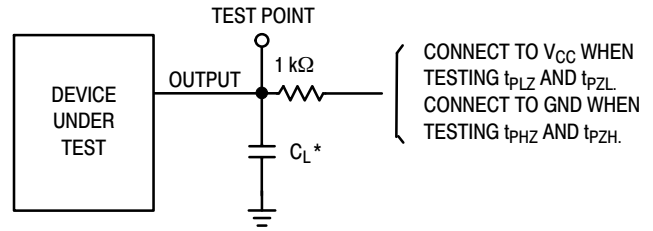


Figure 5. Switching Waveform



Figure 6. Switching Waveform



*Includes all probe and jig capacitance

Figure 7. Test Circuit



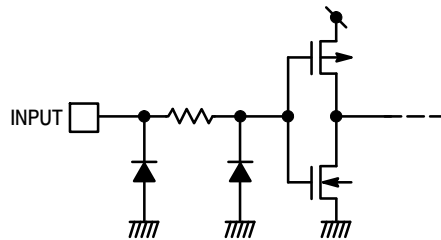*Includes all probe and jig capacitance

Figure 8. Test Circuit



Figure 9. Input Equivalent Circuit

## ORDERING INFORMATION

| Device | Package | Shipping[†] |
|---|---|---|
| MC74VHCT257ADG | SOIC−16 (Pb−Free) | 48 Units / Rail |
| MC74VHCT257ADR2G | SOIC−16 (Pb−Free) | 2500 Tape & Reel |
| MC74VHCT257ADTG | TSSOP−16 (Pb−Free) | 96 Units / Rail |
| M74VHCT257ADTR2G | TSSOP−16 (Pb−Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**SOIC−16 9.90x3.90x1.37 1.27P**
**CASE 751B**
**ISSUE M**

DATE 18 OCT 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS | | |
|-----|------|------|------|
|     | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.10 | 0.18 | 0.25 |
| A2 | 1.25 | 1.37 | 1.50 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | --- | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| Θ | 0° | --- | 7° |

| TOLERANCE OF FORM AND POSITION | |
|-----|------|
| aaa | 0.10 |
| bbb | 0.20 |
| ccc | 0.10 |
| ddd | 0.25 |
| eee | 0.10 |

TOP VIEW

SIDE VIEW

END VIEW

DETAIL "A"

DETAIL "A"
Scale 3:1

0.25 GAUGE PLANE

8X
6.40

1.270
PITCH

16X
0.58

1.120

RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

| **DOCUMENT NUMBER:** | **98ASB42566B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| **DESCRIPTION:** | **SOIC−16 9.90X3.90X1.37 1.27P** | | **PAGE 1 OF 2** |

# SOIC−16 9.90x3.90x1.37 1.27P
## CASE 751B
## ISSUE M

DATE 18 OCT 2024

## GENERIC
## MARKING DIAGRAM*

```
16 ┌────────────────┐
   │ XXXXXXXXXXXXG  │
   │ XXXXXXXXXXXXX  │
 o │    AWLYWW      │
 1 └────────────────┘
```
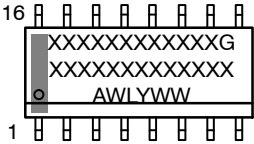
| | |
|---|---|
| XXXXX | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot "▪", may
or may not be present. Some products may
not follow the Generic Marking.

**STYLE 1:**
PIN 1. COLLECTOR
2. BASE
3. EMITTER
4. NO CONNECTION
5. EMITTER
6. BASE
7. COLLECTOR
8. COLLECTOR
9. BASE
10. EMITTER
11. NO CONNECTION
12. EMITTER
13. BASE
14. COLLECTOR
15. EMITTER
16. COLLECTOR

**STYLE 2:**
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION
4. CATHODE
5. CATHODE
6. NO CONNECTION
7. ANODE
8. CATHODE
9. CATHODE
10. ANODE
11. NO CONNECTION
12. CATHODE
13. CATHODE
14. NO CONNECTION
15. ANODE
16. CATHODE

**STYLE 3:**
PIN 1. COLLECTOR, DYE #1
2. BASE, #1
3. EMITTER, #1
4. COLLECTOR, #1
5. COLLECTOR, #2
6. BASE, #2
7. EMITTER, #2
8. COLLECTOR, #2
9. COLLECTOR, #3
10. BASE, #3
11. EMITTER, #3
12. COLLECTOR, #3
13. COLLECTOR, #4
14. BASE, #4
15. EMITTER, #4
16. COLLECTOR, #4

**STYLE 4:**
PIN 1. COLLECTOR, DYE #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. COLLECTOR, #3
6. COLLECTOR, #3
7. COLLECTOR, #4
8. COLLECTOR, #4
9. BASE, #4
10. EMITTER, #4
11. BASE, #3
12. EMITTER, #3
13. BASE, #2
14. EMITTER, #2
15. BASE, #1
16. EMITTER, #1

**STYLE 5:**
PIN 1. DRAIN, DYE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. DRAIN, #3
6. DRAIN, #3
7. DRAIN, #4
8. DRAIN, #4
9. GATE, #4
10. SOURCE, #4
11. GATE, #3
12. SOURCE, #3
13. GATE, #2
14. SOURCE, #2
15. GATE, #1
16. SOURCE, #1

**STYLE 6:**
PIN 1. CATHODE
2. CATHODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE
7. CATHODE
8. CATHODE
9. ANODE
10. ANODE
11. ANODE
12. ANODE
13. ANODE
14. ANODE
15. ANODE
16. ANODE

**STYLE 7:**
PIN 1. SOURCE N-CH
2. COMMON DRAIN (OUTPUT)
3. COMMON DRAIN (OUTPUT)
4. GATE P-CH
5. COMMON DRAIN (OUTPUT)
6. COMMON DRAIN (OUTPUT)
7. COMMON DRAIN (OUTPUT)
8. SOURCE P-CH
9. SOURCE P-CH
10. COMMON DRAIN (OUTPUT)
11. COMMON DRAIN (OUTPUT)
12. COMMON DRAIN (OUTPUT)
13. GATE N-CH
14. COMMON DRAIN (OUTPUT)
15. COMMON DRAIN (OUTPUT)
16. SOURCE N-CH

| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. | |
|---|---|---|---|
| DESCRIPTION: | SOIC−16 9.90X3.90X1.37 1.27P | | PAGE 2 OF 2 |

**onsemi**

**TSSOP−16 WB**
CASE 948F
ISSUE B

DATE 19 OCT 2006

16

1

**SCALE 2:1**

16X **K** REF

$\oplus$ | 0.10 (0.004) Ⓜ | T U Ⓢ V Ⓢ

△ | 0.15 (0.006) | T U Ⓢ

2X **L**/2

**L**

**16** ... **9**

PIN 1
IDENT.

**1** ... **8**

△ | 0.15 (0.006) | T U Ⓢ

**A**

−V−

**B**
−U−

**K**
**K1**

**J1**

**SECTION N−N**

**J**

**N**

0.25 (0.010)

**M**

**N**

**F**

**DETAIL E**

**C**

△ | 0.10 (0.004)

−T− | SEATING
PLANE

**D**

**G**

**H**

**DETAIL E**

−W−

NOTES:
1. DIMENSIONING AND TOLERANCING PER
   ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD
   FLASH. PROTRUSIONS OR GATE BURRS.
   MOLD FLASH OR GATE BURRS SHALL NOT
   EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE
   INTERLEAD FLASH OR PROTRUSION.
   INTERLEAD FLASH OR PROTRUSION SHALL
   NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR
   PROTRUSION. ALLOWABLE DAMBAR
   PROTRUSION SHALL BE 0.08 (0.003) TOTAL
   IN EXCESS OF THE K DIMENSION AT
   MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR
   REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE
   DETERMINED AT DATUM PLANE −W−.

| DIM | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

**RECOMMENDED**
**SOLDERING FOOTPRINT***

7.06

1

0.65
PITCH

16X
0.36

16X
1.26

DIMENSIONS: MILLIMETERS

**GENERIC**
**MARKING DIAGRAM***

16

XXXX
XXXX
ALYW

1
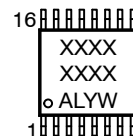
XXXX = Specific Device Code
A    = Assembly Location
L    = Wafer Lot
Y    = Year
W    = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to
device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪ ",
may or may not be present. Some products
may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering
details, please download the **onsemi** Soldering and Mounting
Techniques Reference Manual, SOLDERRM/D.

| **DOCUMENT NUMBER:** | 98ASH70247A | | |
|---|---|---|---|
| **DESCRIPTION:** | TSSOP−16 | | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

◊