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Eliminating the Tradeoff between Protection and Signal Integrity

Using PicoGuard XS ESD Protection Architectures

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TECHNICAL NOTE

Executive Summary

Two important trends are leading to fundamental changes in ESD protection strategies at the system design level: increased susceptibility of system ICs to ESD as they migrate to more advance process technologies, and increasingly stringent signal integrity requirements as data rates continue to climb.

The traditional approach to dealing with higher data rates has been to reduce the capacitance of the ESD protection device, but doing this tends to reduce the ESD protection capabilities of the device. As a result, system designers are forced to make tradeoffs between system reliability and signal integrity.

This paper is intended to eliminate the confusion around ESD protection architectures so that you can confidently take the next step toward designing more reliable systems without the tradeoffs.

Main topics include ESD protection device trends, shortcomings of traditional ESD protection architectures, and important considerations for choosing an ESD protection device for superior signal integrity. Lastly, this paper introduces an innovative, breakthrough ESD protection architecture created by ON Semiconductor that eliminates the tradeoff between signal integrity and ESD protection.

THE CHANGING ESD PROTECTION LANDSCAPE

Smaller Manufacturing Geometries − as manufacturing geometries for today's most advanced ASICs decrease to 90 nm and less, the voltage and current levels that can cause ESD related failures for these devices also decrease. The increasing adoption of high speed data interfaces adds to the complexity of maintaining a high level of signal integrity while ensuring robust ESD protection. More robust ESD protection typically means higher levels of capacitance, which negatively impacts signal integrity and forces designers to compromise on one or the other.

A Reduction in On-Chip Protection − increased susceptibility to ESD damage has been widely publicized as the Industry Council on ESD Target Specifications recently announced a move to reduce the standard level of onchip ESD protection, making external ESD protection circuits even more critical for adequate system reliability.

The Changing Application Environment – the proliferation of laptops, cell phones, MP3 players, digital cameras, and other hand-held mobile devices, used in uncontrolled environments (i.e., no wrist-grounding straps or conductive and grounded table surfaces). In these environments, people touch I/O connector pins while connecting and disconnecting cables. A portable device can also build up a charge during normal usage and discharge that energy when connected to another device, such as a computer or a TV.

Increasing Data Rates and Smaller Geometries

Consider the increase in data rates:

- HDMI® − 3.4 Gbps per Link
- DP − 2.7 Gbps per Link
- eSATA − 3 Gbps (Moving to 6 Gbps)
- USB − 480 Mbps for High Speed (10x in "Super Speed" USB 3.0)
- 1394/Firewire − 800 Mbps (Moving to 3.2 Gbps)

This trend is likely to continue. To support growing data rates, transmitters and receivers are designed in smaller geometry silicon, which is inherently more prone to ESD damage. External ESD protection is required for these high speed circuits. Generally, as ESD protection levels increase, ESD device capacitance also increases. However, adding capacitance can negatively impact signal integrity.

Increasing capacitance increases the attenuation of the signal and essentially functions as an unwanted filter. Increasing capacitance also causes impedance mismatches that can cause reflections, signal skew, and EMI problems, all of which contribute to poor signal integrity.

As data rates go up, even small increases in capacitance or minor changes in impedance can cause signal integrity problems. With traditional device architectures, there are generally only two approaches for choosing ESD protection solutions for high speed signals:

- Select a Device Optimized for Low Capacitance
- Select a Device Optimized for ESD Protection

Balancing the inverse relationship between robust ESD protection and low capacitance levels makes this choice more complex. While lower capacitance improves signal

integrity, it reduces ESD protection. Existing solutions compromise on one or the other.

With multi-gigabit data rates, even small capacitance levels or small mismatches in capacitance can cause signal integrity problems. These mismatches can be overcome, sometimes through careful attention to layout (such as trace necking to increase inductance and eliminating ground fill under traces), as well as by adding additional components such as common mode chokes. However, these approaches are suboptimal, and can add unwanted cost and complexity to a design.

Existing ESD Architecture Limitations – Which Device is Best?

There are several types of ESD protection devices available today, but the most common are divided into three categories:

- **Polymer Devices** − While polymers seem attractive for high-frequency applications due to their sub-picofarad capacitance of 0.05–0.1 pF, this low capacitance comes with not-so-attractive side effects. A polymer device does not break down until it reaches a trigger voltage that is much higher than the clamping voltage. The high trigger voltage can result in permanent damage to the system. In addition, after the charge is dissipated, the polymer is supposed to return to its high-impedance state, but this can take from several hours to a day, which makes them unattractive for consumer applications. Finally, polymers degrade over time and with multiple strikes, making them unreliable for long-term ESD protection.
- **Varistors and Suppressors** − Suppressors and varistors are also low capacitance, typically in the 0.05 to 1.0 pF range. These devices suffer from high trigger voltages, high clamping voltages, and extremely high dynamic resistance (often > 20 Ω), which results in most of the energy reaching the protected device instead of being shunted to ground. Another disadvantage of suppressors is that they degrade with use. Changes in electrical properties have been observed after a single ESD strike, including changes in capacitance. Most suppressors fail after 10 to 20 ESD strikes. Like polymers, they are unreliable for long-term ESD protection and generally unattractive for consumer applications.
- **Semiconductor Diodes** − Characterized by low clamping voltages, low resistance, fast turn-on times, and better reliability. Due to their much lower clamping voltages and dynamic resistance (~1 Ω typical), semiconductor diodes provide much better ESD protection and are required in any system where quality and ESD protection are considered important. The downside is that semiconductor diodes are typically higher capacitance than polymers and suppressors, typically in the range of 0.7 to 2.0 pF. Diode manufacturers are continuing to push towards lower capacitance solutions, but as capacitance goes down, the dynamic resistance also typically increases, reducing ESD performance.

Generally, polymers, suppressors, and varistors should never be used for ESD protection unless a semiconductor based solution is not possible. Engineers should always choose a device that offers low clamping voltages and low dynamic resistance if they want to provide adequate ESD protection.

The most difficult task in determining which ESD protection device to choose is figuring out which device will provide the greatest protection. Often, system vendors compare ESD protection devices using data sheet ESD level ratings. In reality, these ratings say nothing about how well the device will protect the system. For example, device X may say 8 kV, device Y says 15 kV, so device Y is better – or is it? ESD ratings for protection devices say only what the device itself will survive, not what the system will survive. In many cases, an 8 kV device may offer more protection than the 15 kV device, depending on other characteristics of the device.

In addition to the ESD rating level of the protection device, voltage level (clamping voltage) and how much current (residual current) will be seen by the ASIC are critical considerations. ESD protection devices function by shunting most of the current to ground and “clamping” the voltage seen at the ASIC to a lower value than the strike voltage.

Determining the clamping voltage and residual current is not an easy task. The clamping voltage quoted in most ESD protection datasheets can be misleading. Most datasheets quote clamping voltage based on a 1.0 A pulse that has a rise time of 8 ms and a duration of 20 ms. This has little to do with a real ESD pulse, which has a rise time of less than 1 ns and a duration of 60 ns. However, it can be used to compare between two parts on a relative basis. Other datasheets may quote a clamping voltage based on the IEC 61000−4−2 pulse, but will quote the voltage after 30 ns. This is well after the peak voltage that occurs at 1 ns and can be misleading.

The residual current is never quoted, because it is a product of the system layout rather than solely of the device itself. As a proxy, using the protection circuit’s dynamic resistance can help compare devices, since a device with lower resistance will shunt a higher proportion of the current. Unfortunately, this value is also rarely mentioned in protection datasheets. Luckily, most semiconductor datasheets usually contain enough information to approximate the dynamic resistance of the protection device, making it possible to compare between devices.

For the best ESD protection, always choose a device that minimizes the clamping voltage and residual current.

Compensating to Match Impedance

Typically, using any type of ESD protection circuit on high speed lines requires some sort of external compensation. To understand this, it is first important to understand impedance matching.

A critical factor in high speed layouts is to have matched impedance along the entire transmission line. The impedance is affected by many variables, including trace width, board dielectric thickness, board materials, components on the traces, etc. A simple way to understand impedance is that it is the square root of L/C, where L is the inductance and C is the capacitance at any given point on the transmission line. This means that if a capacitance is added at one point, the impedance will drop at that point. If inductance is added, the impedance will rise.

While the goal of the optimized layout is to match the impedance along the entire line, it is difficult to truly achieve "matched" impedance. However, in most designs, variations of ~15% are considered acceptable. For example, in HDMI, the goal is for the differential impedance to be centered around 100 Ω, but it can vary between 85 Ω and 115 Ω, and still be considered compliant to the standard.

Any protection device added to the line, whether it is a diode, varistor, suppressor, or polymer, will add capacitance, not only from the device itself, but also due to the pads used to connect the device to the PCB. To compensate for the added capacitance of the protection solution, system designers typically change the design by reducing capacitance elsewhere on the board, or by adding inductance. Typical techniques for doing this include:

- Adding a common mode choke or filter: This is a common solution, since adding the inductance of the choke can offset the capacitance of the ESD device. Unfortunately, adding high speed common mode chokes to a design can be quite expensive, and should be avoided if possible.
- Reducing the trace widths in the area of the protection device, increasing the inductance of the trace without adding capacitance: This is often called trace necking and can be very effective when only small amounts of compensation are required. One limitation with this approach is that on thin dielectric boards, if the capacitance of the ESD device is too high, it can be difficult to achieve matched impedance.
- Reducing the capacitance under the trace: This can be done by eliminating any ground plane from under the trace and reducing capacitance only in the area of the ESD component.

All of these solutions are sub-optimal, add complexity, and sometimes cost. These techniques require well-controlled design and manufacturing environments and sometimes more costly components, either in the form of external components such as common mode chokes, or thicker dielectric PCBs. Another major drawback to using these techniques is that many engineers do not have experience designing impedance controlled layouts. This inexperience often results in design errors that increase development cost due to multiple board spins, as well as design and production slips.

XtremeESD Protection: Superior Protection and Superior Signal Integrity

Recognizing that a radically new approach is required to meet today's ESD requirements, ON Semiconductor has introduced the XtremeESD family of ESD protection devices. The XtremeESD family consists of several architectures that fundamentally change the approach to providing ESD protection for high speed data ports. The PicoGuard XP architecture offers dramatically better ESD performance than traditional ESD protection devices, while maintaining excellent signal integrity, and will soon be followed by the PicoGuard XS architecture, which is designed to provide outstanding signal integrity for high speed data interfaces along with improved ESD protection. With these new options, designers can ensure their systems meet both their reliability and signal integrity goals without compromise.

Figure 1 illustrates how XtremeESD solutions compare to traditional devices when addressing the balance between protection and signal integrity.

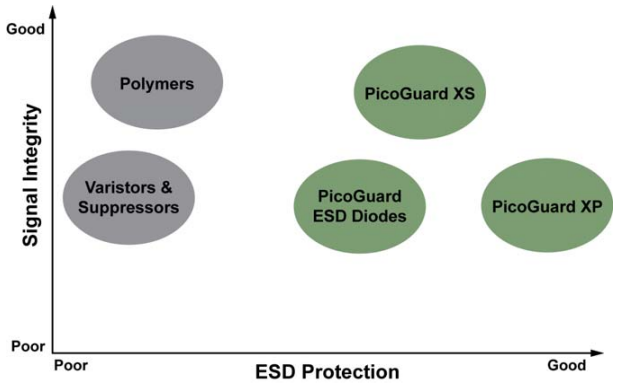

Figure 1. Signal Integrity vs ESD Protection

PicoGuard XS: Superior Protection and Outstanding Signal Integrity

In a fundamental breakthrough in how ESD devices are designed and used in a system, PicoGuard XS eliminates the engineer's tradeoff between ESD protection and signal integrity. PicoGuard XS achieves superior ESD protection while eliminating the need for external compensation for impedance matching on high speed data lines.

PicoGuard XS devices eliminate design and layout concerns, enable optimal signal integrity, improve ESD performance, and are ideal solution for high-speed, multi-gigabit per second ports such as HDMI, DisplayPort, and eSATA. PicoGuard XS devices provide ESD protection for extreme high-speed data interfaces where designers require robust ESD protection and no-compromise signal integrity performance.

PicoGuard XS improves signal integrity with on-chip matching, skew and EMI reduction, as well as improved TDR due to integrated inductance, making it the ideal solution for safeguarding high speed data ports.

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