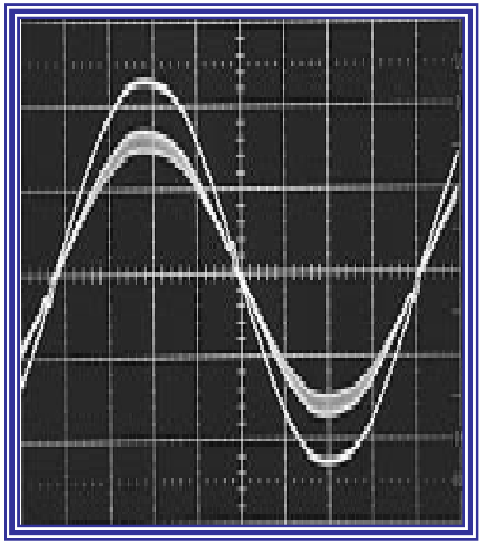
ON Semiconductor®

Advanced Power Factor Correction

Agenda

- Introduction
  - Basic solutions for power factor correction
  - New needs to address
- Interleaved PFC
  - Basic characteristics
  - A discrete solution
  - Performance
- Bridgeless PFC
  - Why should we care of the input bridge?
  - Main solutions
  - Ivo Barbi solution
  - Performance of a wide mains, 800 W application
- Conclusion



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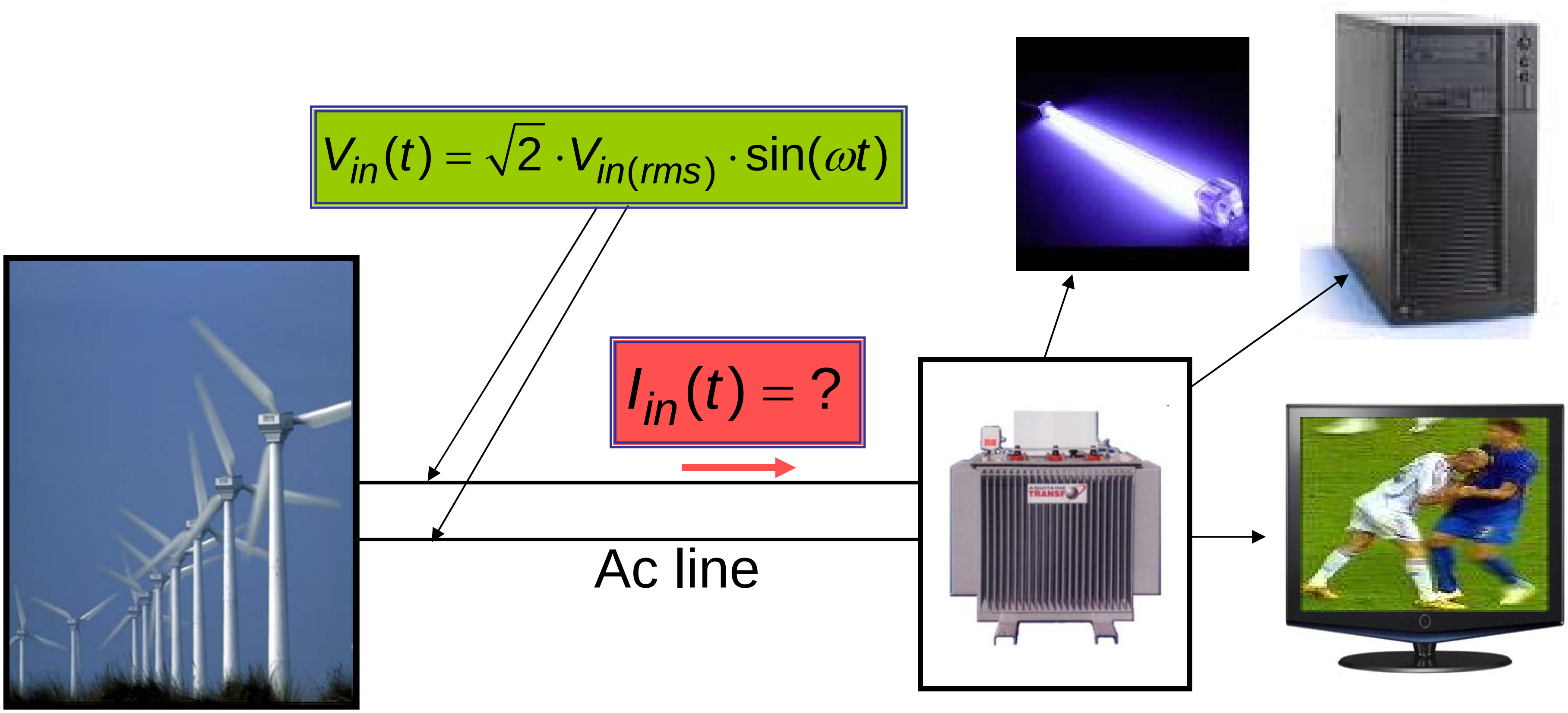
Harmonic	Class-A Amp	Class-B Amp	Class-C % of Fund	Class-D mA/Watt
2	1.08	1.62	2	
3	2.30	3.45	30*PF	3.4
4	0.43	0.65		
5	1.44	2.16	10	1.9
6	0.30	0.45		
7	0.77	1.12	7	1
8	0.23	0.35		
9	0.40	0.60	5	0.5
10	0.18	0.28		
11	0.33	0.50	3	0.35
12	0.15	0.23		
13	0.21	0.32	3	0.296
14/40 (even)	1.84/n	2.76/n		
15/39 (odd)	2.25/n	3.338/n	3	3.85/n

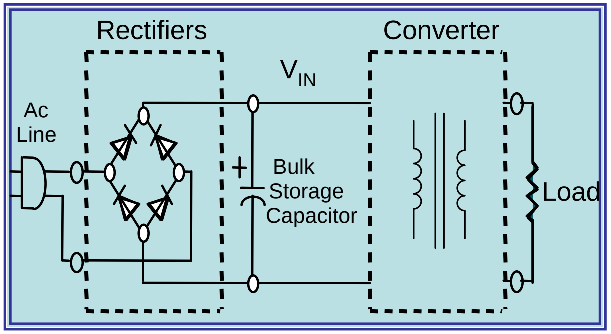
Table -1 EN/IEC61000-3-2 Harmonic current limits

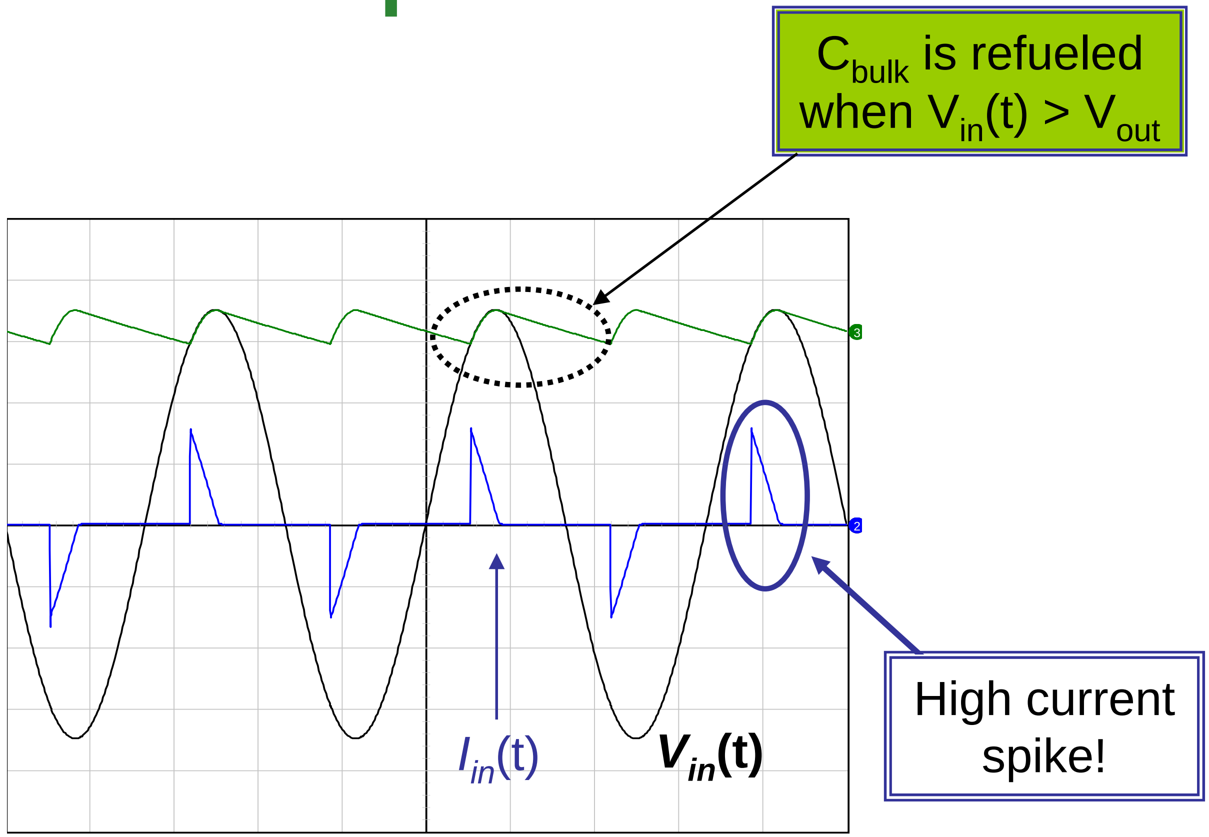
Why Implement PFC?



- The mains utility provides a sinusoidal voltage $\boldsymbol{V_{in}(t)}$.
- The shape and phase of $\boldsymbol{I_{in}(t)}$ depend on the load.

AC Line Rectification Leads to Current Spikes…





- Only the fundamental component produces real power
- Harmonic currents circulate uselessly (reactive power)
- The line rms current increases

Too High rms Currents!...

- High rms currents reduce outlet capability

n°1
- $P_{in(avg)}$ = 119 W, $V_{in(rms)}$ = 85 V
- $I_{in(rms)}$ = 2.5 A

n°2
- $P_{in(avg)}$ = 119 W, $V_{in(rms)}$ = 85 V
- $I_{in(rms)}$ = 1.4 A

PF = 0.56

PF = 1.00

Same power (W)

n°1 ← 16/2.5 = **6** monitors

n°2 ← 16/1.4 = **11** resistors

$(I_{in(rms)})_{max}$ = 16 A

$$\boxed{I_{in(rms)} = \frac{P_{in(avg)}}{V_{in(rms)} \cdot PF}}$$

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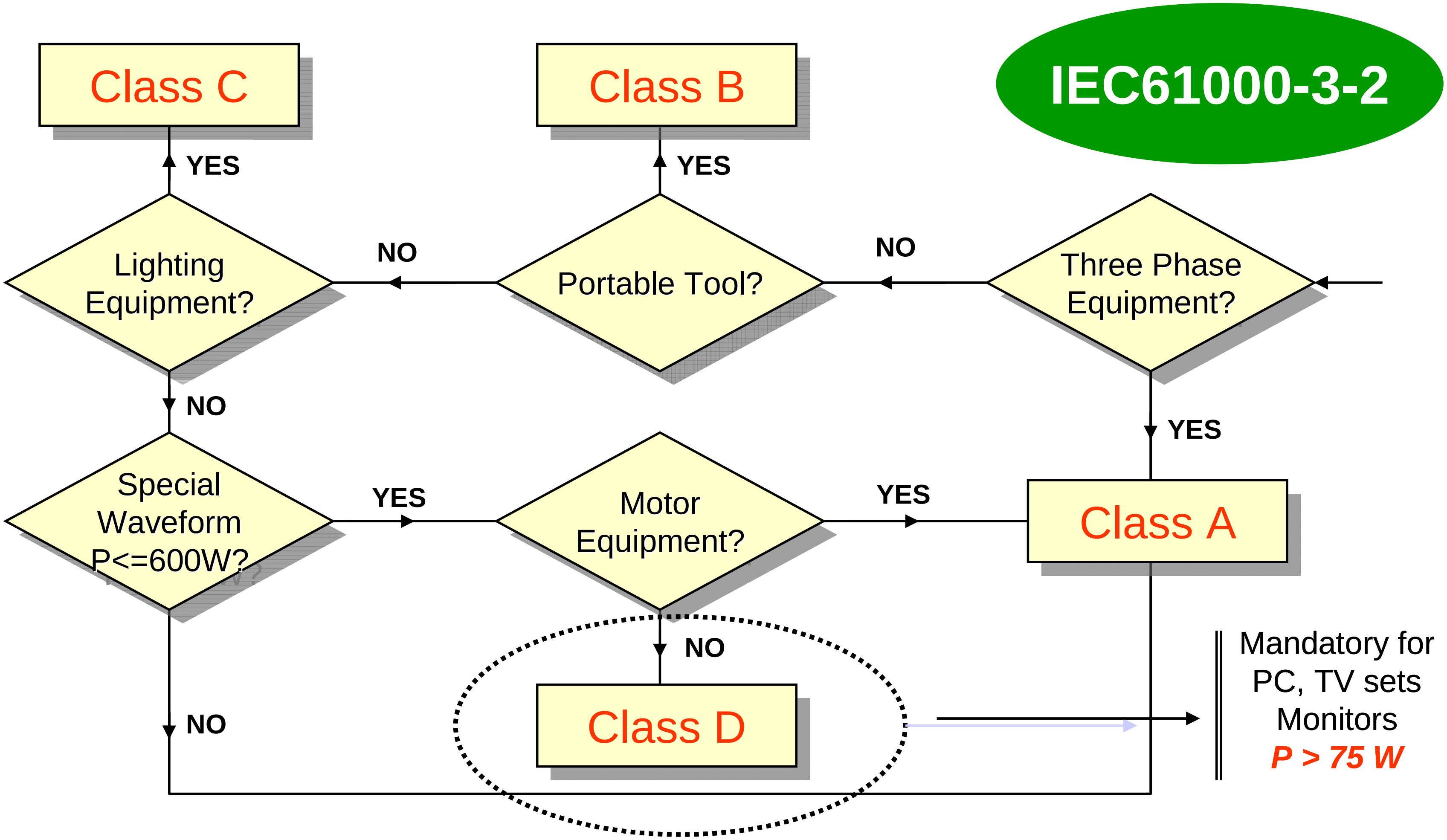
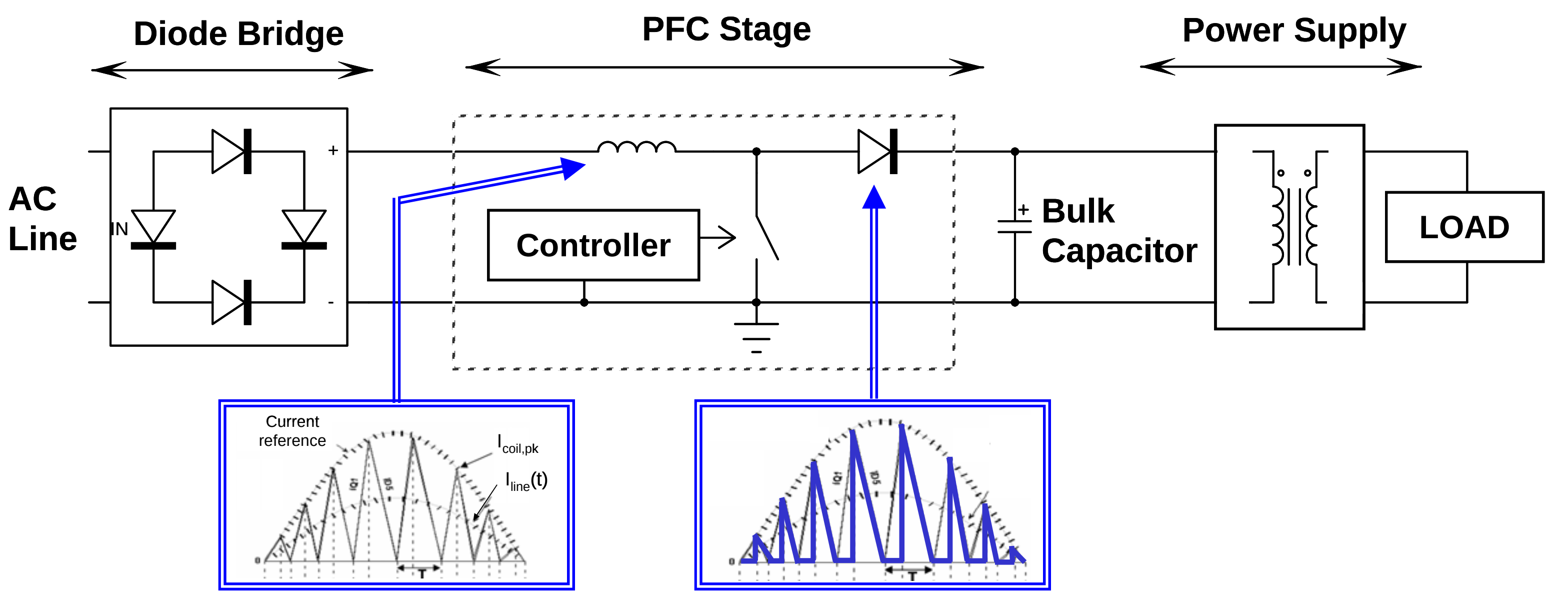
Power Factor Standard



- The standard specifies a maximum level up to harmonic 39

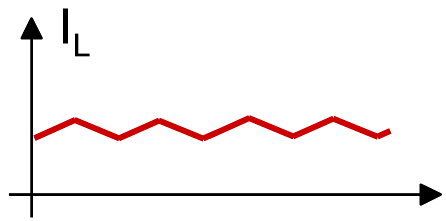
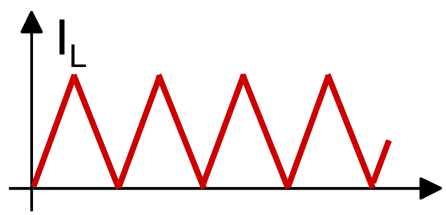
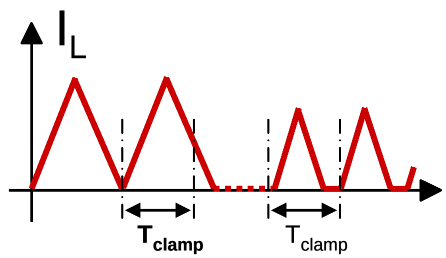
Need for a PFC Stage



- A boost pre-converter draws a sinusoidal current from the line to provide a dc voltage (bulk voltage)
- The current within the coil is made sinusoidal by:
  - Forcing it to follow a sinusoidal reference (current mode)
  - Controlling the duty-cycle appropriately (voltage mode)

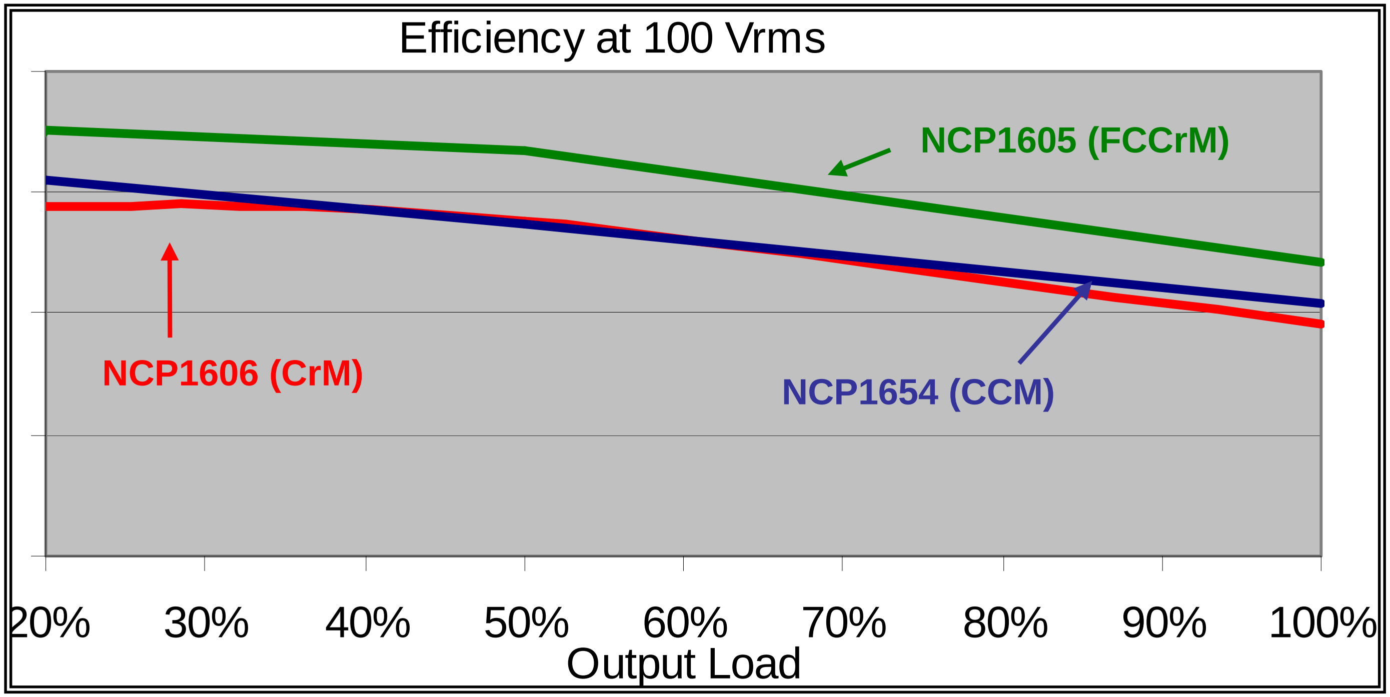
Operating Modes Overview

- ON Semiconductor offers solutions for three modes

	Operating Mode	Main Feature
	**<u>C</u>**ontinuous **<u>C</u>**onduction **<u>M</u>**ode (**CCM**)	Always hard-switching Inductor value is largest Minimized rms current **e.g.: NCP1654**
	**<u>Cr</u>**itical conduction **<u>M</u>**ode (**CrM**)	Large rms current Switching frequency is not fixed **e.g.: NCP1606**
	**<u>F</u>**requency **<u>C</u>**lamped **<u>C</u>**ritical **<u>C</u>**onduction **<u>M</u>**ode (**FCCrM**)	Large rms current Frequency is limited Reduced coil inductance **e.g.: NCP1605**

FCCrM: an Efficient Mode

- Frequency Clamped CrM seems the most efficient solution
- Efficiency of a 300 W, wide mains PFC has been measured:



The complete study will be published in the PFC handbook revision that will be released in Q1 2009.

New Needs to Address

- High efficiency for ATX power supplies:
  - Efficiency is measured at:
    - 20% $P_{out(max)}$
    - 50% $P_{out(max)}$
    - 100% $P_{out(max)}$

- Slim LCD TVs:
  - Components height is limited

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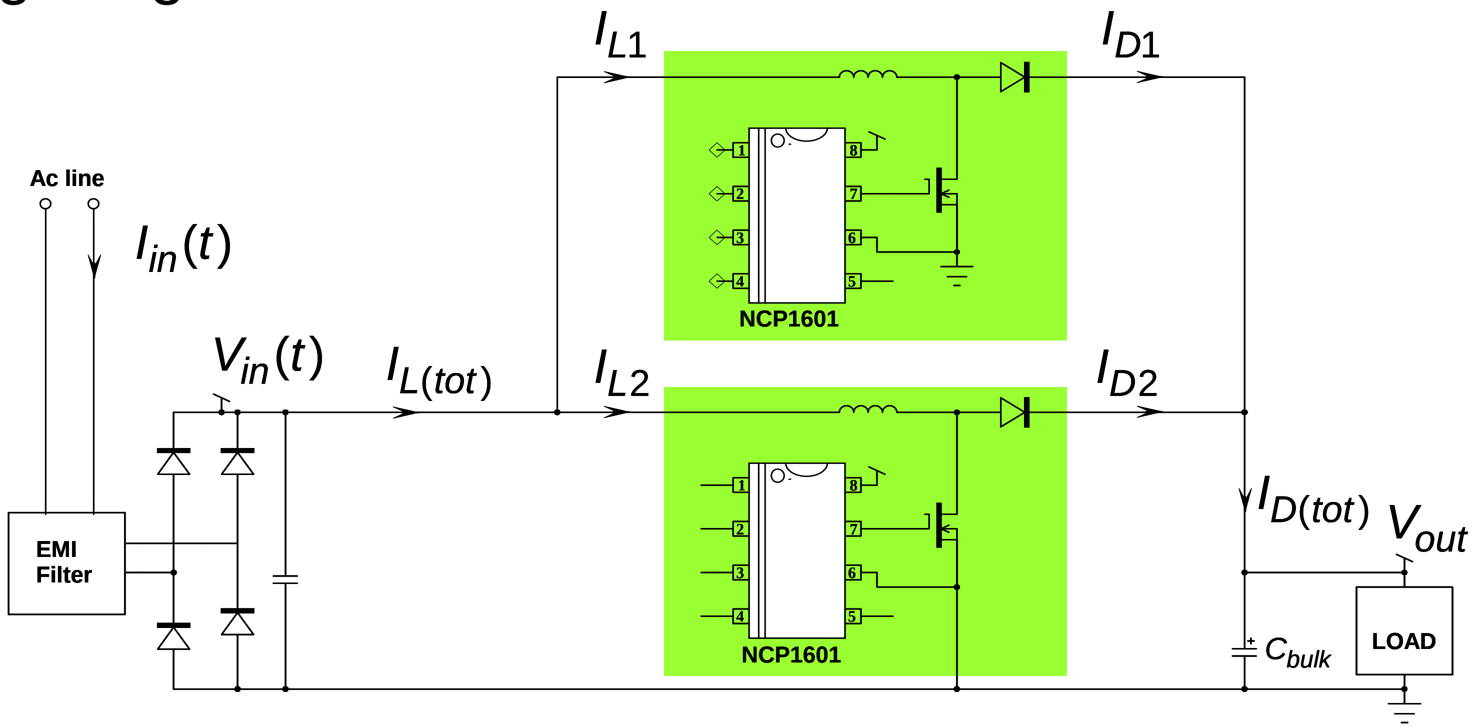
Interleaved PFC

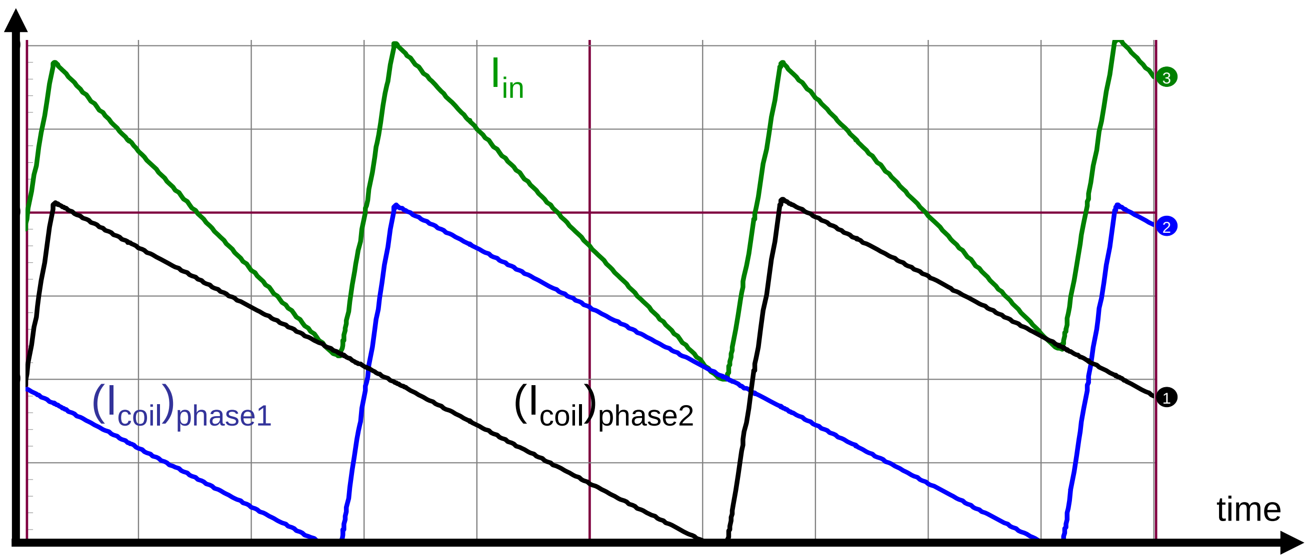
- Two small PFC stages delivering ($\boldsymbol{P}_{in(avg)}$ / 2) in lieu of a single big one



- If the two phases are out-of-phase, the resulting currents ($I_{L(tot)}$) and ($I_{D(tot)}$) exhibit a dramatically reduced ripple.

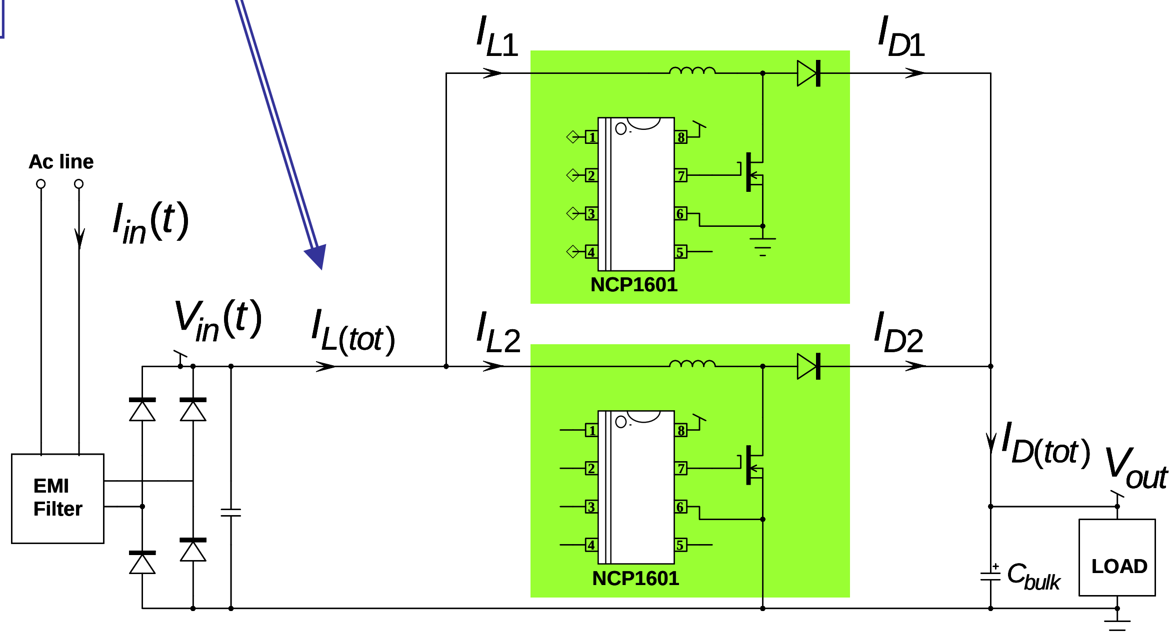
Interleaved Benefits

- More components but:
  - A 150 W PFC is easier to design than a 300 W one
  - Modular approach
  - Two DCM PFCs look like a CCM PFC converter…
    - Eases EMI filtering and reduces the output rms current
- Only interleaving of DCM PFCs will be considered



Input Current Ripple

What is the ripple of the $I_{L(tot)}$ total input current?

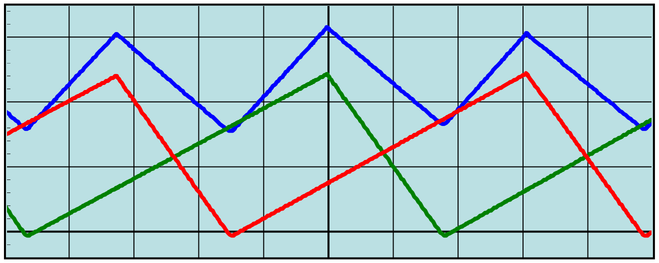


Computing the Input Current Ripple

- Let's assume that:
  - V_{in} and the switching period are constant over few cycles
  - The two branches operate in CrM

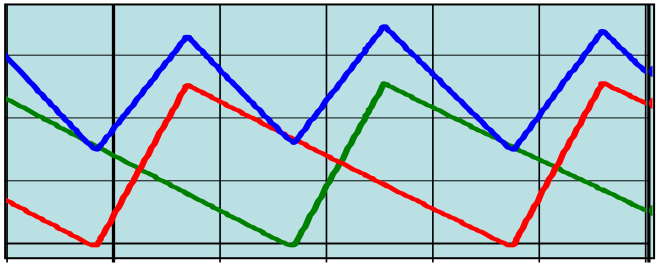
- There are two cases:
  - $V_{in}<V_{out}/2$ **(or d>0.5)**:

    The on-times of the two phases overlap. The input current peaks at the end of the conduction intervals.



  - $V_{in}>V_{out}/2$ **(or d<0.5)**:

    There is no overlap but still, the input current peaks at the end of the each conduction time

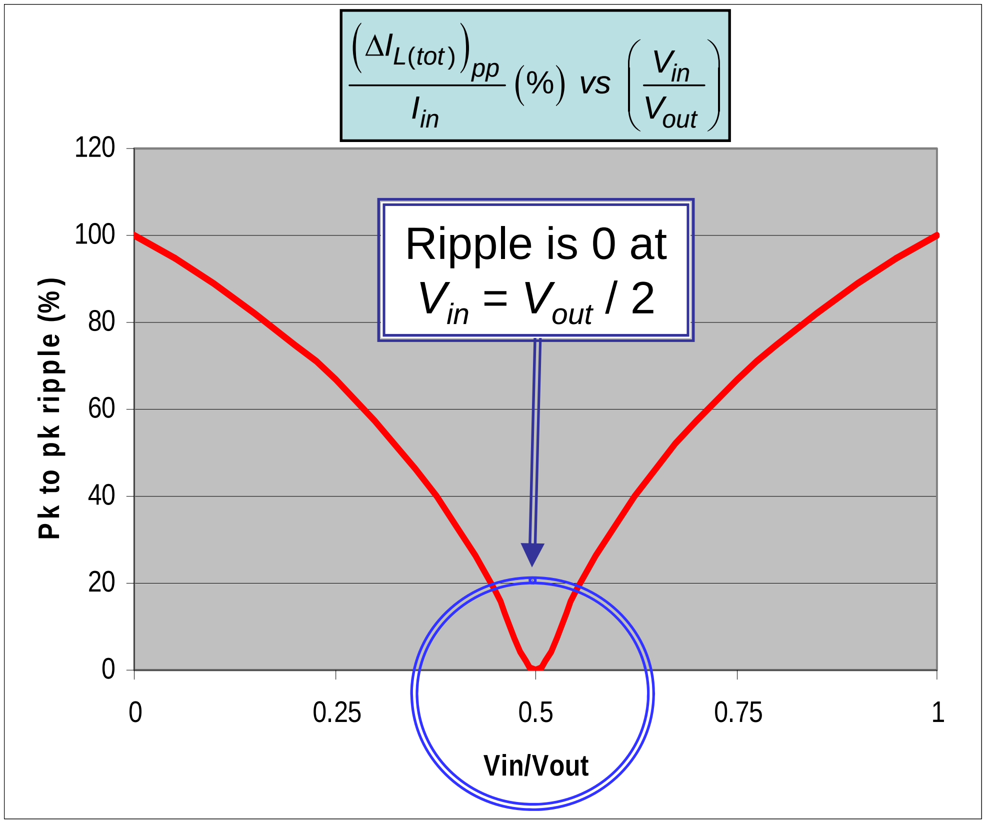


- Using $\left(d=\frac{t_{on}}{T_{sw}}=1-\frac{V_{in}}{V_{out}}\right)$, we can derive the current ripple

Finally,…

	$V_{in}(t) \le \dfrac{V_{out}}{2}$	$V_{in}(t) \ge \dfrac{V_{out}}{2}$
Averaged input current (line current)	$I_{in}(t) = \left\langle I_{L(tot)} \right\rangle_{T_{sw}} = \dfrac{V_{in}}{R_{in}} = \dfrac{V_{in} \cdot P_{in(avg)}}{V_{in(rms)}^{2}}$	
Peak to peak ripple	$\left(\Delta I_{L(tot)}\right)_{pp} = I_{in} \cdot \left(1 - \dfrac{V_{in}}{V_{out} - V_{in}}\right)$	$\left(\Delta I_{L(tot)}\right)_{pp} = I_{in} \cdot \left(2 - \dfrac{V_{out}}{V_{in}}\right)$
Peak Current envelop	$\left(I_{L(tot)}\right)_{pk} = 2 \cdot I_{in} \cdot \left(1 - \dfrac{V_{out}}{4 \cdot \left(V_{out} - V_{in}\right)}\right)$	$\left(I_{L(tot)}\right)_{pk} = 2 \cdot I_{in} \cdot \left(1 - \dfrac{V_{out}}{4 \cdot V_{in}}\right)$
Valley Current envelop	$\left(I_{L(tot)}\right)_{v} = I_{in} \cdot \dfrac{V_{out}}{2 \cdot (V_{out} - V_{in})}$	$\left(I_{L(tot)}\right)_{v} = \dfrac{P_{in(avg)} \cdot V_{out}}{2 \cdot V_{in(rms)}^{2}}$

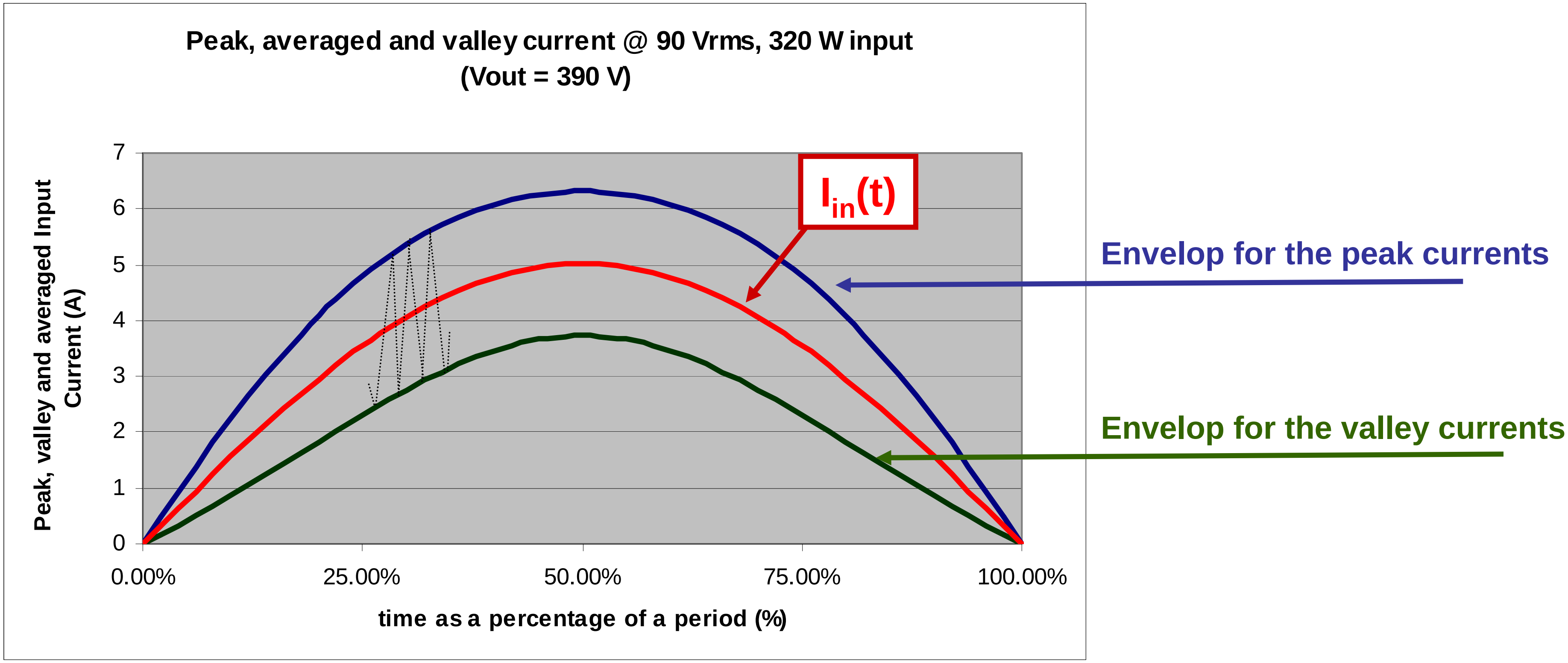
Peak to Peak Ripple of the Input Current



- The input ripple only depends on the ratio (V_{in}/V_{out}):
- Unlike in CCM:
  - L plays no role
  - The ripple percentage does not depend on the load
- At low line ($V_{in}/V_{out}=0.3$), the ripple is +/-28% (at the sinusoid top, assuming 180° phase shift and CrM operation)

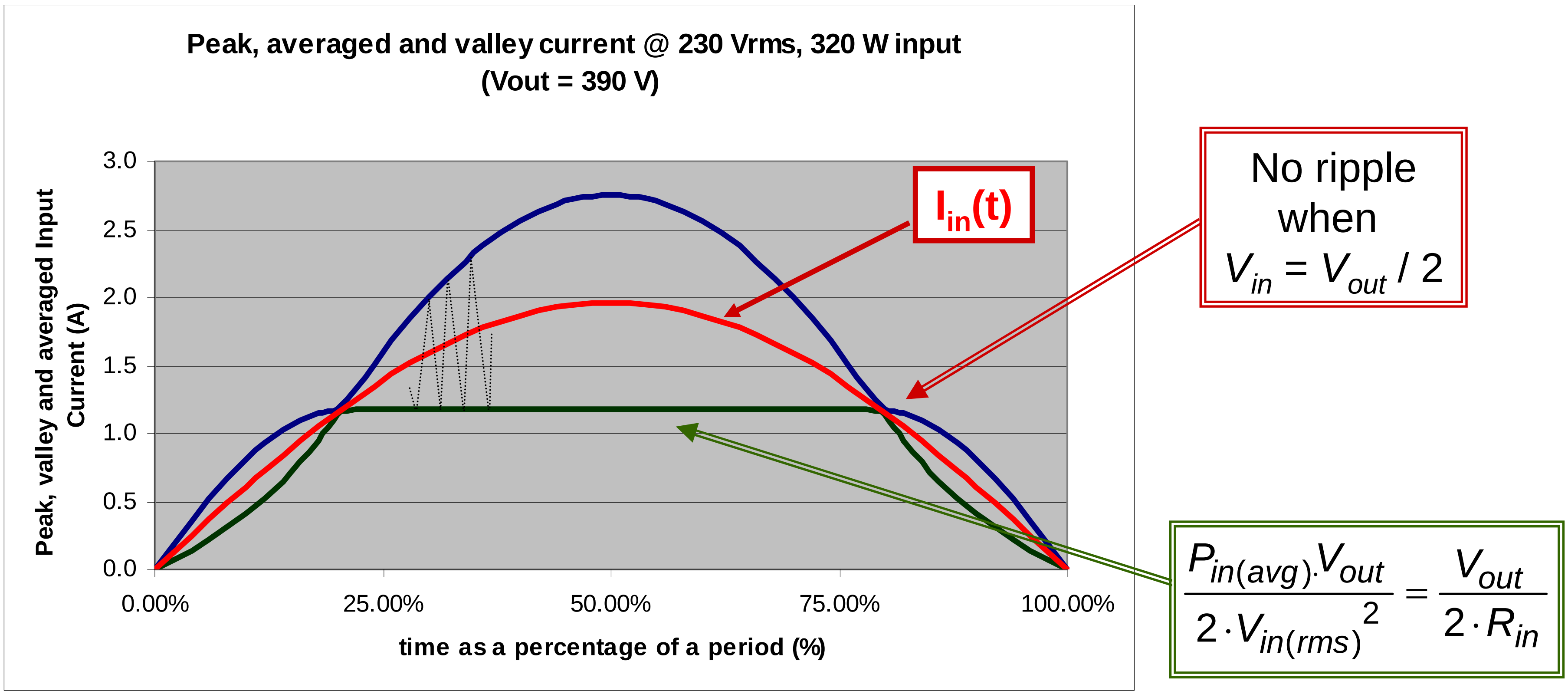
Input Current Ripple at Low Line

- When V_{in} remains lower than $V_{out}/2$, the input current looks like that of a CCM, hysteretic PFC
- ($I_{L(tot)}$) swings between two nearly sinusoidal envelops



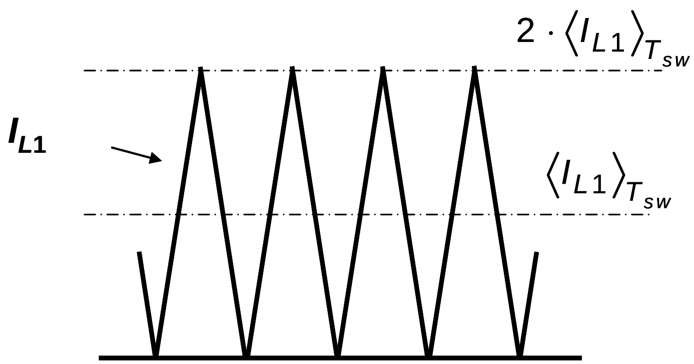
Input Current Ripple at High Line

- When V_{in} exceeds $(V_{out}/2)$, the valley current is constant!
- It equates $\left(\dfrac{V_{out}}{2 \cdot R_{in}}\right)$ where R_{in} is the PFC input impedance



Line Input Current

- <u>For each branch</u>, somewhere within the sinusoid:



- The sum of the two averaged, sinusoidal phases currents gives the total line current:

$$I_{in} = \left\langle I_{L(tot)} \right\rangle_{\frac{T_{sw}}{2}} = \langle I_{L1} \rangle_{T_{sw}} + \langle I_{L2} \rangle_{T_{sw}}$$

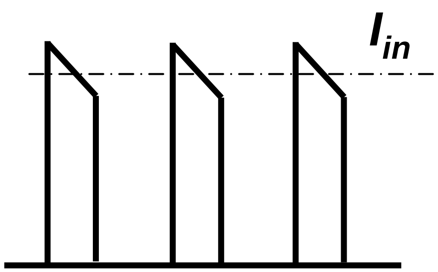
- Assuming a perfect current balacing:

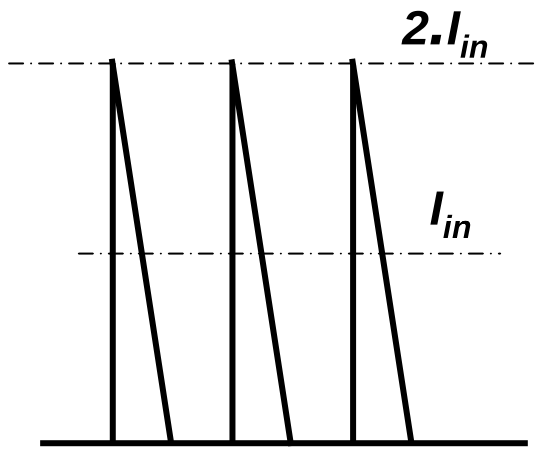
$$2 \cdot \langle I_{L1} \rangle_{T_{sw}} = 2 \cdot \langle I_{L2} \rangle_{T_{sw}} = I_{in}$$

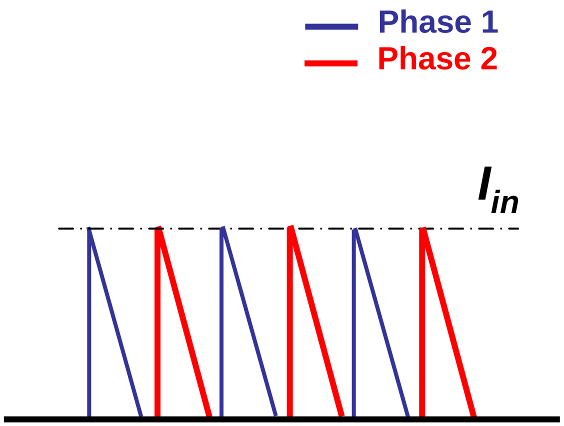
- **The peak current in each branch is I_{in}(t)**

Ac Component of the Refueling Current

- The refueling current (output diode(s) current) depends on the mode:







Single phase CCM

rms value over T_{sw}

$$I_{in}\cdot\sqrt{\frac{V_{in}}{V_{out}}}$$

Single phase CrM

rms value over T_{sw}

$$\frac{2}{\sqrt{3}}\cdot I_{in}\sqrt{\frac{V_{in}}{V_{out}}}$$

Interleaved CrM

rms value over T_{sw}

$$\sqrt{\frac{2}{3}}\cdot I_{in}\sqrt{\frac{V_{in}}{V_{out}}}$$

A Reduced RMS Current in the Bulk Capacitor

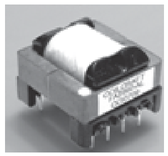
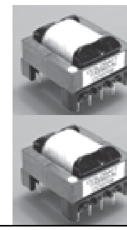
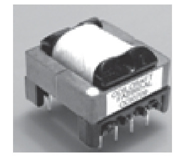
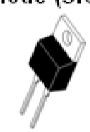
- Integration over the sinusoid leads to (resistive load):

	Single phase CCM PFC	Single phase CrM or FCCrM PFC	Interleaved CrM or FCCrM PFC
Diode(s) rms current (***I***$_{D(rms)}$)	$\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$	$\frac{2}{\sqrt{3}}\cdot\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$	$\sqrt{\frac{2}{3}}\cdot\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$
Capacitor rms current (***I***$_{C(rms)}$)	$\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$	$\sqrt{\frac{32\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{9\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$	$\sqrt{\frac{16\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{9\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$
300 W, V_{out}=390V $V_{in(rms)}$=90 V	$I_{D(rms)}$ = 1.9 A $I_{C(rms)}$ = 1.7 A	$I_{D(rms)}$ = 2.2 A $I_{C(rms)}$ = 2.1 A	$I_{D(tot)(rms)}$ = 1.5 A $I_{C(rms)}$ = 1.3 A

- Interleaving dramatically reduces the rms currents

➔ **reduced losses, lower heating, increased reliability**

Summary

	Single FCCrM stage		Interleaved FCCrM stage		Single CCM stage	
	General	300-W, wide mains	General	300-W, wide mains	General	300-W, wide mains
$\Delta I_{in(max)}$ (A)	Independent on L	10.0 A	Independent on L	2.6 A	Depends on L	2.6 A (at 90 V_{rms}, full load if L = 250 µH)
Inductor	1 coil 	75 µH $I_{L,pk(max)}$ = 10 A $I_{L,rms(max)}$ = 4.1 A $L^*I_{pk}^2$ = 7.5 mJ	2 coils 	150 µH $I_{L,pk(max)}$ = 5.0 A $I_{L,rms(max)}$ = 2.0 A $L^*I_{pk}^2$ = 3.7 mJ	1 coil 	250 µH $I_{L,pk(max)}$ = 6.3 A $I_{L,rms(max)}$ = 3.5 A $L^*I_{pk}^2$ = 9.9 mJ
Total MOSFET conduction losses (with below MOSFETs)	$\frac{4 R_{DS(on)}}{3} \cdot \left(\frac{P_{in(avg)}}{V_{in(rms)}}\right)^2 \cdot \left(1 - \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi V_{out}}\right)\right)$	4.6 W	$\frac{2 \cdot R_{DS(on)}}{3} \cdot \left(\frac{P_{in(avg)}}{V_{in(rms)}}\right)^2 \cdot \left(1 - \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi V_{out}}\right)\right)$	4.6 W	$R_{DS(on)} \cdot \left(\frac{P_{in(avg)}}{V_{in(rms)}}\right)^2 \cdot \left(1 - \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi V_{out}}\right)\right)$	3.5 W
MOSFETs		1 * SPP20N60 or 2* SPP11N60		2 * SPP11N60		1 * SPP20N60 or 2* SPP11N60
Diode	Ultrafast	MUR550 (TO220) 	2 * Ultrafast	2 * MUR550 (axial) 	Low t_{rr} diode	High speed diode (SiC..) 
$I_{C(rms)(max)}$ (A)	$\sqrt{\frac{32\sqrt{2} \cdot \left(\frac{P_{out}}{\eta}\right)^2}{9\pi \cdot V_{in(rms)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}}\right)^2}$	2.0	$\sqrt{\frac{16\sqrt{2} \cdot \left(\frac{P_{out}}{\eta}\right)^2}{9\pi \cdot V_{in(rms)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}}\right)^2}$	1.3	$\sqrt{\frac{8\sqrt{2} \cdot \left(\frac{P_{out}}{\eta}\right)^2}{3\pi \cdot V_{in(rms)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}}\right)^2}$	1.7
EMI complexity	DM: high CM: moderate		DM: moderate CM: moderate		DM: moderate CM: high	
Characteristics	Compact design		Low profile designs		Compact design	

Compared to CrM, FCCrM allows the use of smaller inductances (due to frequency clamp)

The inductance for the single and interleaved FCCrM stages is based on a 130 kHz frequency clamp (high frequency design).

The switching frequency is also supposed to be 130 kHz for the CCM stage.

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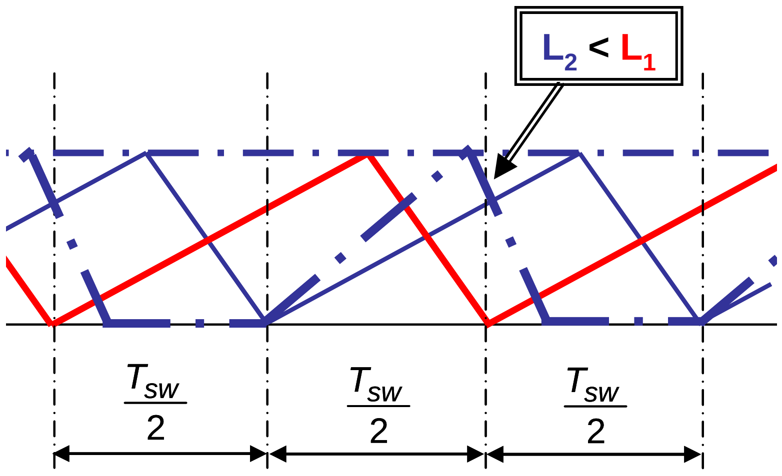
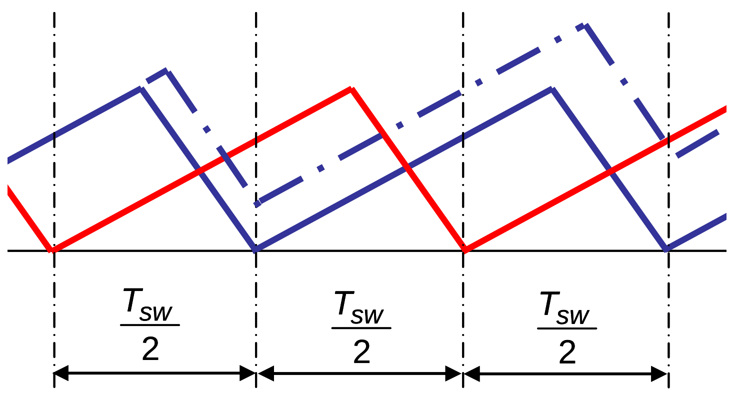
Interleaving: Master/Slave Approach…

- The master branch operates freely
- The slave follows with a 180° phase shift
- Main challenge: maintaining the CrM operation (no CCM, no dead-time)



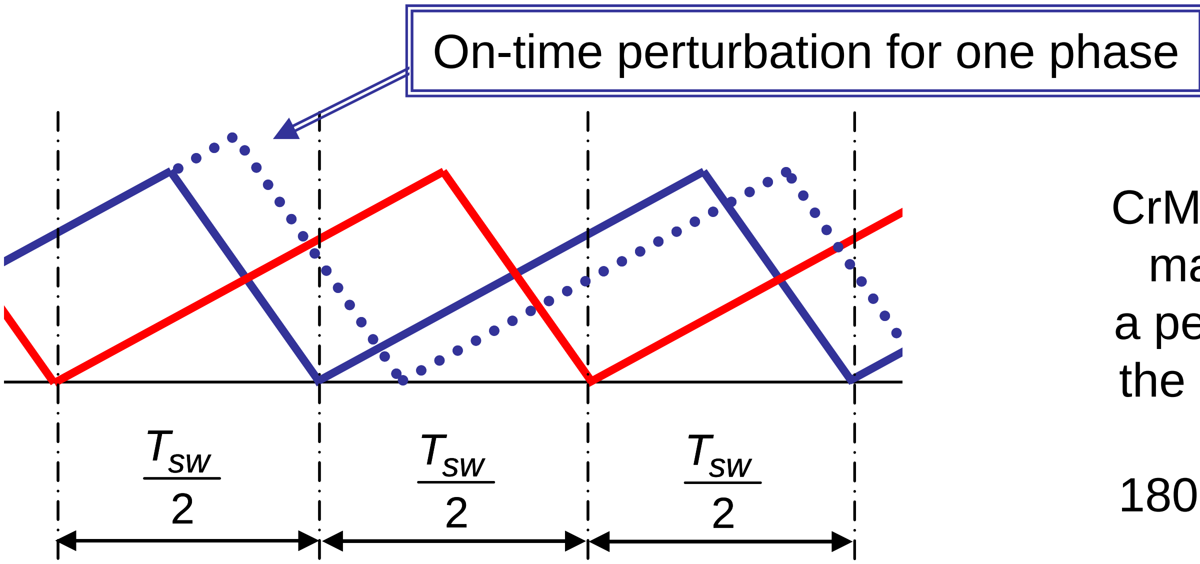
Current mode: inductor unbalance



Voltage mode: on-time shift

Interleaving: Independent Phases Approach…

- Each phase properly operates in CrM or FCCrM.
- The two branches interact to set the 180° phase shift
- Main challenge: to keep the proper phase shift

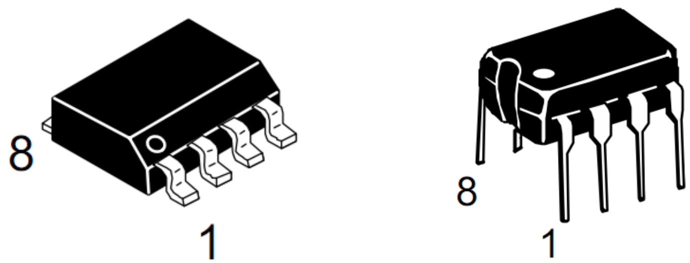


CrM operation is maintained but a perturbation of the on-time may degrade the 180° phase shift

- **We selected this approach**

General Principle on a Two-NCP1601 Solution

- The solution lies on the Frequency Clamp Critical Conduction mode, unique scheme developed by ON Semiconductor (NCP1601)



- Two NCP1601 drive two independent PFC branches:
  - Auxiliary windings are used to detect the core reset of each branch
  - The current sensing is shared by the two stages for protection only (Over Current Limitation)

- The two branches are operating in voltage mode

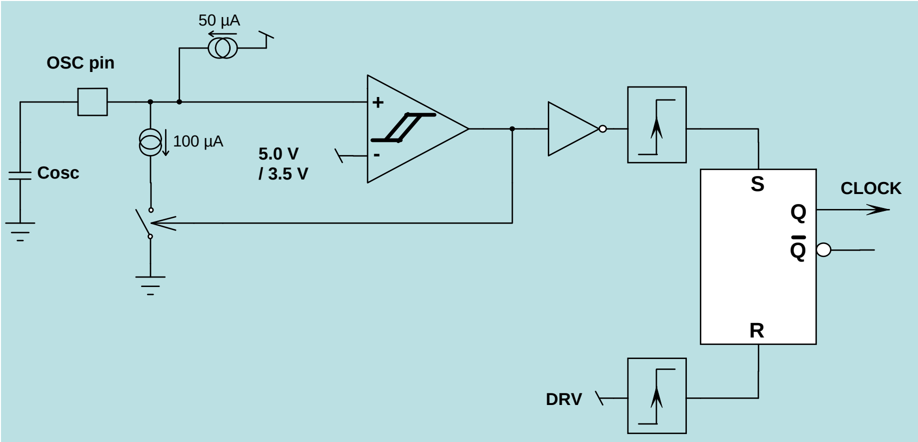
Synchronization: the Main Challenge

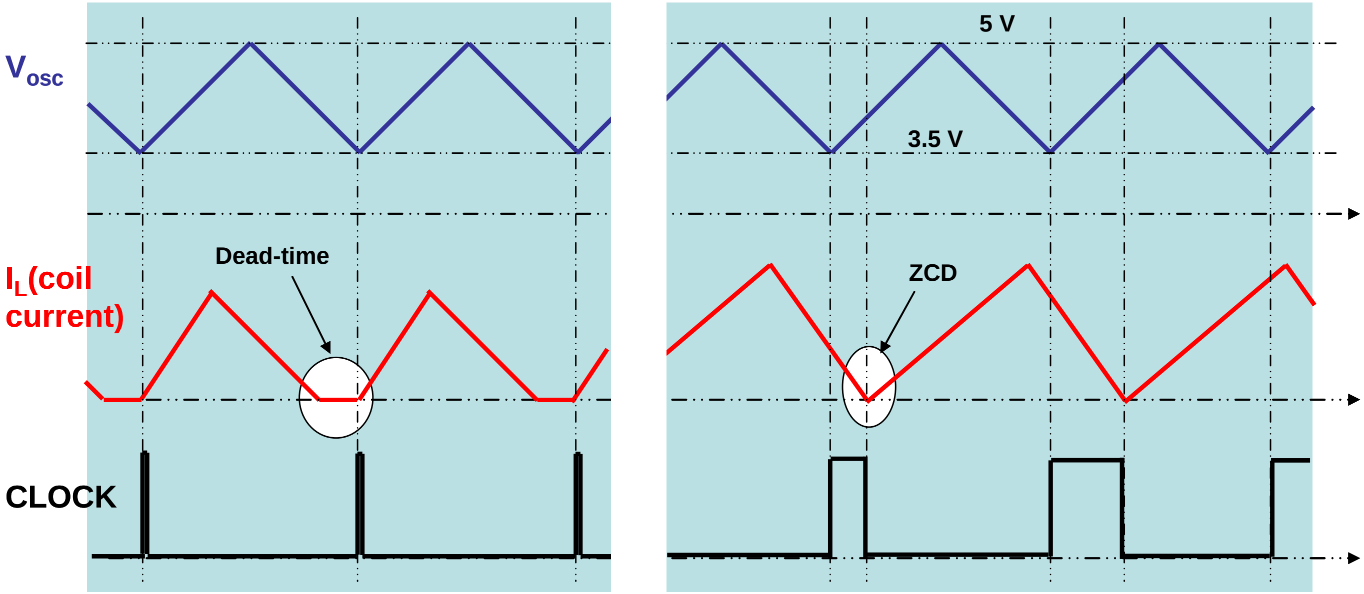
- One driver (DRV2) synchronizes the two branches so that:
  - Branch 1 (DRV1) cannot turn high until a time τ has elapsed
  - Branch 2 (DRV2) cannot dictate a new conduction phase within 2τ

- Hence:
  - In fixed frequency operation, the switching period for each branch is 2τ and the two phases are naturally interleaved
  - In CrM, the switching frequency is that imposed by the current cycle ($T_{sw}>2\tau$) and must stabilize out of phase.

- Possible slippages are contained by a phase compensation circuitry (refer to www.onsemi.com for detailed AN available in Q4 2008).

NCP1601 Synchronization Capability





Fixed Frequency

Critical Conduction Mode

- The oscillator oscillates between 3.5 and 5 V
- The NCP1601 generates a clock when the oscillator goes below 3.5 V
- The clock signal is stored until ZCD is detected

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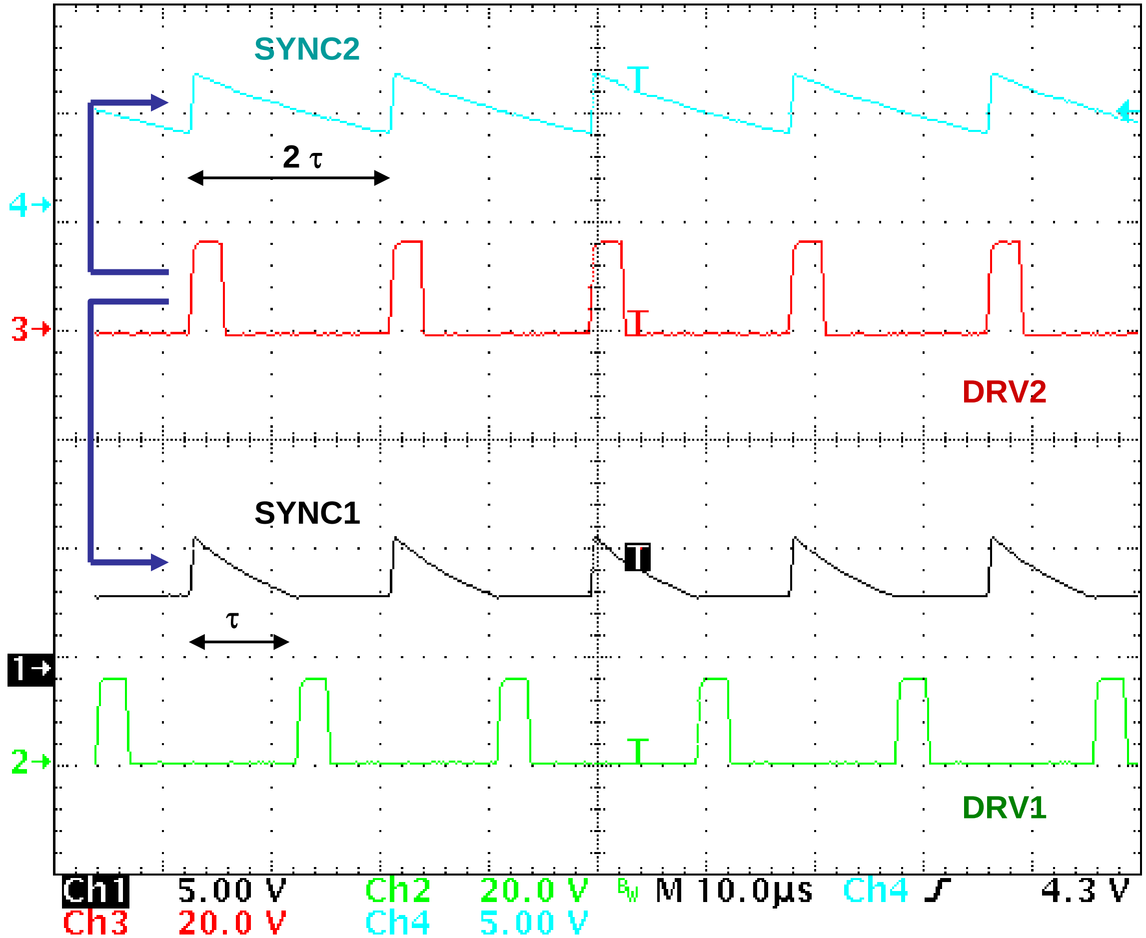
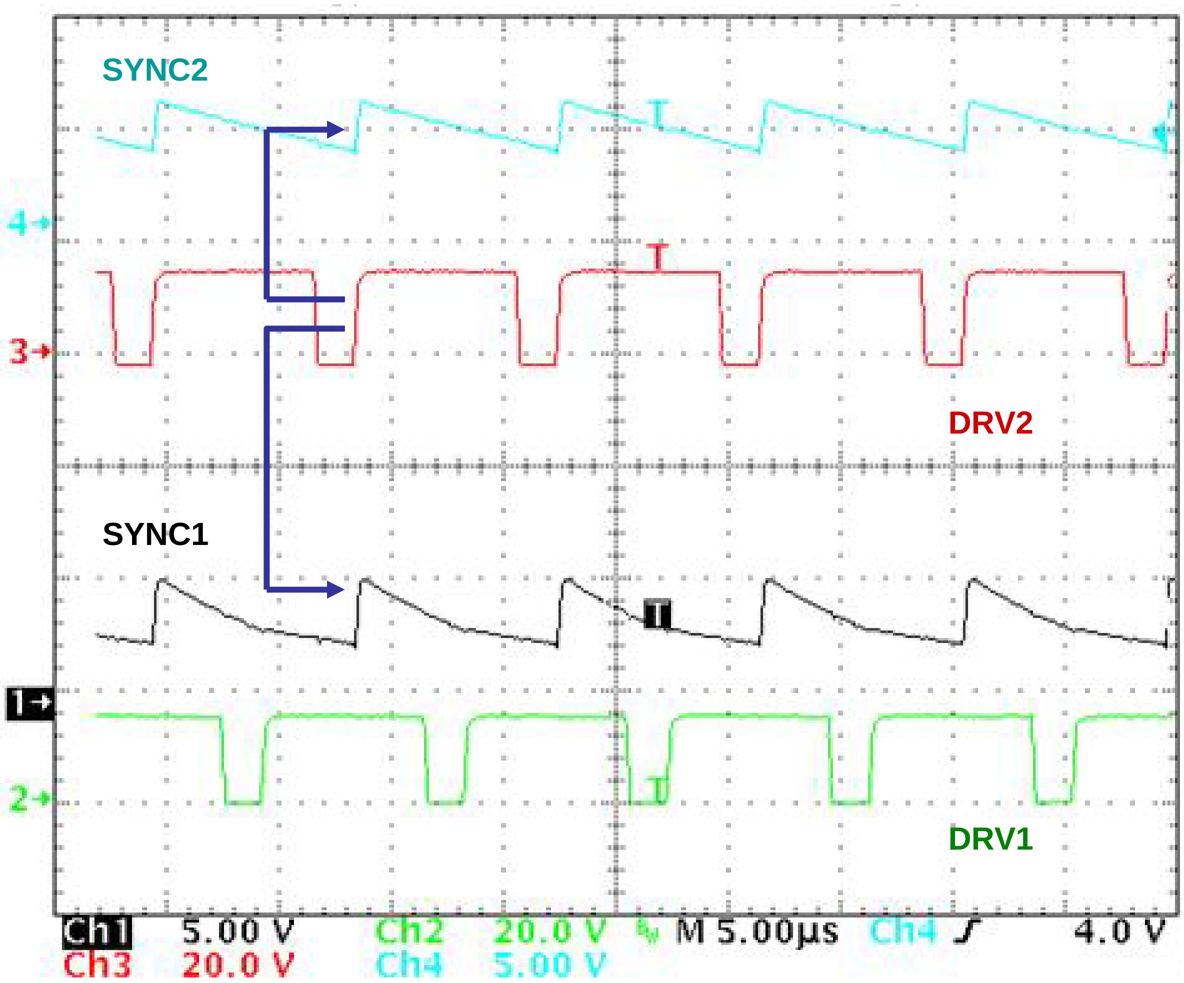
Operation @ 230 V_{rms}, Medium Load



- Each stage operates in fixed frequency mode
- Both branches are synchronized to DRV2
- A new DRV2 pulse can take place after 2τ
- A new DRV1 pulse can occur after τ
- The switching period for each branch is then 2τ and they operate out of phase.

❑ A new drive sequence cannot take place as long as the SYNC signal remains higher than 3.5 V (see NCP1601 operation).

Operation at Low Line, Full Load

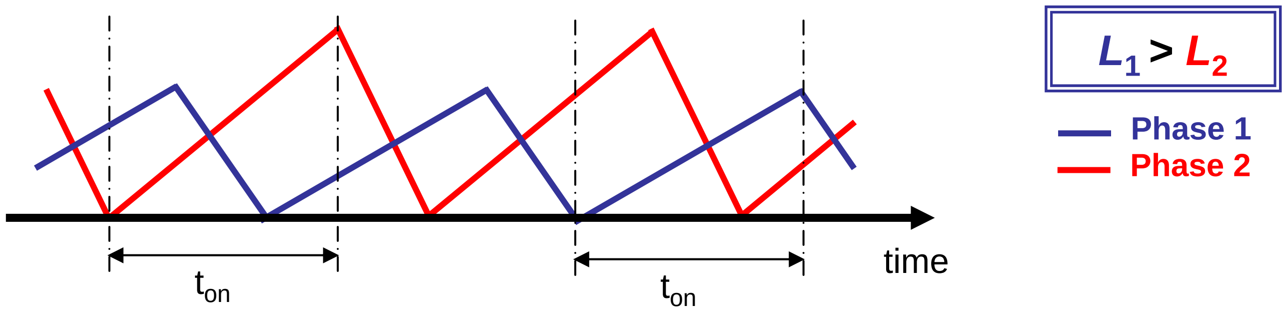


- The circuit operates in critical conduction mode
- The operation of both branches are synchronized to DRV2
- A new DRV2 pulse can take place after 2τ, but the MOSFET turn on is delayed until the core is reset
- A new DRV1 pulse can occur after τ, but again, the MOSFET turn on is delayed until the core is reset

Remarks on the Solution

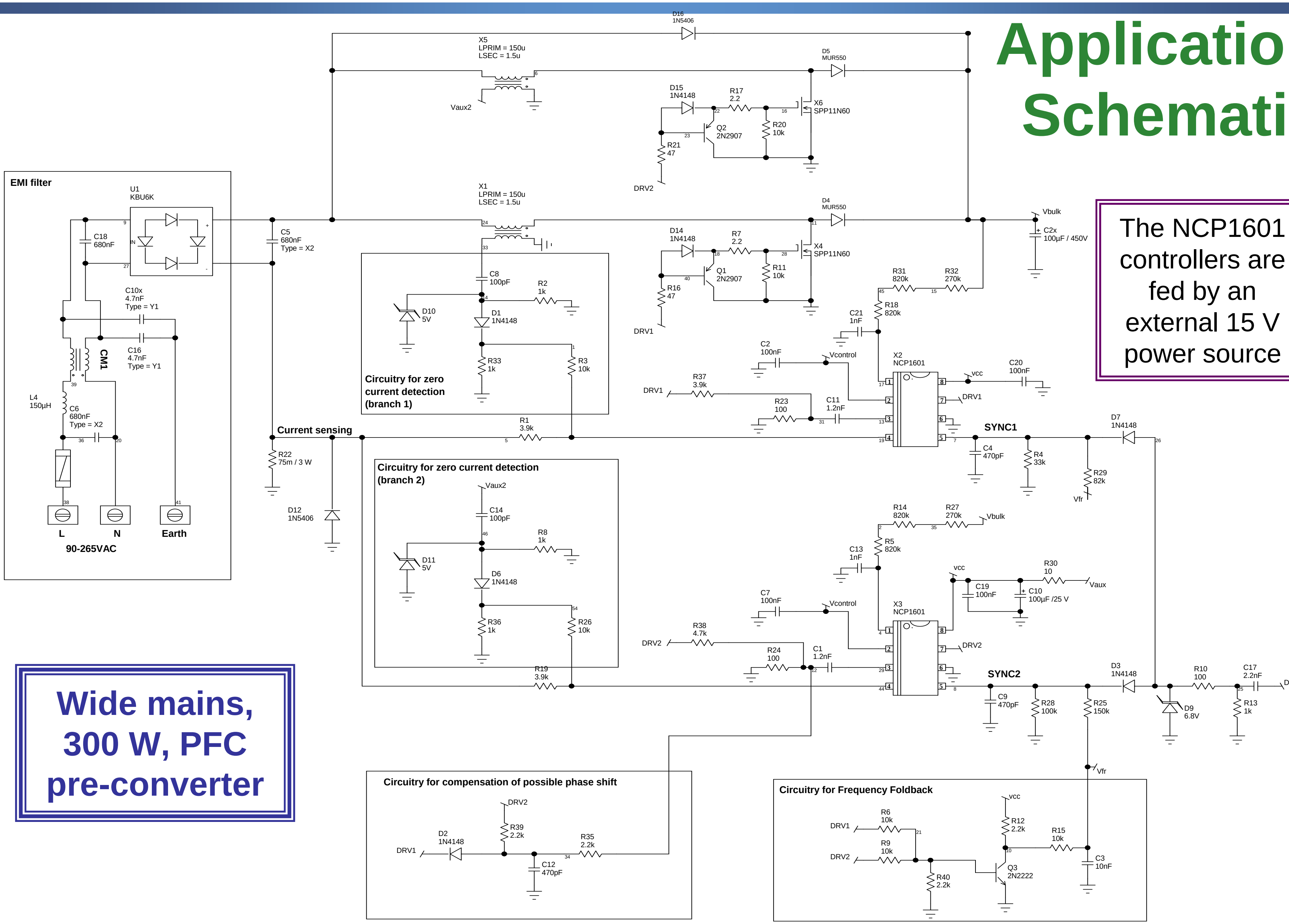
- The NCP1601 operates in voltage mode
- Same on-time and hence switching period in the two branches
- A coil imbalance
  - Does not affect the switching period
  - “Only” causes a difference in the power amount conveyed by each branch

$$\frac{I_{in(1)}}{I_{in(2)}} = \frac{L_2}{L_1}$$



- The two branches are synchronized but they operate independently:
  - Discontinuous conduction mode is guaranteed (zero current detection)
  - No risk of CCM operation
  - Both branches enter CrM at full load

Application Schematic

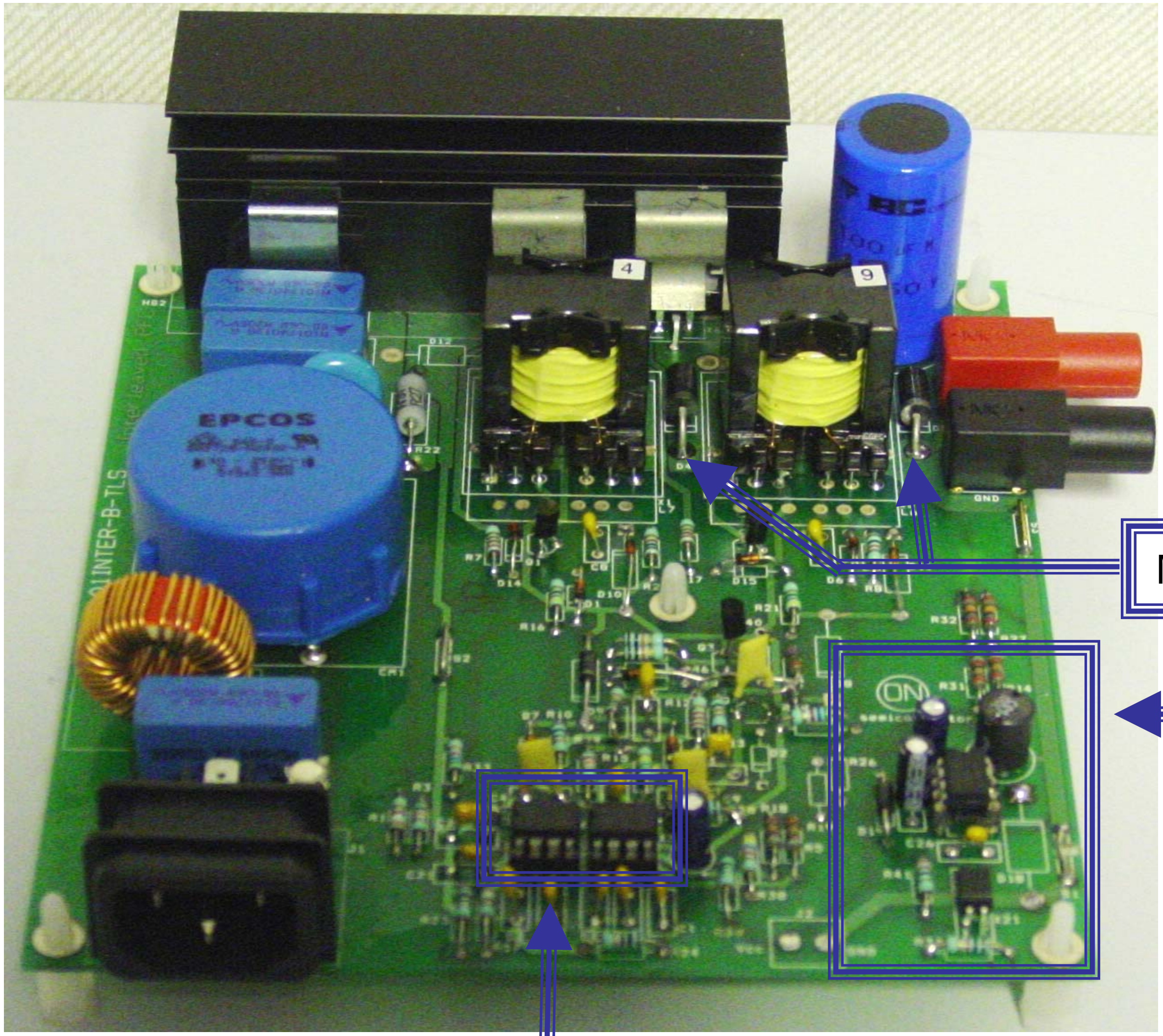


The NCP1601 controllers are fed by an external 15 V power source

Wide mains, 300 W, PFC pre-converter

The Board…

Wide mains, 300 W, PFC pre-converter

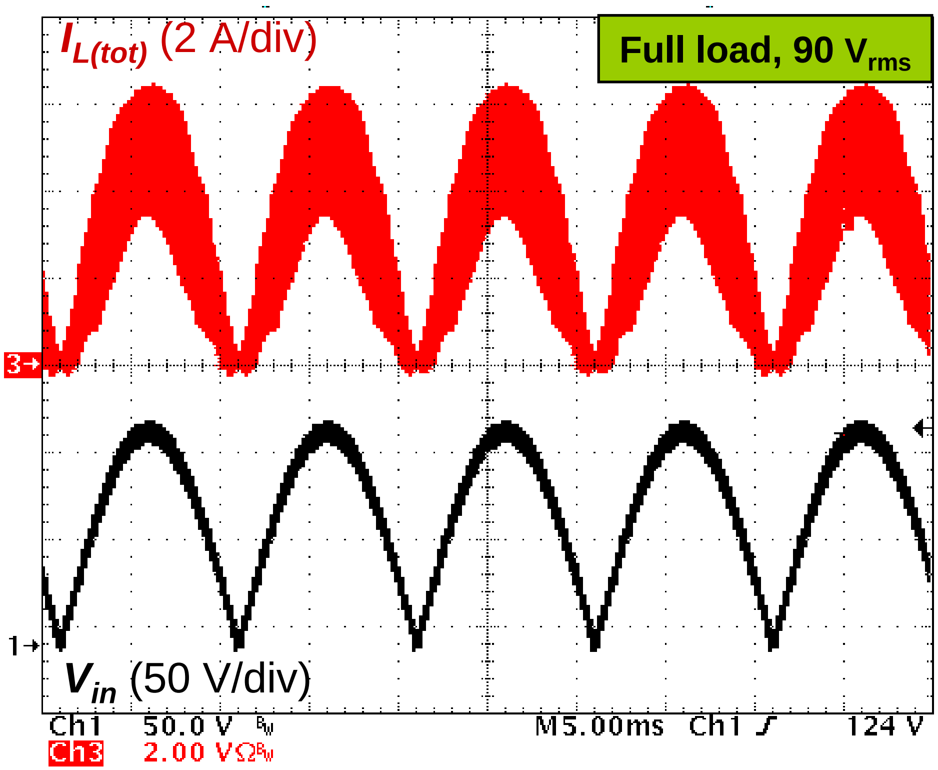


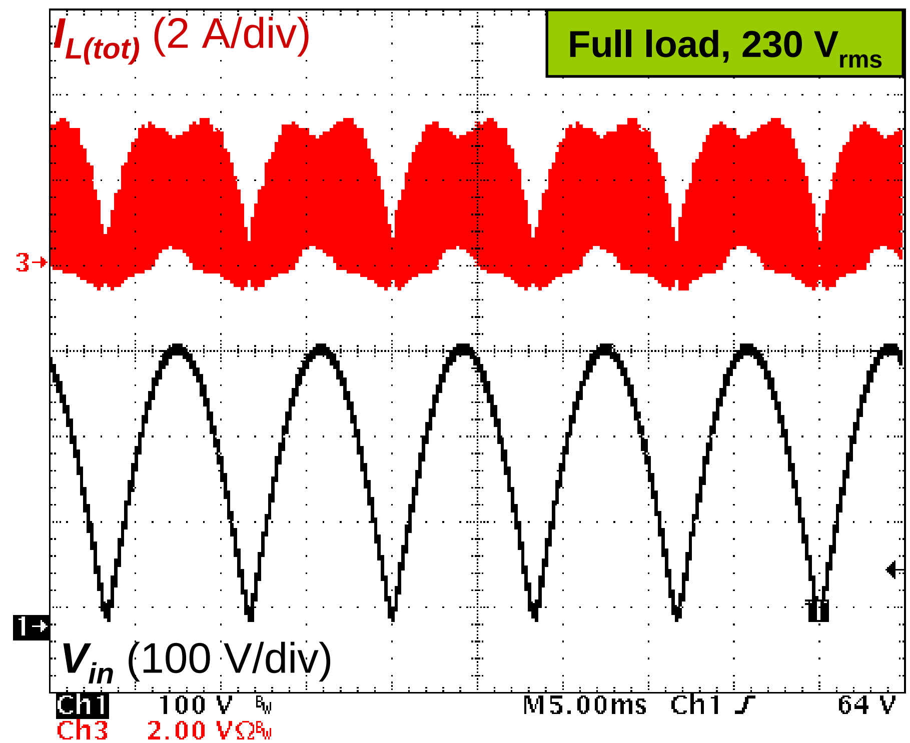
MUR550

Buck converter to provide Vcc (not used for test)

Two NCP1601 circuits

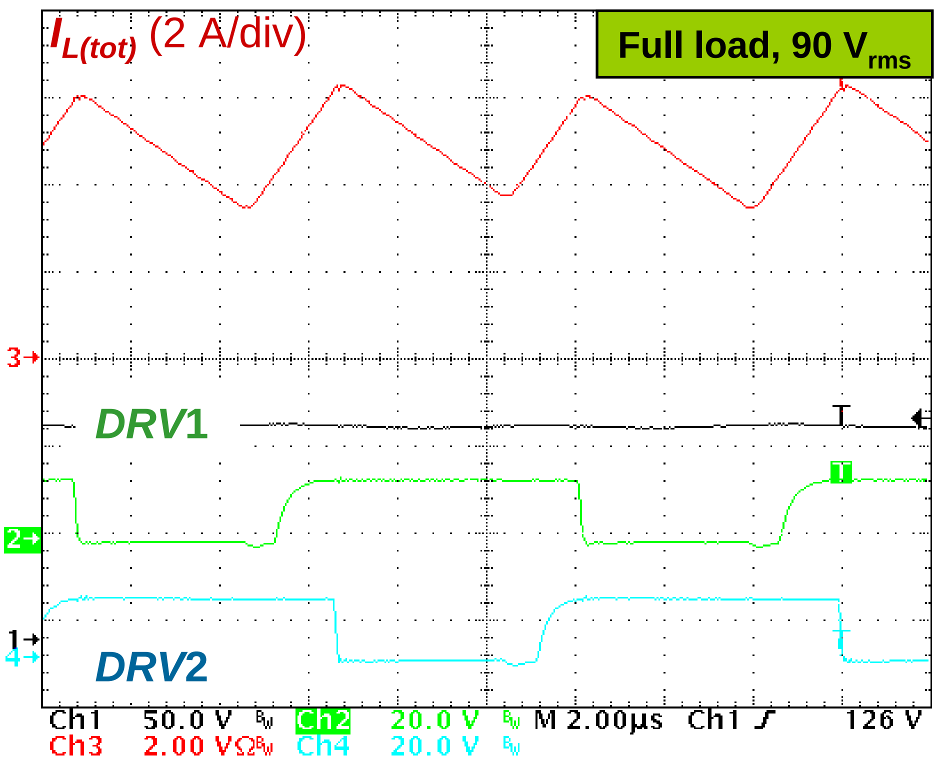
Input Voltage and Current

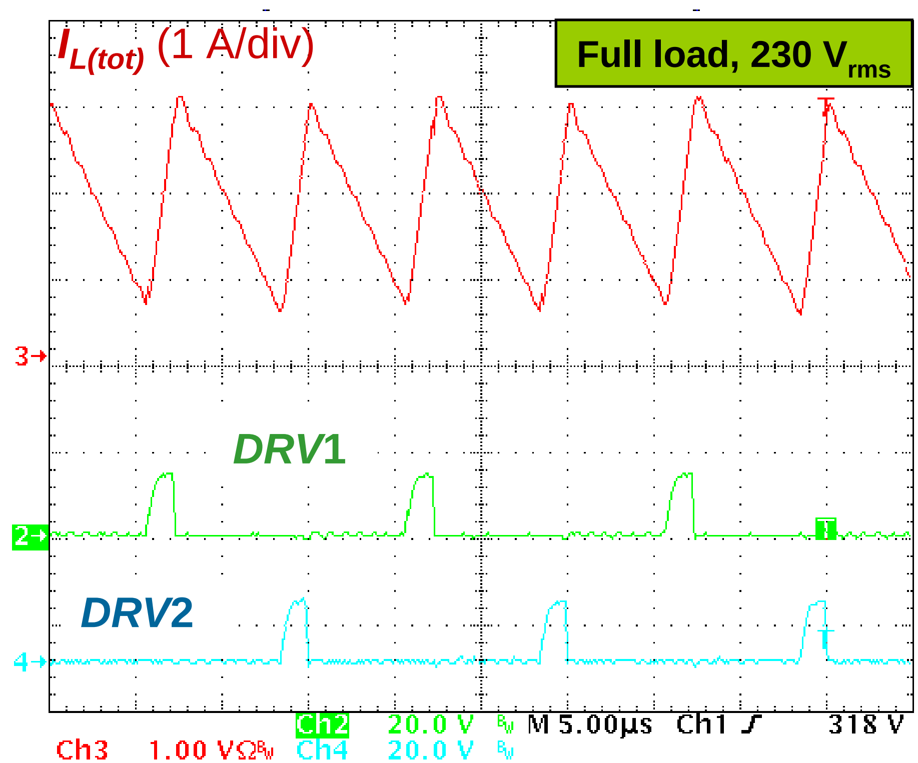




- As expected, the input current looks like a CCM one
- At high line, frequency foldback influences the ripple

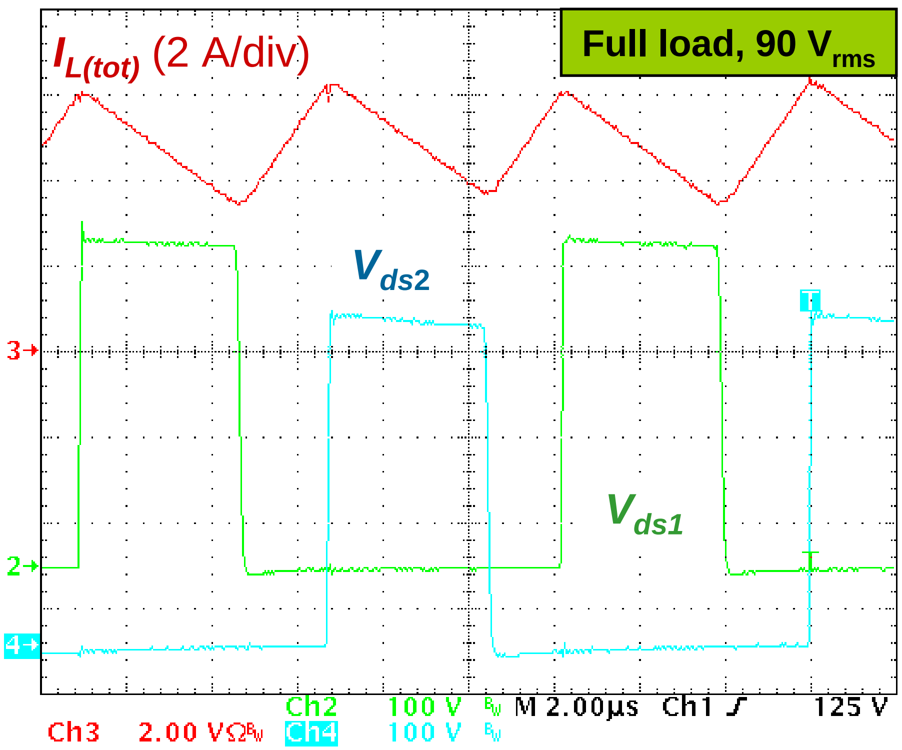
Zoom of the Precedent Plots

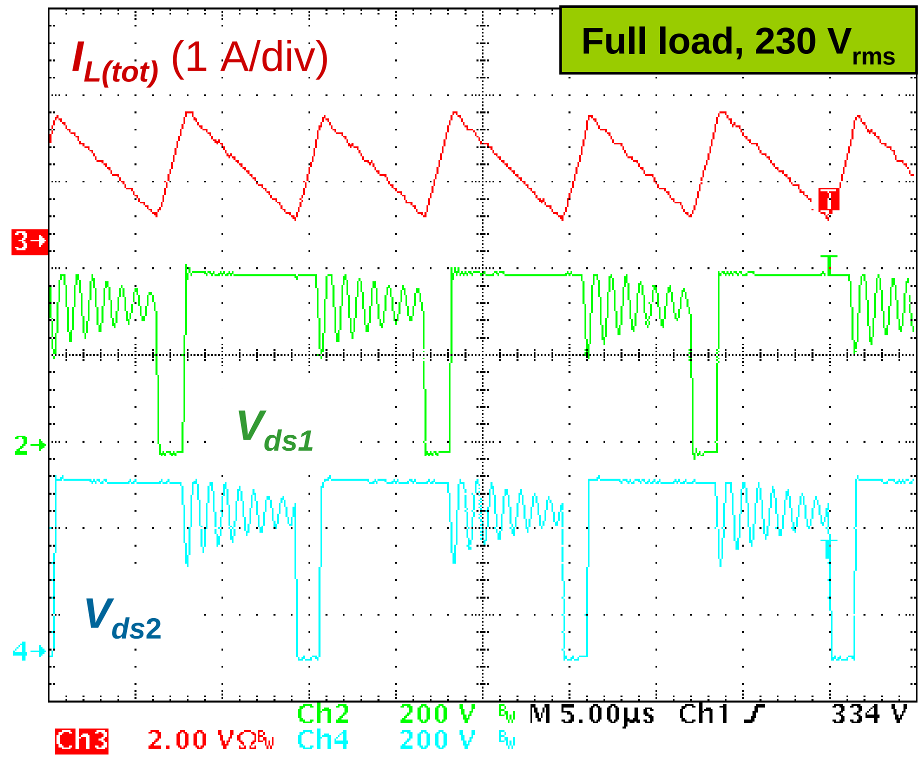




- These plots were obtained at the sinusoid top
- The current swings at twice the frequency of each phase
- At low and high line, the phase shift is substantially 180°

No Overlap between the Refueling Sequences





- CrM at low line with valley switching
- Fixed frequency operation at high line (frequency foldback)
- No overlap between the demag. phases in both cases

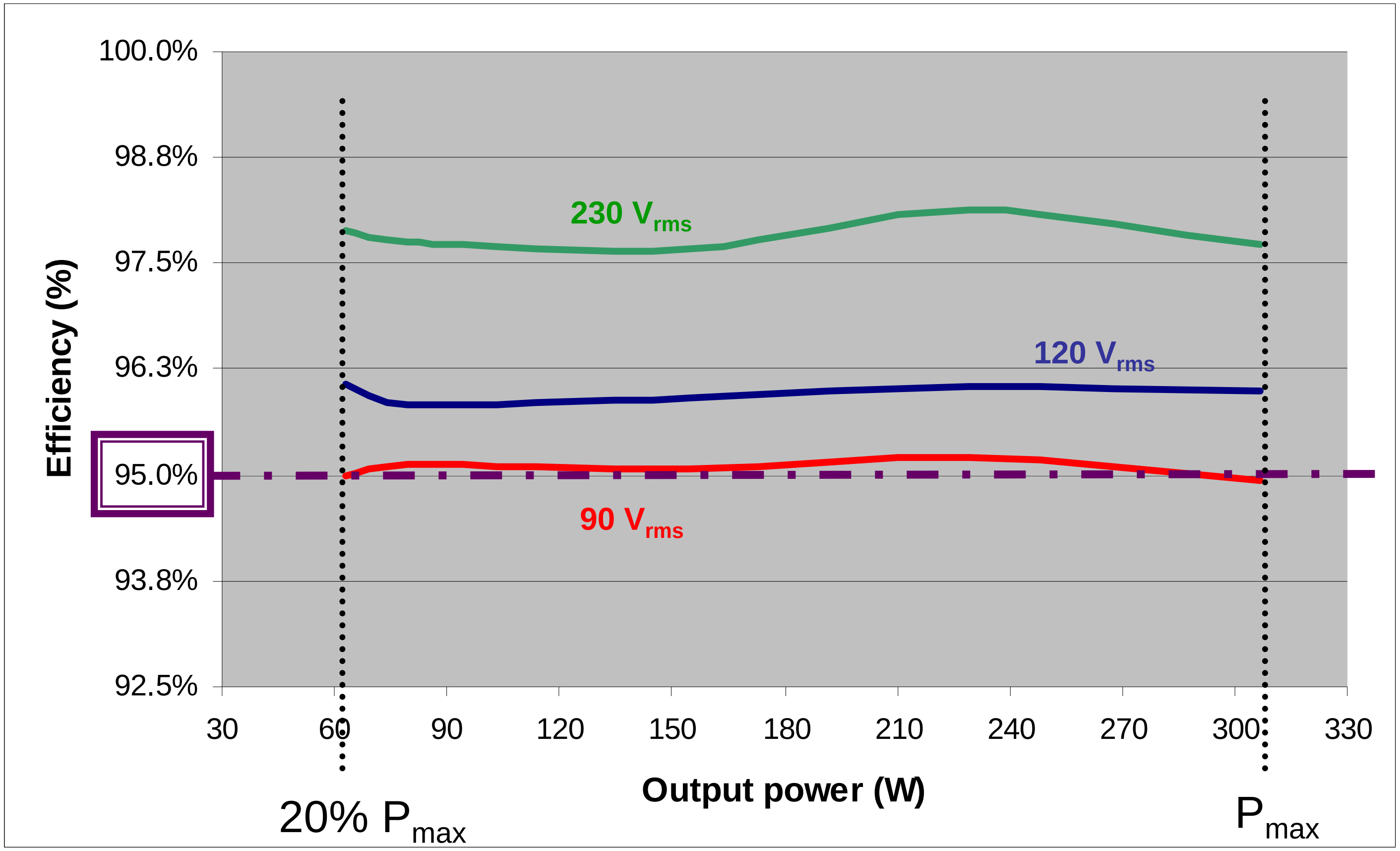
Performance Measurements

- Conditions for the measurements:
  - The measurements were made after the board was 30 mn operated full load, low line
  - All the measurements were made consecutively without interruption
  - PF, THD, $I_{in(rms)}$ were measured by a power meter PM1200
  - $V_{in(rms)}$ was measured directly at the input of the board by a HP 34401A multimeter
  - V_{out} was measured by a HP 34401A multimeter
  - The input power was computed according to:

$$P_{in(avg)} = V_{in(rms)} \cdot I_{in(rms)} \cdot PF$$

  - **Open frame, ambient temperature, no fan**

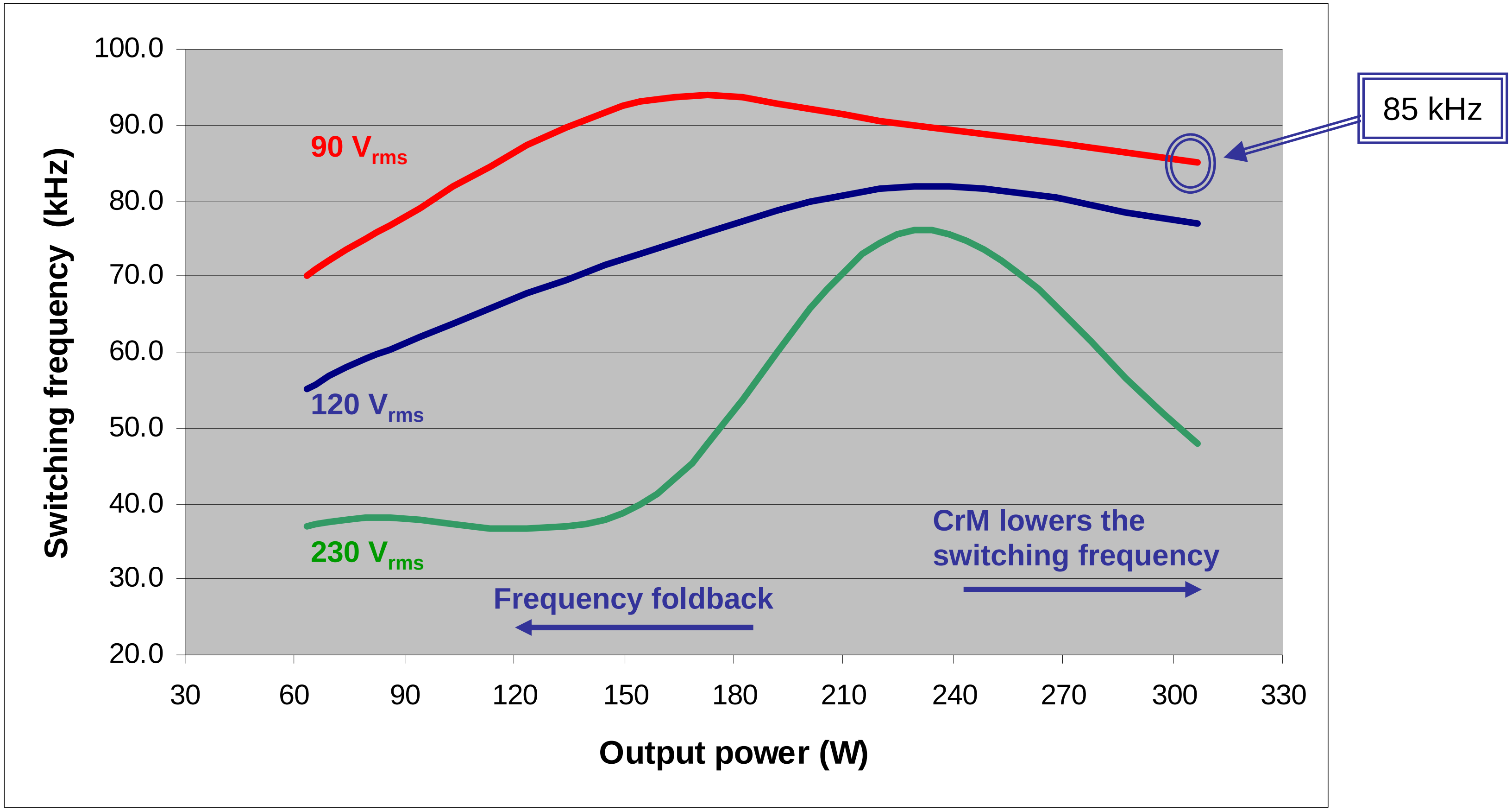
Efficiency versus Load



Results obtained in a relatively high frequency application allowing the use of small inductors: (85 kHz in each phase at 90 V_{rms}, full load, $L_1 = L_2$ =150 µH)

- ❑ The plot portrays the efficiency over the line range, from 20% to 100% of the load
- ❑ The efficiency remains higher than 95%!

Switching Frequency (at the Sinusoid Top)



- ❑ The plot portrays f_{sw} (sinusoid top) over the line range, as a function of the load
- ❑ The PFC stages operate in CrM at full load

Conclusion

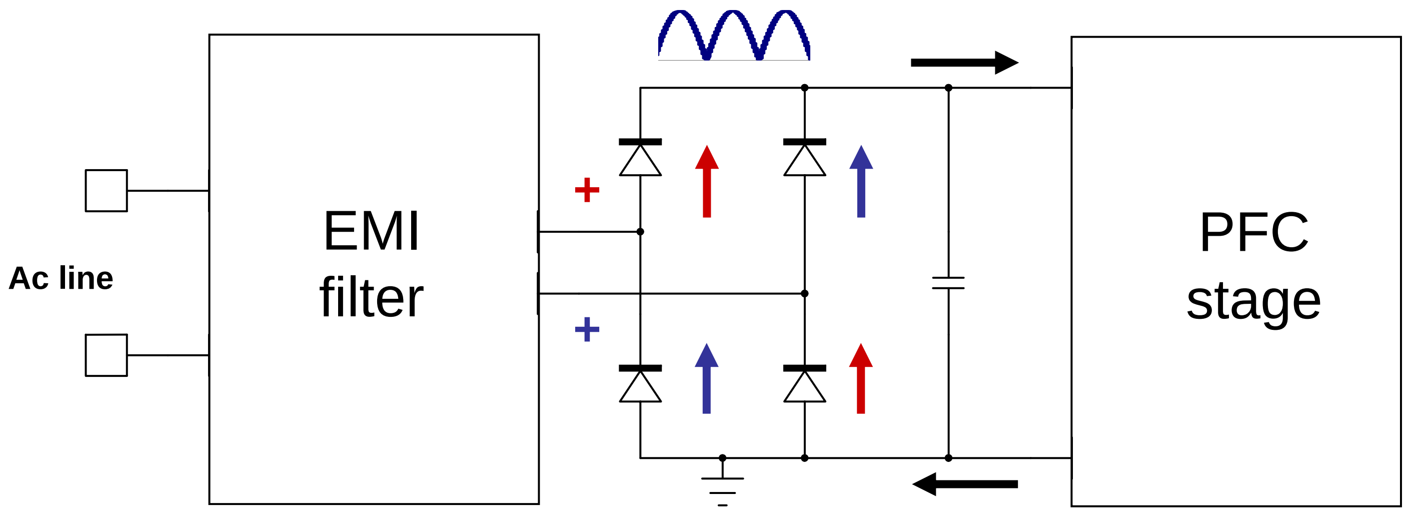
- Interleaved PFCs
  - Reduce the input current ripple
  - Lower the bulk capacitor rms current
- Two NCP1601 provide an efficient solution for interleaving
- Besides interleaving, this solution takes benefit of:
  - The FCCrM mode that optimizes the efficiency
  - MUR550 diodes optimized for DCM PFC applications
  - Frequency foldback (light load)
- The solution has been tested on a 300 W, wide mains board
- **95% efficiency at 90 V_{rms} over a large load range** (from 20% to 100% load)
- A 16-pin interleaved PFC controller is under development

Agenda

- Introduction
  - Basic solutions for power factor correction
  - New needs to address
- Interleaved PFC
  - Basic characteristics
  - A discrete solution
  - Performance
- **Bridgeless PFC**
  - **Why should we care of the input bridge?**
  - **Main solutions**
  - **Ivo Barbi solution**
  - **Performance of a wide mains, 800 W application**
- Conclusion

No bridge!

The Diodes Bridge



- The diodes bridge rectifies the ac line voltage
- Two diodes conduct simultaneously
- The PFC input current flows through two series diodes

Efficiency Loss caused by the Diodes Bridge

- Average current flowing through the input diodes:

$$\left\langle I_{bridge} \right\rangle_{T_{line}} = \left\langle I_{line}(t) \right\rangle_{T_{line}} = \frac{2\sqrt{2}}{\pi} \cdot \frac{P_{out}}{\eta \cdot V_{in(rms)}}$$

- Dissipation in the diodes bridge:

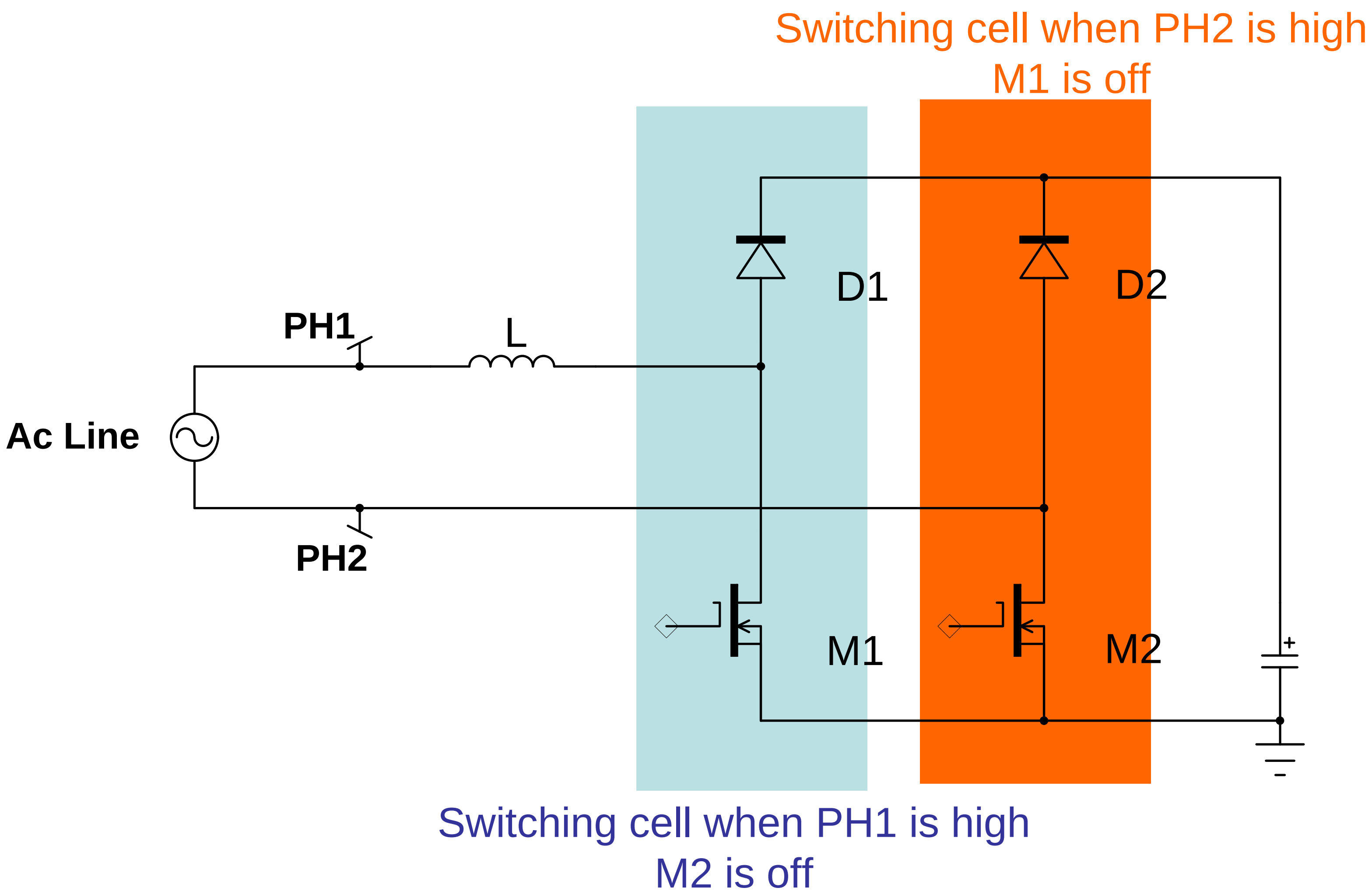
$$P_{bridge} = 2 \cdot V_f \cdot I_{bridge} \approx 2 \cdot V_f \cdot \frac{2\sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot V_{in(rms)}}$$

- If V_f = 1 V and $(V_{in(\mathrm{rms})})_{\mathrm{LL}}$ = 90 V:

$$P_{bridge} \approx 2\% \cdot \frac{P_{out}}{\eta}$$

➔ In low mains applications (@ 90 V_{rms}), the diodes bridge wastes about 2% efficiency!

Basic Bridgeless PFC

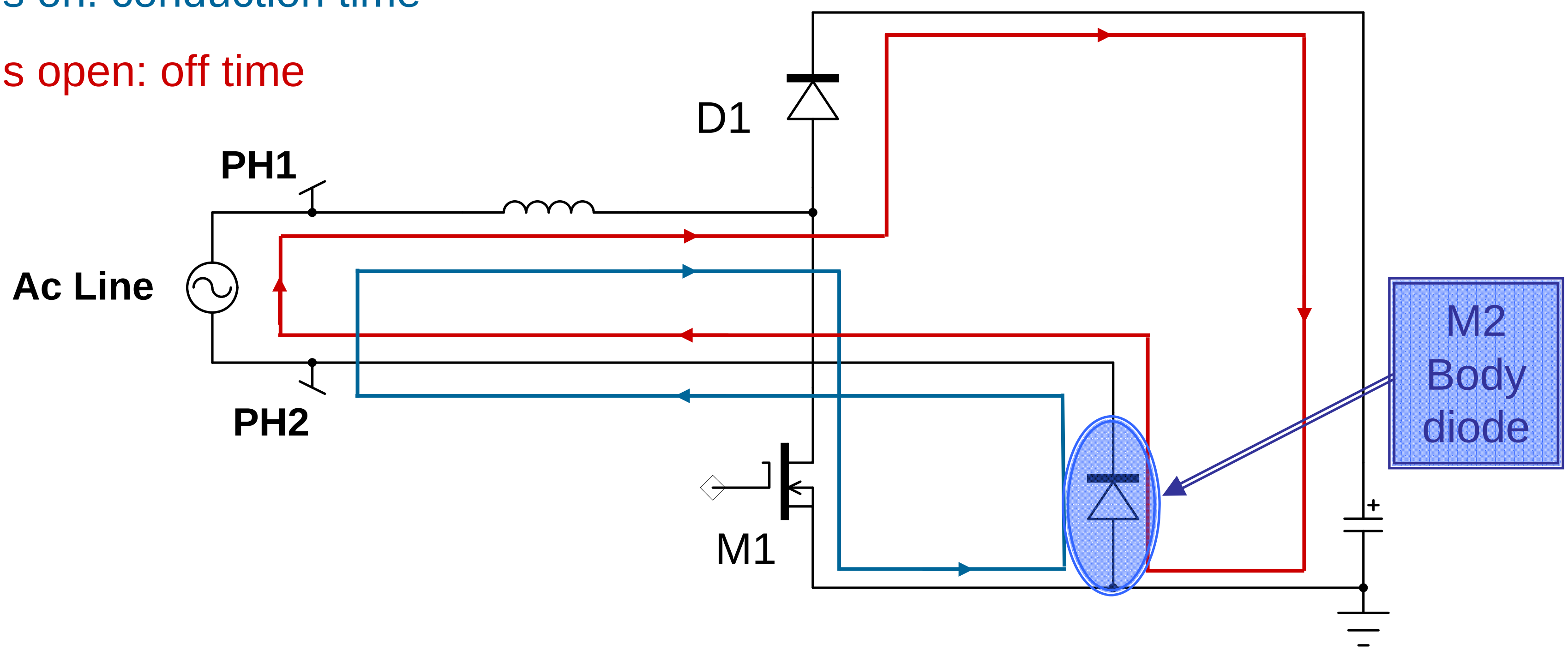


Operation with Positive Half-Wave

- ❑ PH1 is high, PH2 is low:

M1 is on: conduction time

M1 is open: off time



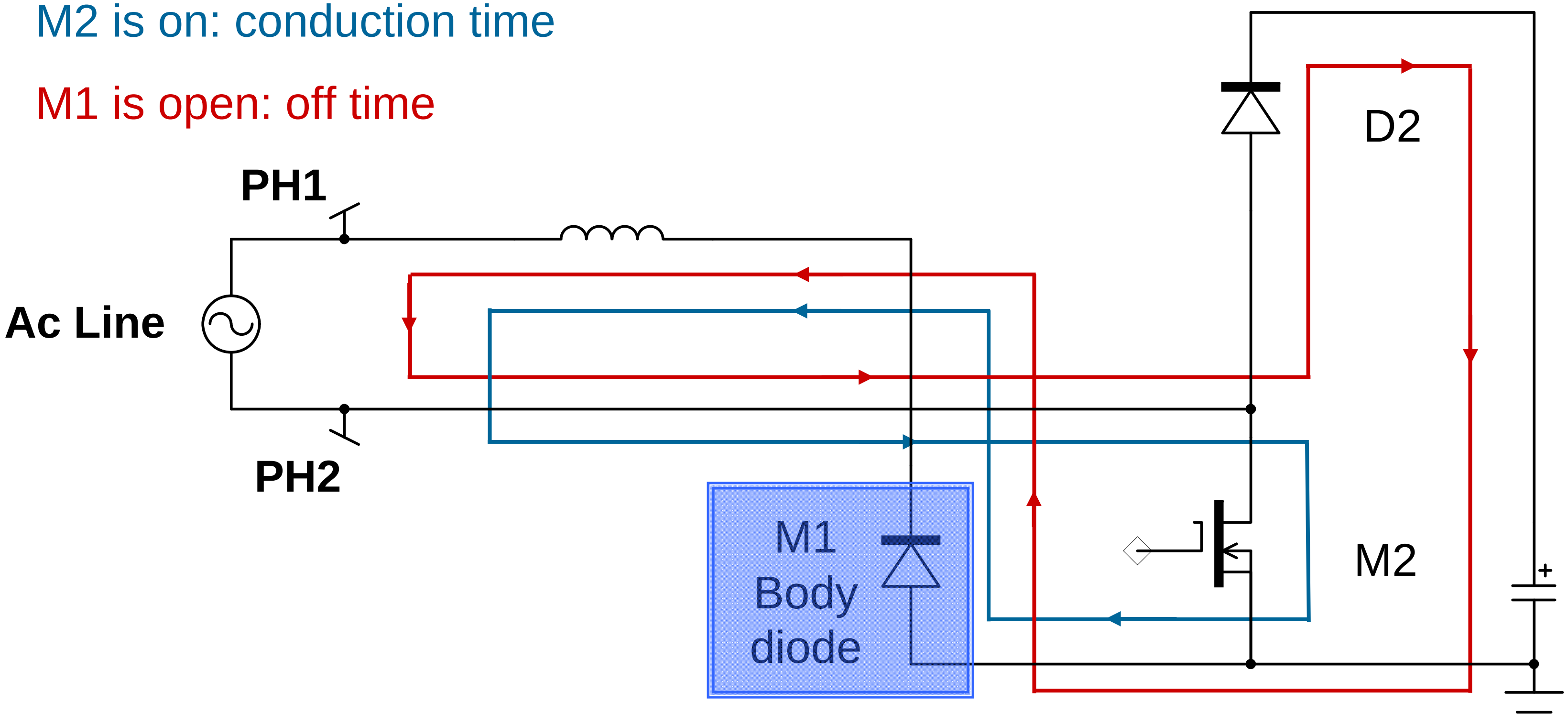
- ❑ M2 body diode grounds PH2 as would a diode bridge.

Operation with Negative Half-Wave

- ❑ PH1 is low, PH2 is high:

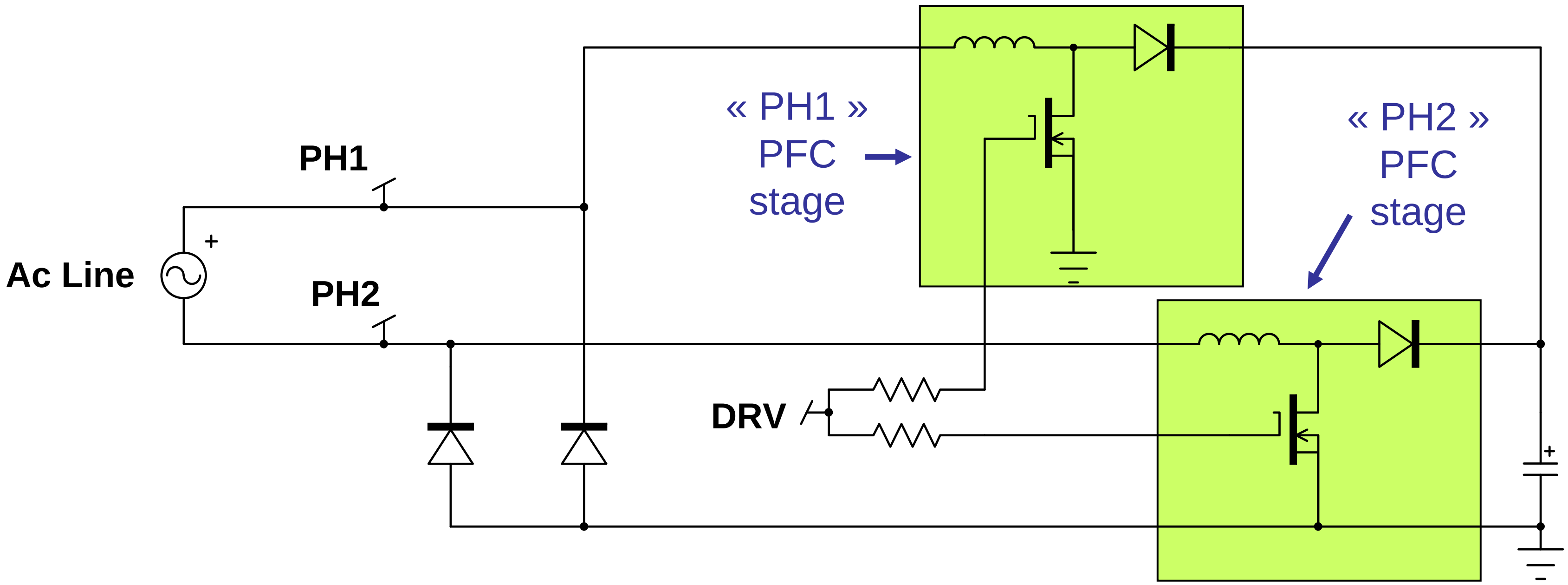
M2 is on: conduction time

M1 is open: off time



- ❑ Both line terminals are pulsating at the switching frequency
- ❑ The pulsation swing is high (V_{OUT})
- ❑ HF noise that leads to a tedious EMI filtering

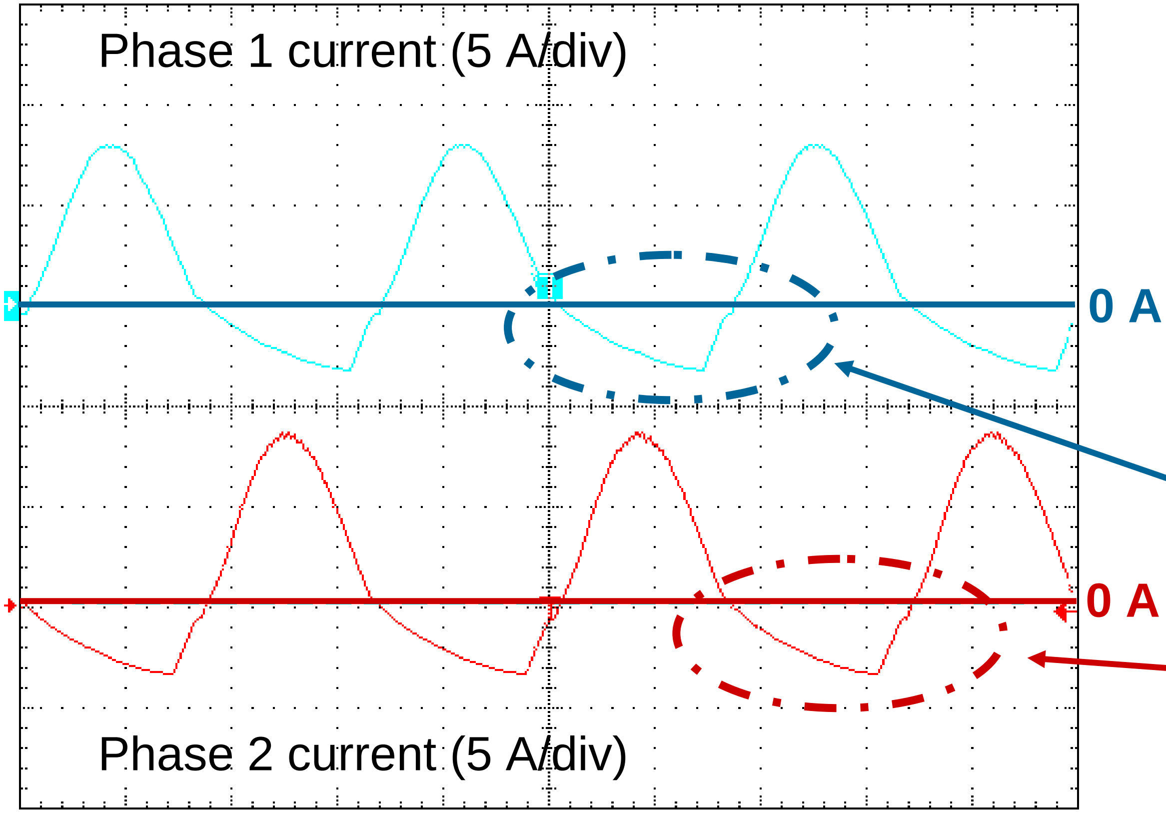
Ivo Barbi Bridgeless Boost



Two PFC stages but:

- One driver with no need for detecting the active half-wave
- Improved thermal performance
- As with convential PFC stages, the negative phase is always attached to ground. EMI issue is solved.

Current Sharing

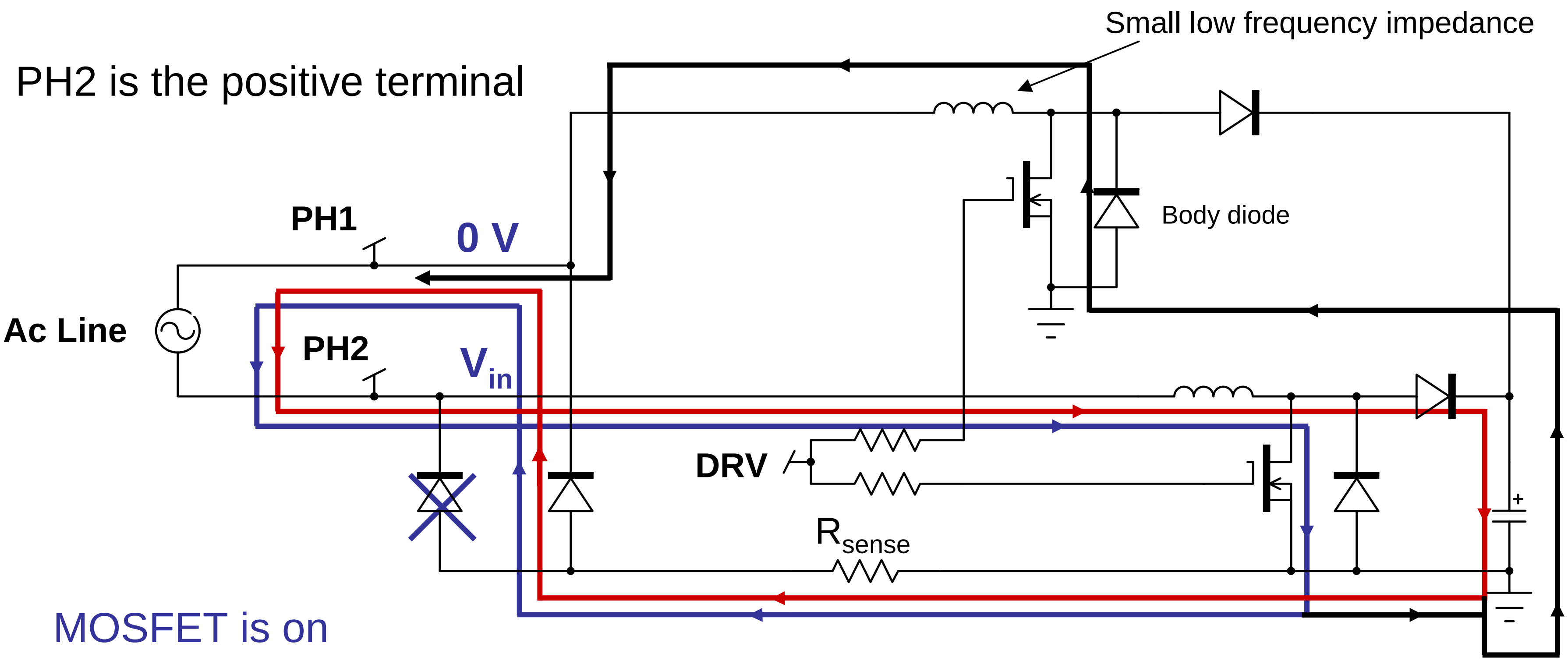


Part of the active phase current flows throught the inactive MOSFET and coil!

Part of the current flows…
… through the supposedly inactive MOSFET and coil

Two Return Paths…

PH2 is the positive terminal

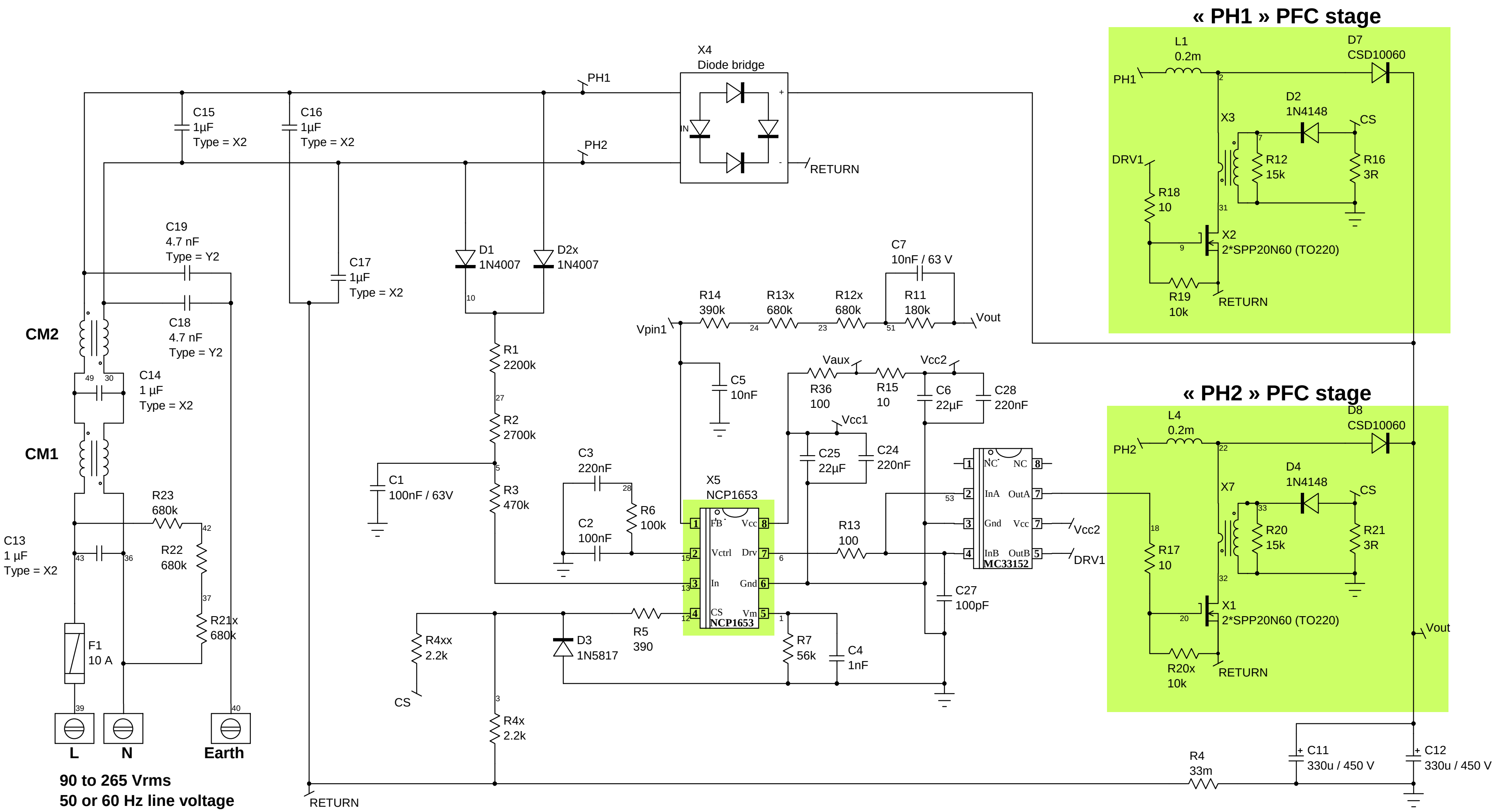


MOSFET is on

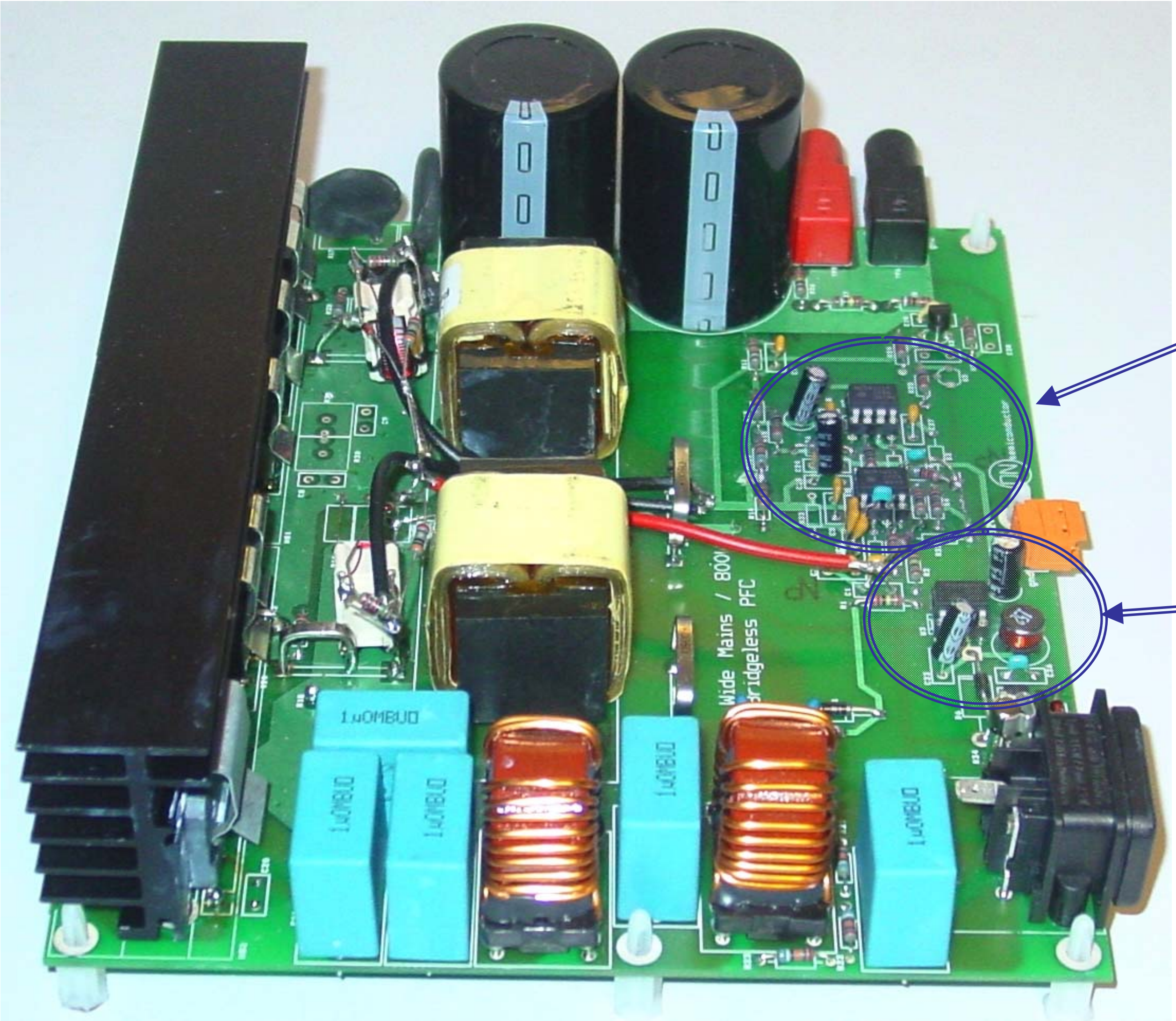
MOSFET is off

Need for current sense transformers

Schematic for 800 W Prototype



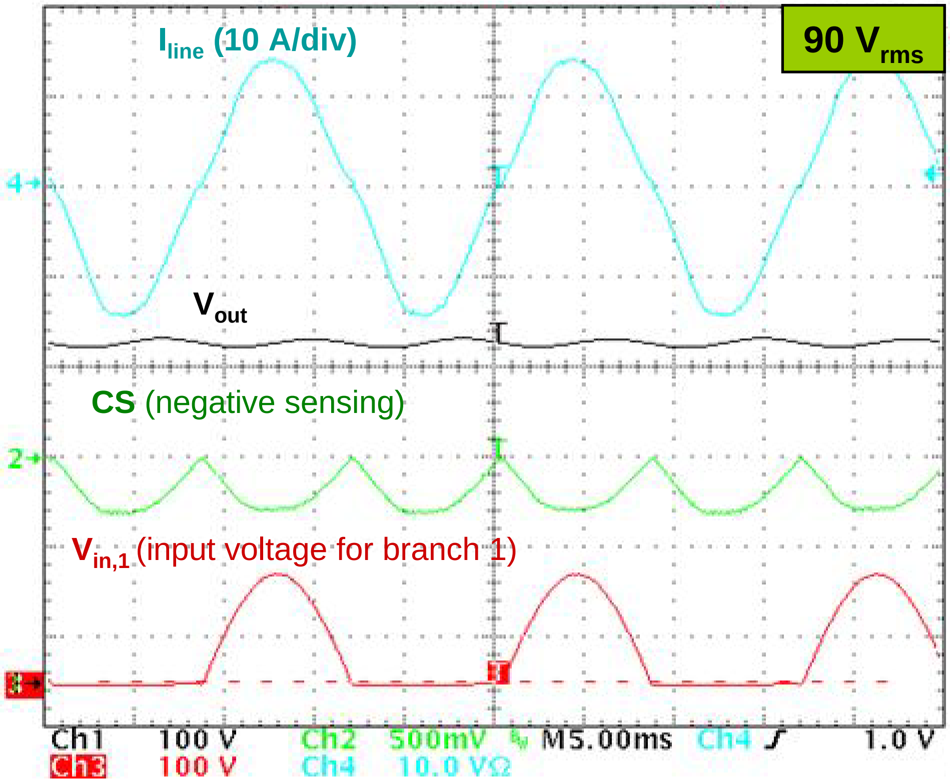
Board Photograph

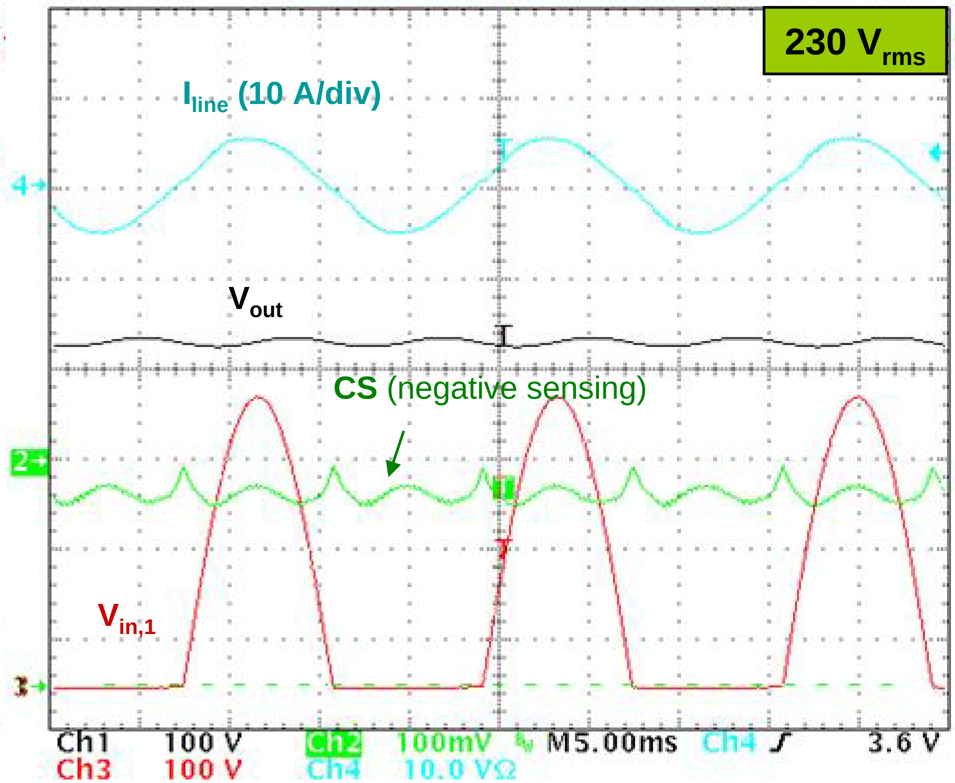


NCP1653
And
MC33152
MOSFET
driver

Bulk
converter to
generate the
V_{cc} voltage
(NCP1012)

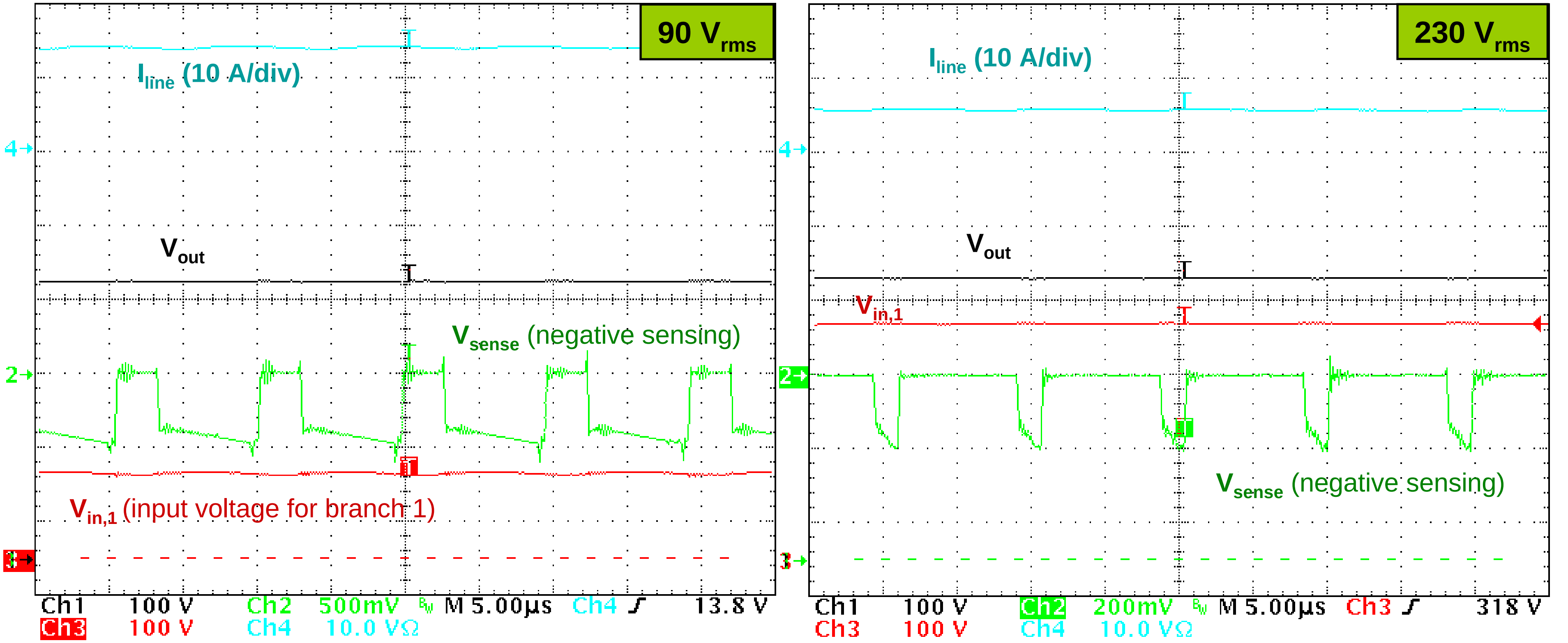
Typical Waveforms





- These plots portray typical waveforms at full load (I_{out} = 2.1 A)
- "CS" is representative of the current flowing into the MOSFETs of the two branches (common output of the current transformers)
- The input current is sinusoidal

Zoom of the Precedent Plots (Top of the Sinusoid)



- The switching frequency is 100 kHz
- The waveforms are similar to those of a traditional CCM PFC

Performance Measurements

- Conditions for the measurements:
  - The measurements were made after the board was 30 mn operated full load, low line
  - All the measurements were made consecutively without interruption
  - PF, THD, $I_{in(rms)}$ were measured by a power meter PM1200
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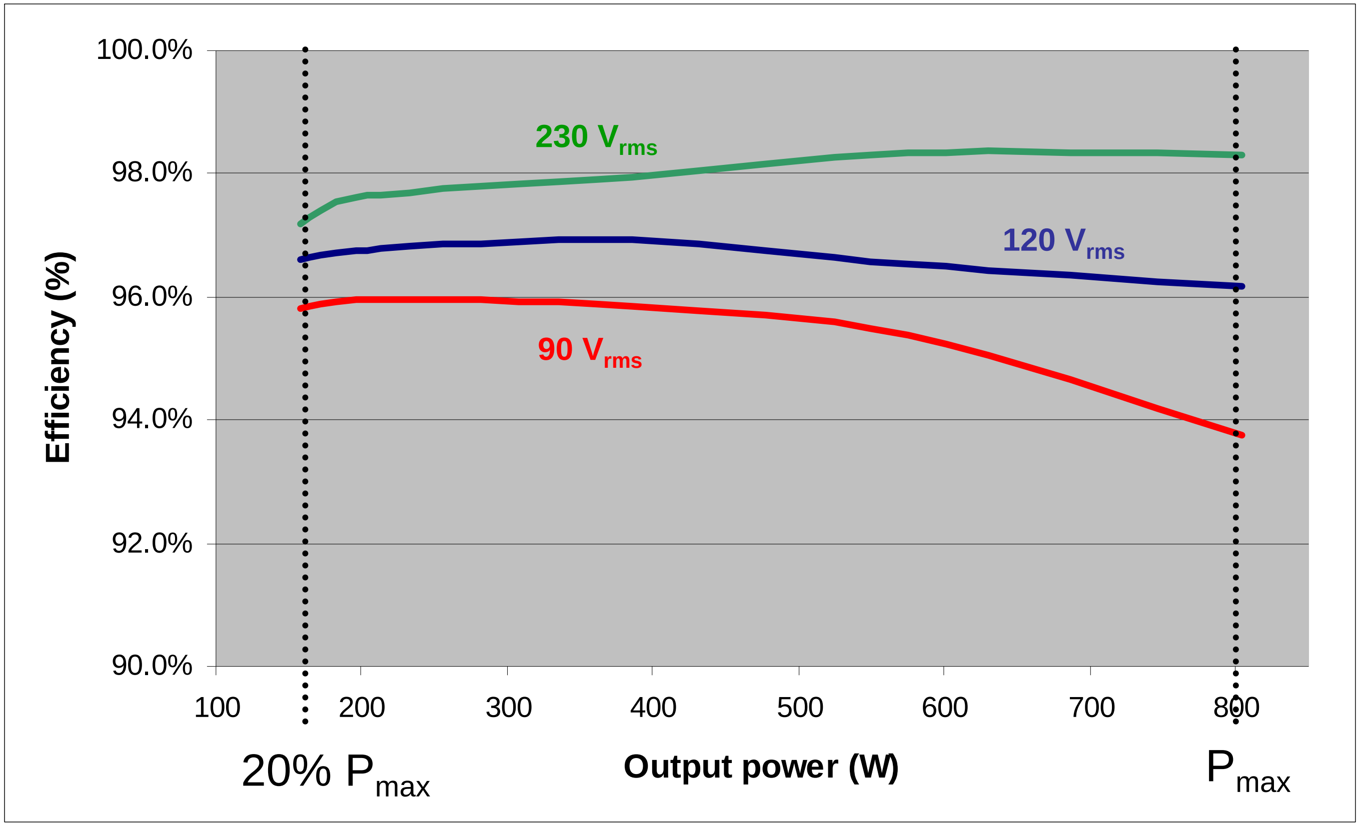
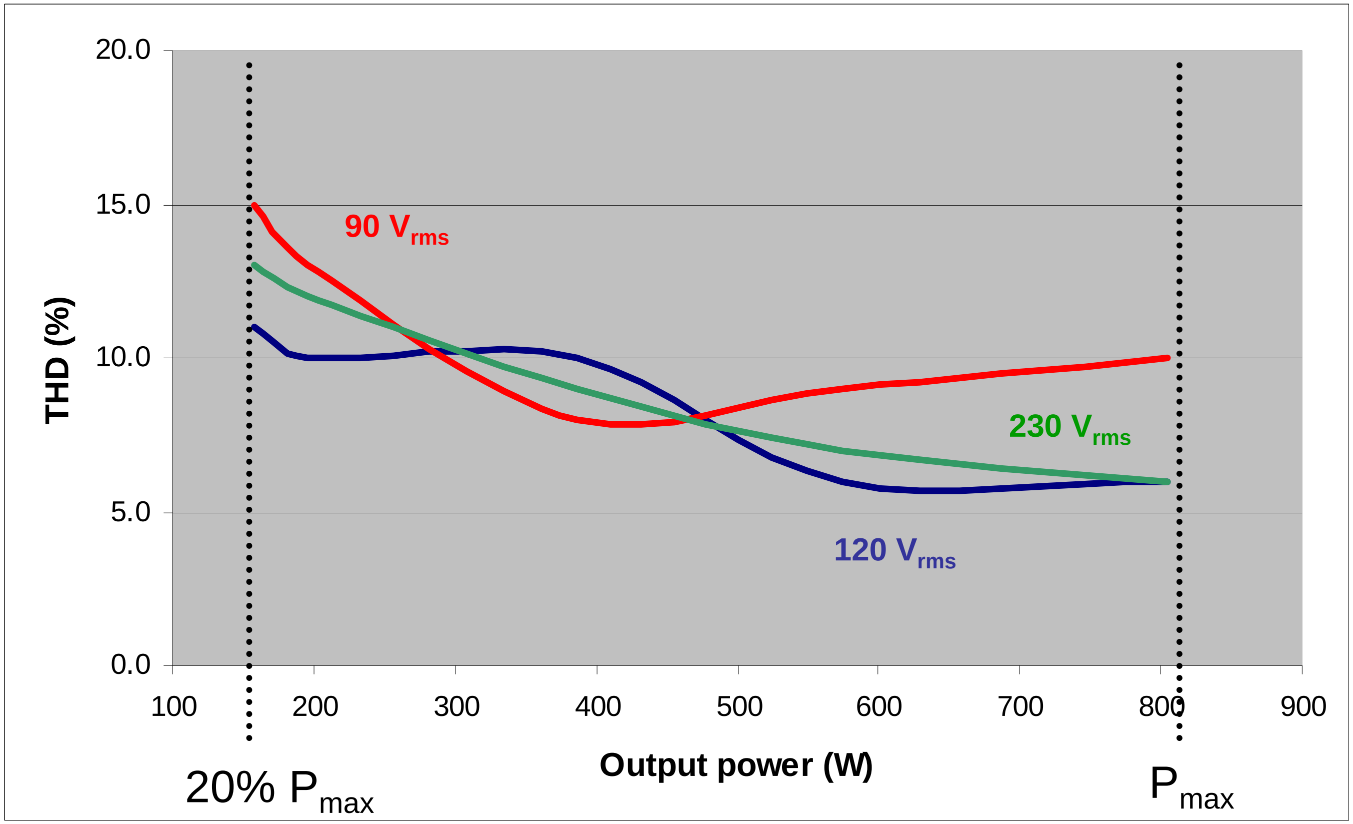
Efficiency versus Load



- The plot portrays the efficiency from 20% to 100% of the load
- At 90 V_{rms}, full load, it is about 94% <u>without fan</u> (95% at 100 V_{rms})
- At 20% of full load, efficiency is in the range or higher than 96%

THD versus Load



- THD remains very low on the whole range

Conclusion

- A bridgeless PFC controlled by the NCP1653 has been developed (100 kHz)
- The prototype was tested at full load (800 W output) without fan (open frame, ambient temperature)
- In these conditions, the efficiency was measured in the range of 94% at 90 V_{rms} and 95% at 100 V_{rms}
- The THD remains very low
- Bridgeless can be an efficient solution for high power applications.
- An application note is being prepared and should be posted in Q4 this year.

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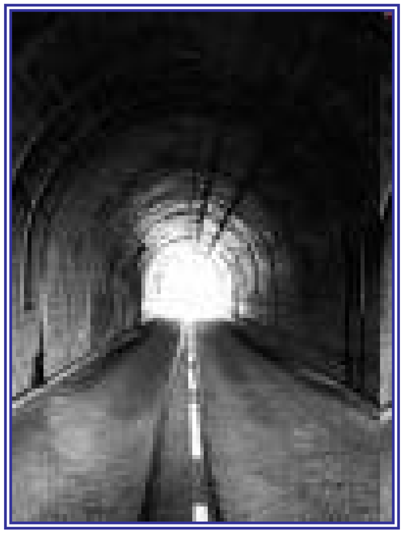

Conclusion

- New requirements:
  - Compactness and form factor (LCD TV)
  - Efficiency (ATX power supplies)
- New solutions can address them
- Interleaved PFC brings:
  - Efficiency
  - Flat design
  - Improved heat distribution
  - Reduced rms current through the PFC stage
  - Modular approach
- Bridgeless PFC:
  - halves the losses in the input rectification
  - Improves the heat distribution
- ON Semiconductor supports these innovative approaches

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com

- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies