TND313/D
Rev 3, Sep-11

High-Efficiency
305 W ATX Reference Design
Documentation Package

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Table of Contents

List of Tables

List of Figures

1. Overview

ON Semiconductor was the first Semiconductor company to provide an 80 PLUS open reference design for an ATX Power Supply in 2005. This 1st generation reference design, was certified and met all the requirements of the 80 PLUS program. Following on this successful 1st generation design, ON Semiconductor is introducing its improved 2nd Generation reference design. This 2nd generation design utilizes newer ICs from ON Semiconductor that enable this design to exceed 80% efficiency starting at 20% load across different line conditions with ample margin to spare.

This reference document provides the details behind this 2nd generation design. The design manual provides a detailed view of the performance achieved with this design in terms of efficiency, performance, thermals and other key parameters. In addition, a detailed list of the bill-of-materials (BOM) is also provided. ON Semiconductor will also be able to provide technical support to help our customers design and manufacture a similar ATX power supply customized to meet their specific requirements.

The results achieved in this 2nd generation design were possible due to the use of advanced new components from ON Semiconductor. These new ICs not only speeded up the overall development cycle for this new design, but also helped achieve the high efficiencies while at the same time keeping a check on the overall cost. With the use of these new ICs, ON Semiconductor has proven again that the emerging requirements for high efficiency desktop power supplies can be met and further, can be optimized to meet specific performance vs. cost goals.

This 2nd generation design consists of a single PCB designed to fit into the standard ATX enclosure along with a fan. Figure 1 below presents the overall architecture employed in this design – detailed schematics are included later in this design manual. As seen in figure 1, this design employed an Active Clamp forward topology using the new, highly integrated Active Clamp Controller IC from ON Semiconductor – NCP1562. A Continuous Conduction Mode (CCM) Power Factor Correction (PFC) IC was employed for the active PFC circuit. This IC, the NCP1653 provides an integrated, robust and cost-effective PFC solution. The standby controller, NCP1027, is an optimized IC for the ATX power supply and incorporates a high-voltage MOSFET. On the secondary side, this architecture employs a post regulator approach for generating the 3.3 V output. This is an alternative approach to the traditional magnetic amplifier (Mag Amp) approach. Though ON Semiconductor believes that this post regulator approach provides the highest efficiency amongst the different means of generating these outputs in the power supply, it is important to note that if the customer desires to use a different approach, that is possible – i.e. a similar design can be developed that utilizes all the other pieces of this architecture without the post regulator and still achieve very good results.

With the introduction of this 2nd generation, high-efficiency ATX Power Supply, ON Semiconductor has shown that with judicious choice of design tradeoffs, optimum performance is achieved at minimum cost.

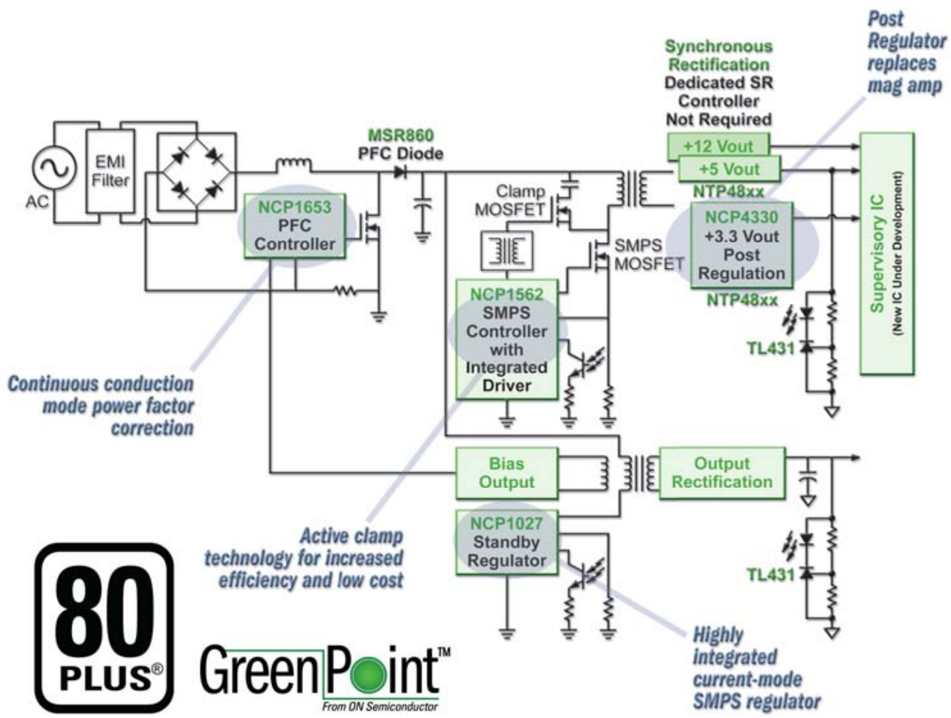


Figure 1: Reference Design Architecture Block Diagram

2. Specifications

The design closely follows the ATX12V version 2.2 power supply guidelines and specifications available from www.formfactors.org, unless otherwise noted. For instance, our reference design had a target of +/- 5% tolerance for both the 5 V and 5 Vstandby outputs. Further, the efficiency targets for the 80 PLUS program and the EPA's Energy Star specification – Energy Star Program Requirements for Computers, version 4.0 that is set to take effect from July 20, 2007 – were targeted. Key specifications are included in **Table 1** below.

Output	**Current**		**Tolerance (%)**	**Ripple/Noise (mV)**
	Min. (A)	**Max (A)**		
5 V	0.3	22	± 3.3	50
5 V standby	0.0	2.5	± 3.3	50
12 V	1.0	18	± 5.0	120
- 12 V	0.0	1	± 10	120

Table 1: Target Specifications

Target specifications for other key parameters of the reference design include:

- Efficiency: Minimum efficiency of 80% for 20%, 50% and 100% of rated output load conditions as defined by the 80 PLUS requirements as well as the Energy Star specification.
- Power Factor: Power factor of 0.9 or greater at 100 % load.
- Input Voltage: Universal Mains – 90 Vac to 265 Vac, 47 – 63 M Hz.
- Output Power: Total maximum output power is 305 W.
- Safety Features: As per the ATX12V specification, this design includes safety features such as OVP, UVP, and OCP.
- This design meets the IEC1000-3-2 requirements over the input line range and under full load conditions.
- This converter was designed for a 20 ms minimum Hold-up time.
- Physical dimensions: This converter is designed to fit into the standard ATX enclosure with dimensions of 150 mm x 140 mm x 86 mm.

3. Architecture Overview

Before discussing the power supply architecture of the Generation 2 design, it is worth reiterating the design goals. We are tasked with providing a flexible power platform, which is required to have the lowest cost and highest efficiency that can be packaged in a small volume. The architecture must deliver a minimum of 80% efficiency over a wide range of operating conditions (high-line and low-line) as well as rated output load conditions (20% load and above). In addition we require a robust design solution having low parts count to provide the same performance on a unit to unit basis in a high volume manufacturing environment.

The architecture selected follows a traditional two stage conversion approach as illustrated in Figure 1. It is worth noting that in order to achieve 80% efficiency overall, the efficiency of each of the two conversion stages must exceed 90 %. The front-end is a universal input, active power factor boost stage delivering a constant output voltage of 385 V to the active clamp stage. The second stage consists of two, dc-dc converters. The first down-stream converter processes 290 W required by the system in the form of tightly regulated +/-12 V, +5 V and +3.3 V outputs. The second converter delivers 15 W of standby power to another isolated 5 V rail.

ON Semiconductor has developed multiple power management controllers and MOSFET devices in support of the ATX program. Web based data sheets, design tools and technical resources are available to assist design optimization. The ICs, supporting the ATX Generation 2 platform, are the NCP1653 PFC controller, the NCP1562 active clamp controller, the NCP4330 post regulator, the NCP1027 standby controller, and the NTP48xx family of MOSFET synchronous rectifiers. It is not possible to discuss the tradeoffs involved in each conversion stage at length, but the selection of the active clamp forward converter topology is a key one and will be covered in depth. Each controller is highly integrated and offers the lowest external parts count available.

PFC Stage

There are a variety of PFC topologies available. These include discontinuous conduction mode (DCM), critical conduction mode (CRM) and continuous conduction mode (CCM). At this power level, CCM is the preferred choice and the NCP1653 will implement a IEC1000-3-2 compliant, fixed frequency, peak current mode PFC boost converter with very few external components.

DC to DC (Main) Converter

The selection of the dc-dc down stream converter is at the heart of the 80% solution. The traditional work horse of the ATX market has been the single switch forward converter operating at a switching frequency of 100 kHz. The converter and its associated drain waveform are illustrated in Figure 2. This topology is robust and delivers good full load efficiency performance at minimal cost. However, as power levels increase and regulatory requirements and energy conservation agencies drive for higher efficiency under all load conditions, the single switch forward topology in its simplest form is reaching its limit.

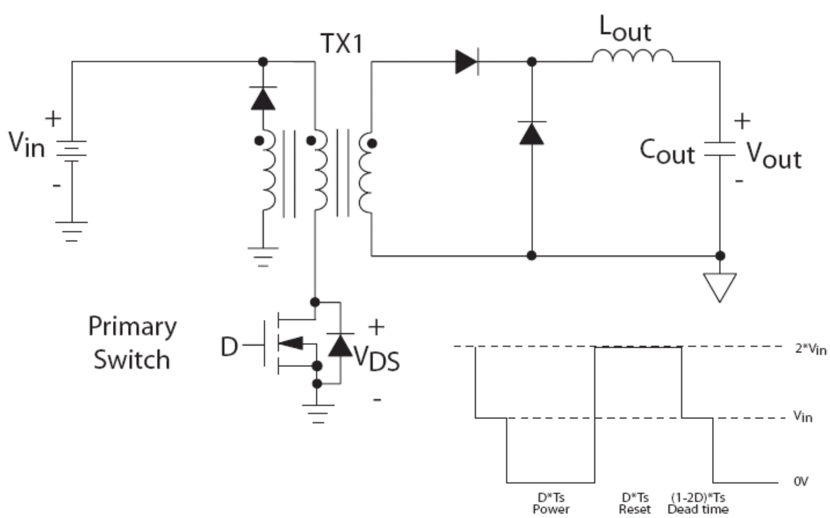


Figure 2: One switch forward topology and associated waveform

There are several technical reasons for this. First, because the main transformer is reset via an auxiliary winding across the input bus, the duty cycle is limited below 50%. Second, because of this reset mechanism there is always a dead time interval, during each converter cycle, when no power is flowing. These two constraints have negative implications on the silicon utilization of the primary switch requiring a costly, large area die to be selected. The primary switch's conduction loss is given by (1)

$$P_{loss(conduction)} = D * I_P{}^2 * R_{DS(on)} \tag{1}$$

where, D is the duty cycle, I_P is the primary current and $R_{DS(on)}$ is the switch on resistance. The topology is a hard switched topology with the primary switch being driven on with 385 V across it each switching cycle. The capacitive switch loss are given by (2),

$$P_{loss(capacitive)} = \frac{1}{2} C_{OSS} * V_{DS}{}^2 * f \tag{2}$$

where, C_{OSS} is the switch output capacitance, V_{DS} is the drain to source voltage and f is the operating frequency. Capacitive losses dominate at light load. Hence a switch selected for full load performance will suffer at light load because of its large drain source capacitance. Reviewing these two loss equations, it becomes apparent for efficiency enhancement under both full load and light load operation, a topology is required that allows the primary switch to operate at lower current and voltage stress. As the loss terms appear as current and voltage squared, small reductions in primary current I_P and switch voltage V_{DS} significantly improve performance.

The active clamp forward converter illustrated in Figure 3 represents the ultimate extension of the single switch converter and provides these benefits. Instead of using an auxiliary winding, transformer reset is achieved using a clamp capacitor and an auxiliary switch. The reset period, controlled by the auxiliary switch now extends to the interval $(1-D)*T_S$, completely eliminating the previous dead time interval. To maintain flux balance in the main transformer core, the reset voltage across the clamp capacitor is determined by the expression $\frac{V_{in} * D}{(1-D)}$. The duty cycle D of the single switch forward converter can extend beyond 50%, limited only by the primary switch's maximum voltage rating.

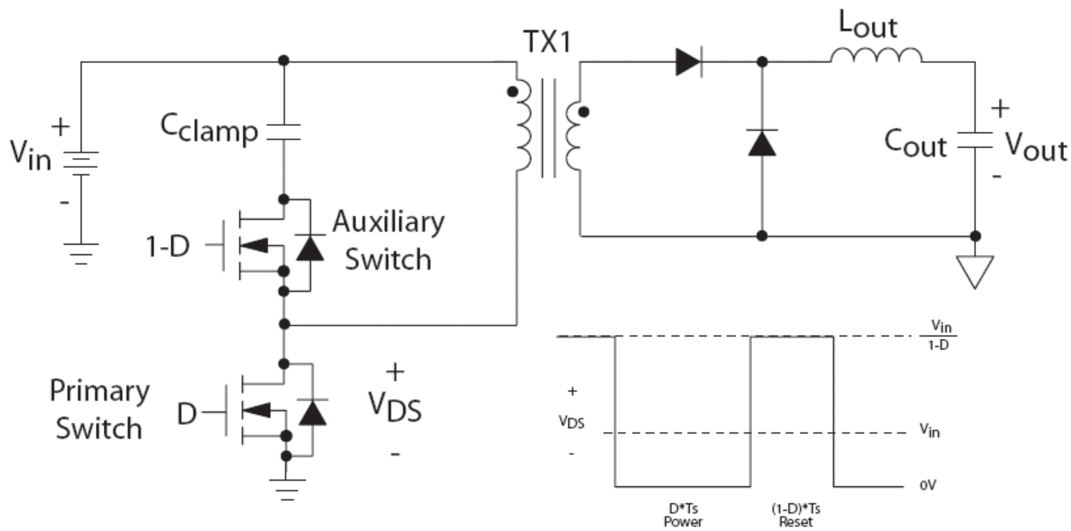


Figure 3: Active clamp forward topology and associated waveform

For a given set of conditions and power throughput, operating at extended duty cycles allows for a lower primary current. This in turn allows the selection of a smaller, lower cost die. Let's look at a design example to illustrate this point.

To reduce cost, a 150 µF bulk capacitor (instead of a 470 µF conventional value) is selected to provide 20 ms of hold up time. Using the energy storage equation given by (3),

$$Energy = \frac{1}{2} C * \left(V_i^2 - V_f^{\,2}\right) = \frac{Power\,Delivered * Hold\ up\ time}{\eta} \qquad (3)$$

where, V_i and V_f are the initial and final voltages of the input capacitor, respectively. The initial voltage is 385 V and converter efficiency is 90%, allows us to calculate the final voltage V_f to be 250 V. In the case of a conventional single switch design, the maximum duty cycle we can practically select and avoid transformer saturation is 0.45. The switch voltage stress is 2 x 250 V. With the active clamp single switch forward, the duty cycle can be extended to 0.67 and the voltage stress on the switch is Vin / (1-D) or 3.03 x 250 V. Each converter has to process 290 / 0.9 or 322 W from the primary bulk source. At nominal 385 V bulk, the average primary current is 0.84 A. Factoring in the primary switch duty cycle D, the peak current I_P in the traditional forward converter is 0.65 / 0.45 or 1.44 times larger than the active clamp approach. Based on the conduction loss equation given by (1), we see that the 1.44 ratio holds true for conduction loss in the primary switch. Put another way, we can choose a MOSFET with 44% higher $R_{DS(on)}$ in the active clamp topology and have the same conduction loss. This is significant, as we can achieve better silicon utilization, lower cost and lower drain capacitance. By reviewing the data sheets from high voltage MOSFET vendors, it is possible to compare output capacitance C_{OSS} versus $R_{DS(on)}$ as a function of die size. For example as MOSFET resistance increases from 3.6 Ω to 4.8 Ω, the output capacitance reduces from

100 pF to 70 pF. The resonant nature of the active clamp allows the switch be turned on at 300 V instead of the conventional 400 V. These two effects allow a reduction in capacitive switching loss of 39% over a conventional design. Again, a significant improvement remembering that light load efficiency is determined predominately by switching loss. The example above illustrates how small changes in switch stress can impact overall cost and performance.

The same argument relating to increased duty cycle operation extends to the secondary by proportionally reducing output rectifier loss. Since the secondary loss is a dominant factor at full load, an additional efficiency improvement/ cost benefit is realized. To achieve the ultimate efficiency, synchronous rectification is required on the +12 V and +5 V outputs. The single switch active clamp forward is very suitable to drive synchronous rectifiers directly from the secondary windings without the need for expensive gate drivers or additional delay timing circuitry.

To allow designers to capitalize on the benefits inherent in the active clamp topology, the NCP1562 has been developed to capture all the necessary control features within a 16 pin package. The full featured controller has been designed for tight tolerance on all parameters, including the maximum duty cycle limit and the important soft stop function.

To boost efficiency and maintain tight regulation, instead of the conventional magnetic amplifier post regulated approach, the 3.3 V output is derived from the 5 Volt winding of the main transformer. The MOSFET drivers, timing, synchronization and control functions to support this output are provided by the NCP4330 controller. A 6 W improvement in the loss budget is achieved when this approach is adopted. Gate charge and $R_{DS(on)}$ have been optimized in the NTP48xx family of MOSFETs and provide synchronous rectification for both the 3.3 V and 5 V outputs.

Standby Power

The NCP1027 integrates a fixed frequency current mode controller and a 700 volt MOSFET. The NCP1027 is an ideal part to implement a flyback topology delivering 15 W to an isolated 5 V output. At light loads the IC will operate in skip cycle mode, thereby reducing its switching losses and delivering high efficiency throughout the load range.

4. Performance Results

The evaluation of the reference design focused on several areas including efficiency, power factor, cross regulation and transient load response. Design optimizations may be needed to customize this reference design to meet specific requirements.

The converter efficiency is measured according to the operating conditions detailed in Table 2. The converter efficiency is measured at 100 Vac, 115 Vac and 230 Vac at 50 Hz. The converter achieves over 80% efficiency with room to spare over all load conditions as shown in Figure 4. The output voltages used for the efficiency calculations are measured at the end of the power cables. The fan is disabled for measurements at or below 20% load. The fan is automatically enabled once the load exceeds 60 W or 20%. The fan is operational for 50% and 100% load measurements. Further increases in the efficiency can be obtained for 50% and 100% load conditions through fan speed control.

Load Condition	**Output Current (A)**					
	5 V	3.3 V	12 V1	12 V2	-12V	5 V SBY
5 %	0.690	0.540	0.385	0.385	0.030	0.070
10 %	1.390	1.070	0.770	0.770	0.070	1.390
15 %	2.080	1.610	1.150	1.150	0.100	0.210
20 %	2.780	2.150	1.510	1.510	0.140	0.280
50 %	6.950	5.370	3.845	3.845	0.350	0.700
100 %	13.900	10.740	7.695	7.695	0.700	1.400

Table 2: Load matrix for efficiency measurements

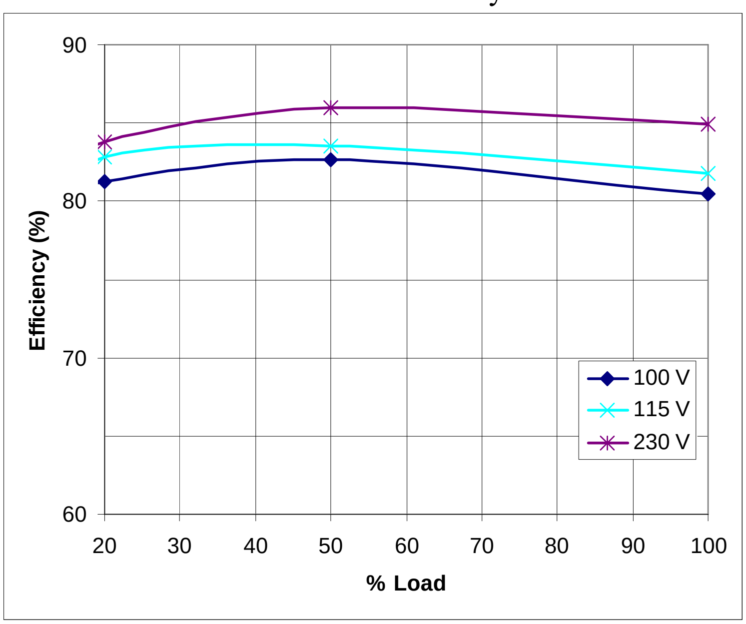


Figure 4: Efficiency vs percentage load from 20% to full load

The power factor exceeds 0.9 over all operating conditions as shown in Figure 5.

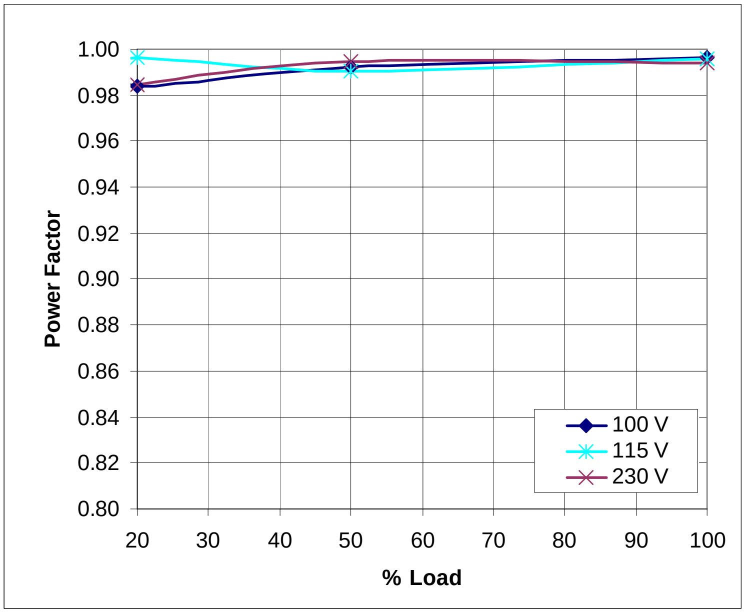


Figure 5: Power factor vs percentage load

In Figure 6, the efficiency measurements are shown from 5% load to full-load. Note that neither the 80 PLUS program nor the Energy Star specification require efficiencies above 80% for any output load below 20%. However, as can be seen in Figure 6, this reference design achieved 80% efficiency down to 16 % load.

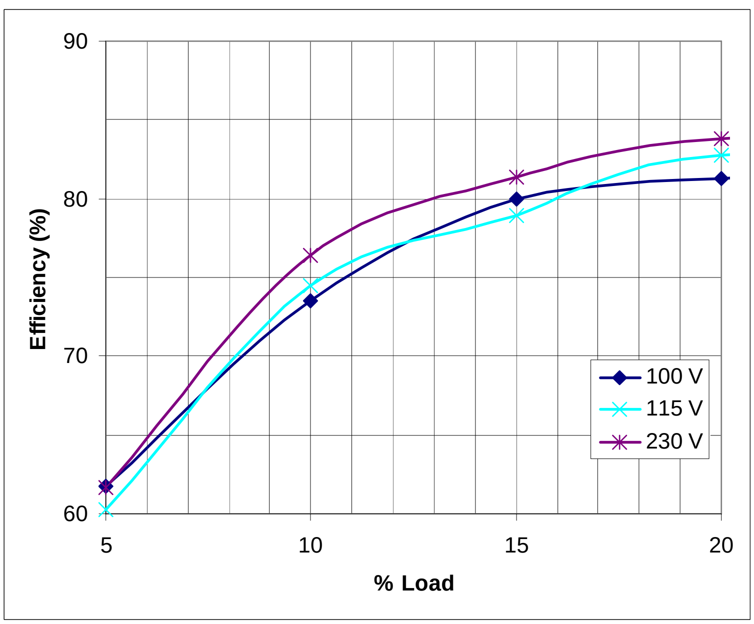


Figure 6: Efficiency vs percentage load from 5% to full load

Output voltage cross regulation is measured according to the load conditions listed in Table 3. The results of the cross regulation measurements are shown in
Figure 7 through Figure 10. Included in these figures are the tolerance requirements based on the target specifications listed in Table **1**. The margin for the 5 V and 5 V SBY outputs can be increased by shifting up the regulation target for the 5 V outputs. It can also be improved by changing the weight of the 12 V and 5 V outputs in the regulation circuit.

Load Condition	**Output Current (A)**					
	5 V (+/-3.3%)	3.3 V (+/-4%)	12 V1 (+/-5%)	12 V2 (+/-5%)	-12 V (+/-10%)	5 V SBY (+/-3.3%)
1	0.3	0.3	0	0	0	0
2	7	3	2	2	0.1	0.5
3	0.3	0.3	0	0	0	0.5
4	0.3	3	2	2	0.1	0.5
5	7	0.3	2	2	0.1	0.5
6	4	0.3	1	1	0.2	0.2
7	18	12	5	5	1	2.5
8	18	12	1	1	0.2	2.5
9	4	12	5	5	1	2.5
10	18	0.3	5	5	1	2.5
11	4	0.2	1	1	0.2	0.2
12	14	17	8	6	1	2.5
13	18	17	1	1	0.2	2.5
14	4	17	8	6	1	2.5
15	18	0.3	8	6	1	2.5
16	4	2	5	5	0.2	1
17	22	17	5	5	1	2.5
18	4	17	5	5	1	2.5
19	22	2	5	5	1	2.5

Table 3: Load matrix for cross regulation measurements

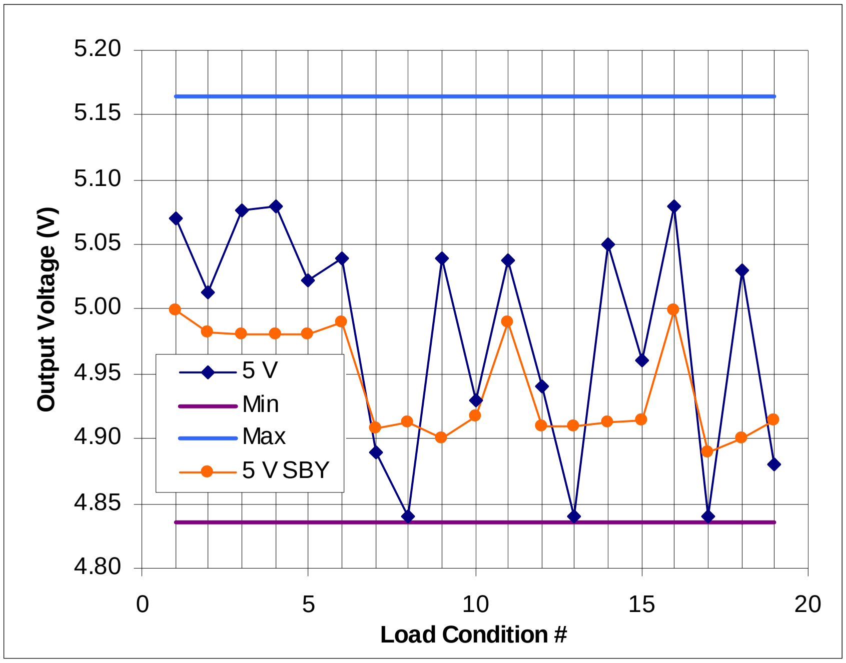


Figure 7: 5 V and 5 V SBY outputs cross regulation vs load conditions

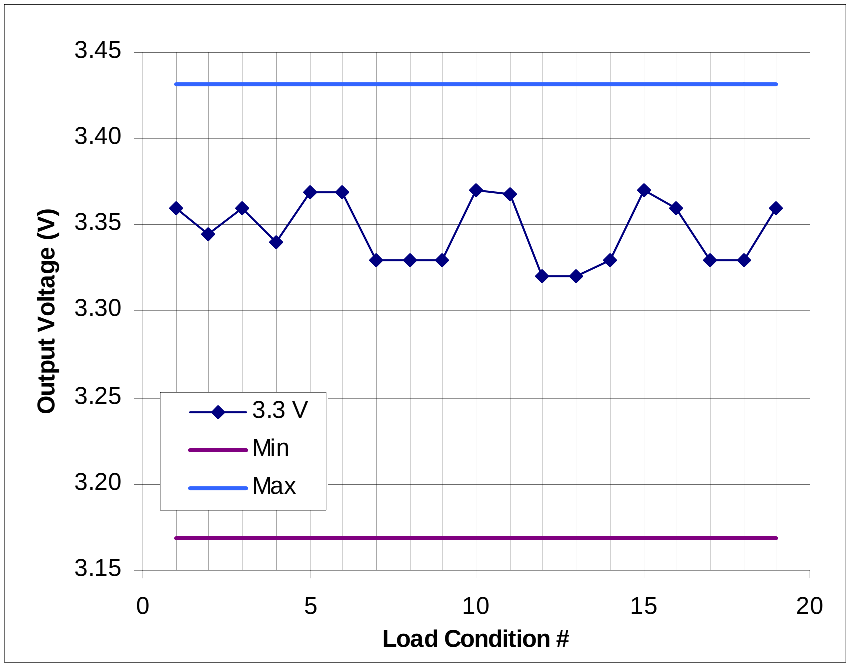


Figure 8: 3.3 V output cross regulation vs load conditions

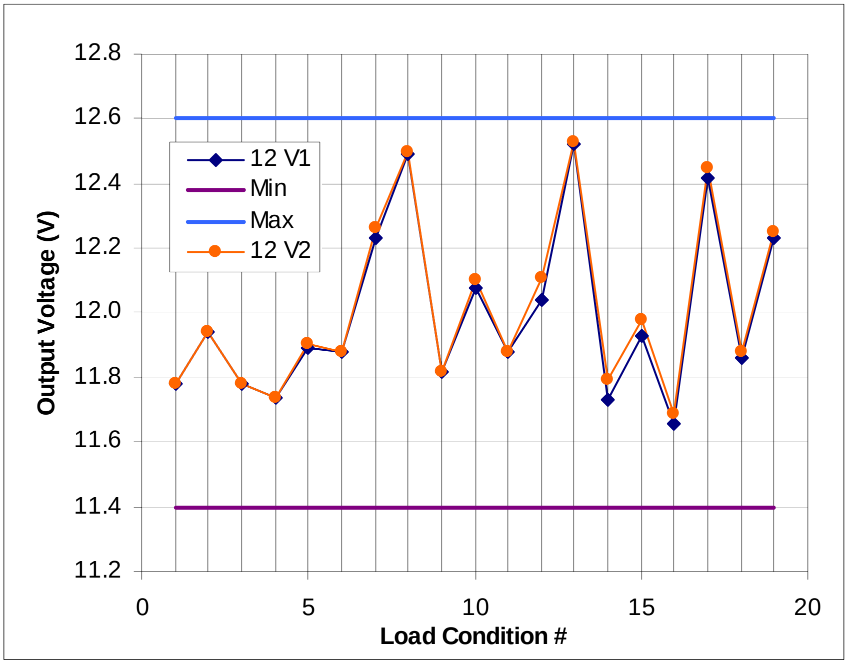


Figure 9: 12 V1 and 12 V2 outputs cross regulation vs load conditions

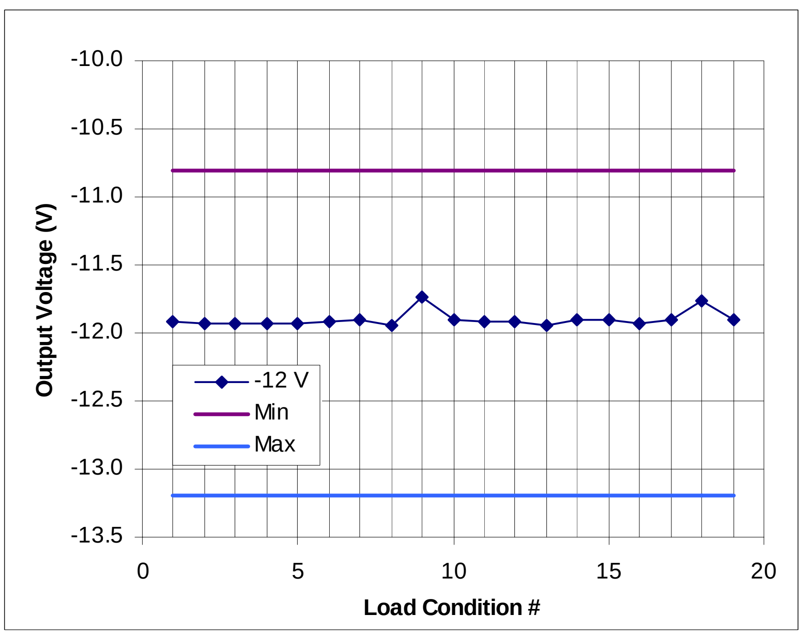


Figure 10: -12 V output cross regulation vs load conditions

The 5 V, 12 V and 3.3 V outputs are evaluated independently under transient load conditions. Each output is loaded at 50% and the load is reduced to 25% or increased to 75% of the maximum rated current. The transient voltage tolerance of each of the 5 V, 12 V and 3.3 V outputs is +/- 5%. Table 4 summarizes the transient load conditions and limits for each output. Transient waveforms are shown in Figure 11 through Figure 14.

Output	Minimum Load (A)	Nominal Load (A)	Maximum Load (A)	Voltage under/overshoot (V)
5 V	5.5	11	16.5	±250mV, ≤0.5V pk-pk
3.3 V	4.25	8.5	12.75	±170mV, ≤0.34V pk-pk
12 V1	4.5	9	13.5	±600mV, ≤1.2V pk-pk
12 V2	4.5	9	13.5	±600mV, ≤1.2V pk-pk

Table 4: Transient load conditions

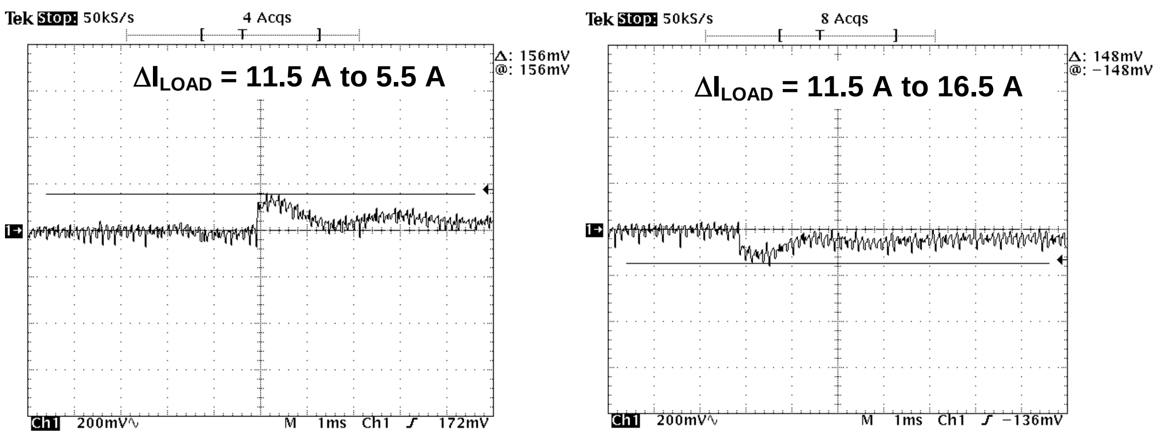


Figure 11: 5 V output transient load response

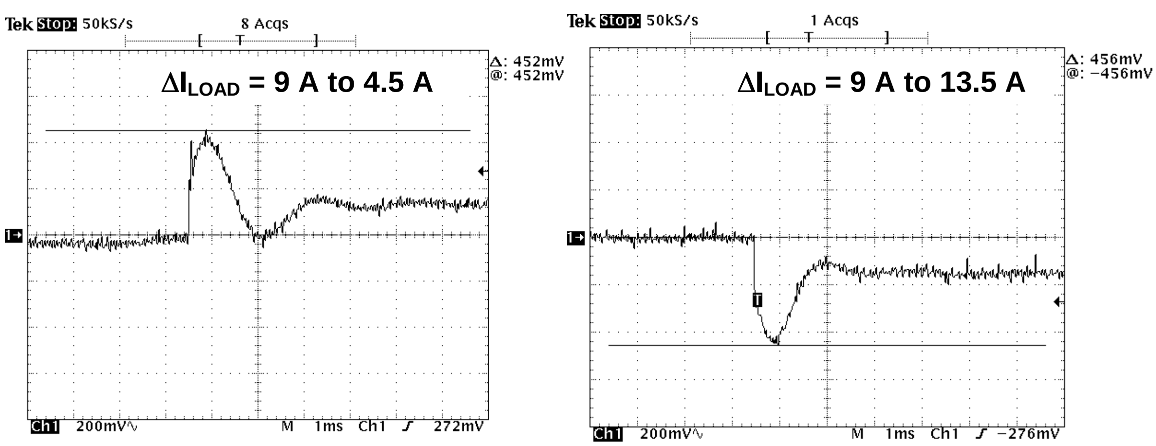


Figure 12: 12 V1 output transient load response

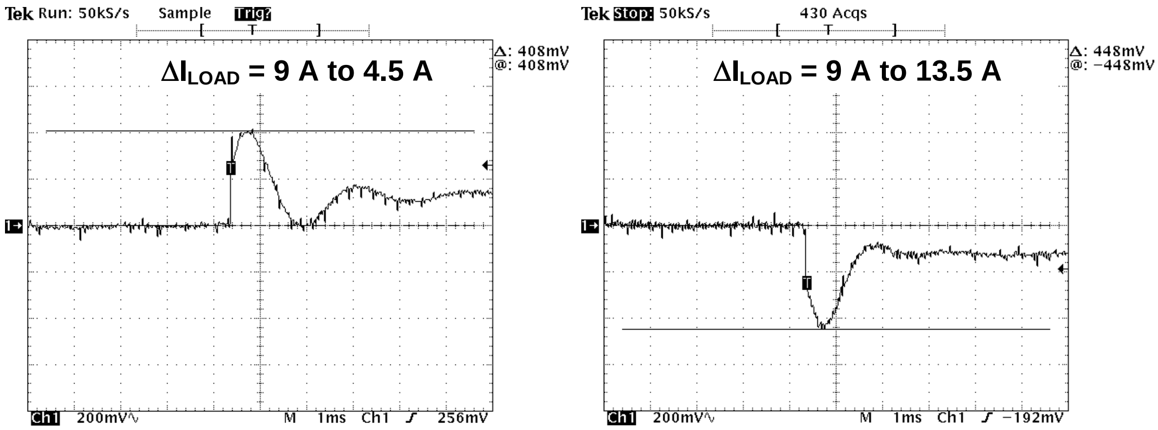


Figure 13: 12 V2 output transient load response

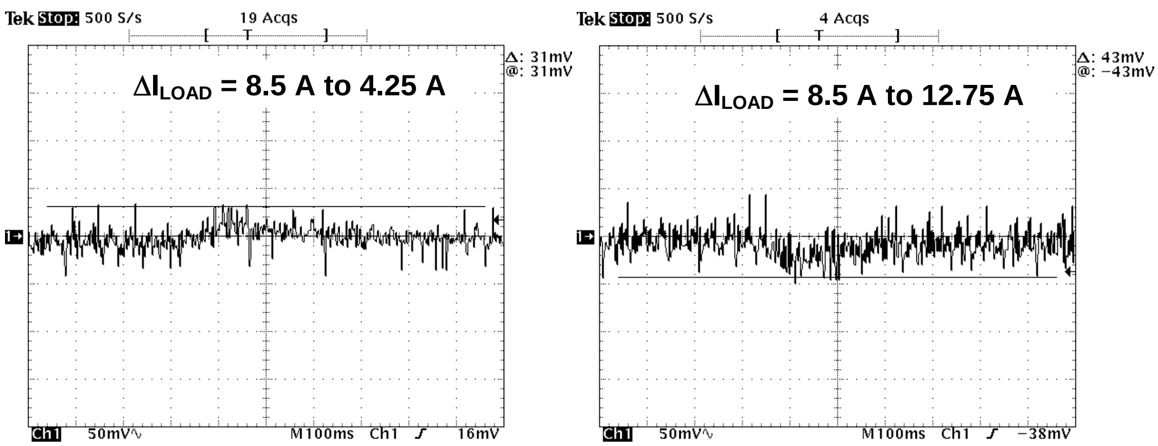


Figure 14: 3.3 V output transient load response

All the outputs meet the transient voltage requirements under the evaluated conditions. The ripple voltage of each output is measured at the maximum load for each output. The output ripple is measured across 10 μF/MLC parallel 1000 μF low ESR/ESL termination capacitors. The target ripple is +/- 120 mV for the 12 V outputs and 50 mV for all other outputs. Figure 15 through Figure 20 show the output voltage ripple measurements. All outputs meet the voltage ripple requirements.

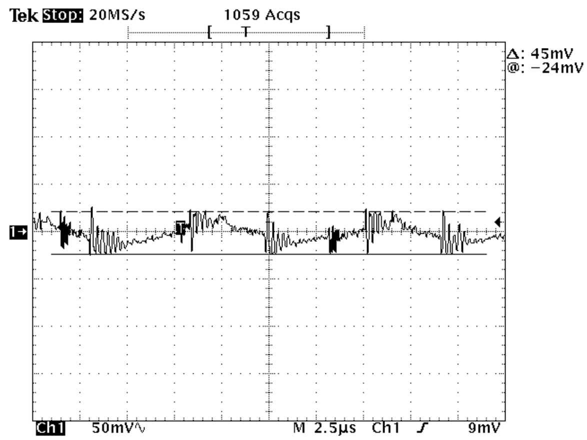


Figure 15: 5 V output voltage ripple at full load

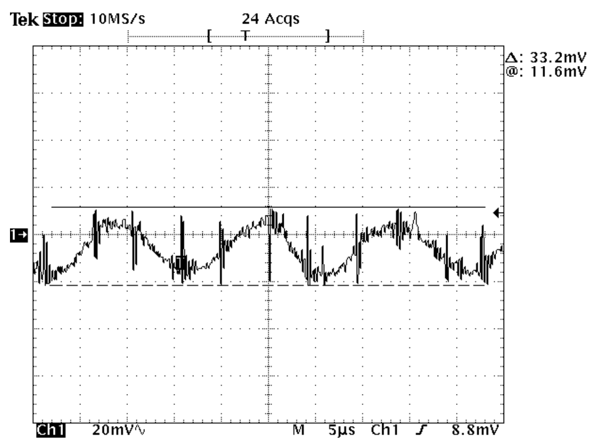


Figure 16: 3.3 V output voltage ripple at full load

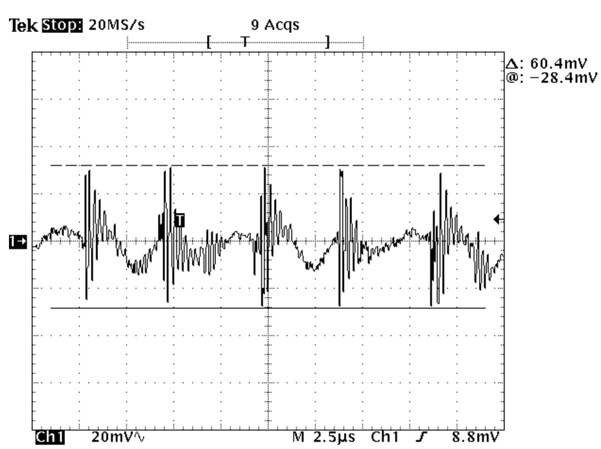


Figure 17: 12 V1 output voltage ripple at full load

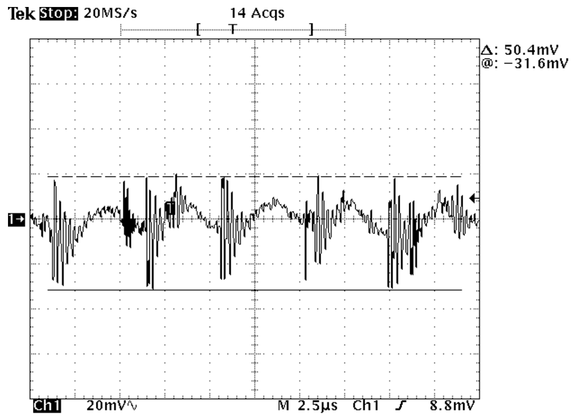


Figure 18: 12 V2 output voltage ripple at full load

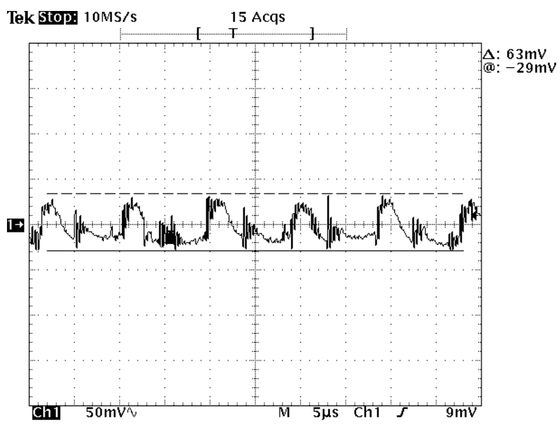


Figure 19: -12 V output voltage ripple at full load

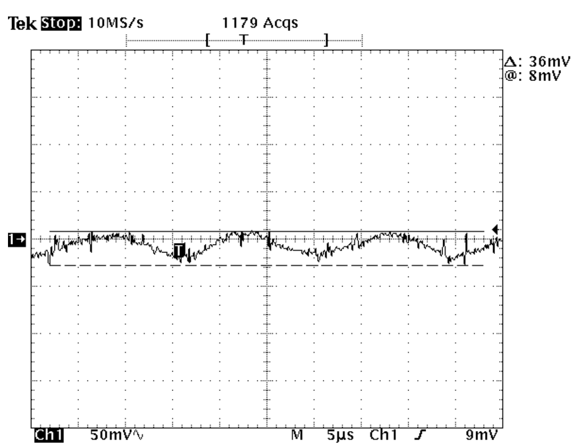


Figure 20: 5 V SBY output voltage ripple at full load

The required holdup time at full load is 20 ms. Holdup time is measured from the moment the AC power is removed to when the PWR_OK signal goes low. Figure 21 shows the holdup time at full load. Channel 1 is the AC power and Channel 2 is the PWR_OK signal. Holdup time is measured at 22.5 ms.

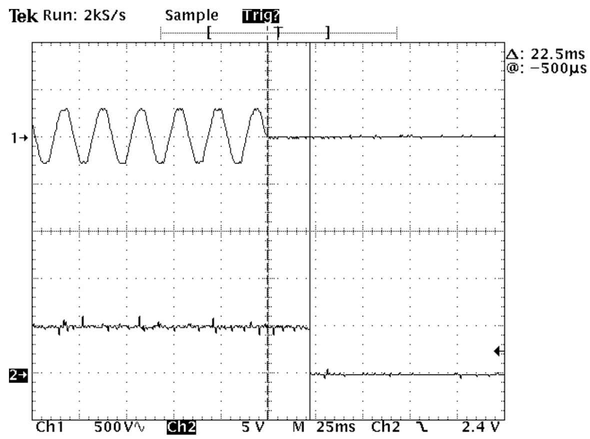


Figure 21: Holdup time at full load

The input inrush current of the system at 230 Vac at full load is measured at 28.8 A as shown in Figure 22.

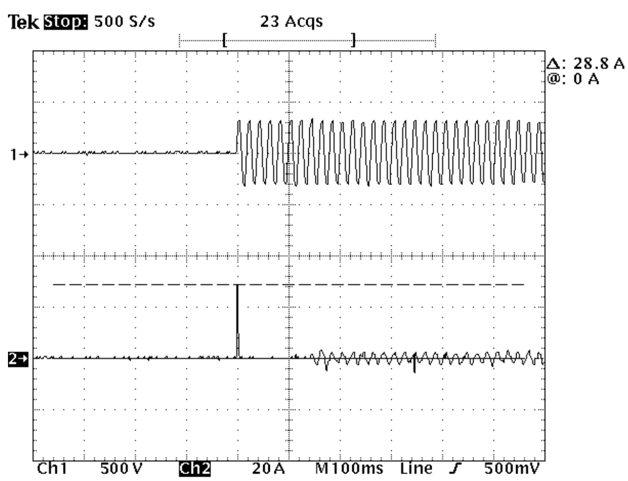


Figure 22: Input inrush current

5. Evaluation Guidelines

Evaluation of the reference design should be attempted only by persons who are intimately familiar with power conversion circuitry. Lethal mains referenced voltages and high dc voltages are present within the primary section of the ATX circuitry. All testing should be done using a mains high-isolation transformer to power the demonstration unit so that appropriate test equipment probing will not affect or potentially damage the test equipment or the ATX circuitry. The evaluation engineer should also avoid connecting the ground terminal of oscilloscope probes or other test probes to floating or switching nodes (e.g. the source of the active clamp MOSFET). It is not recommended to touch heat sinks, on which primary active components are mounted, to avoid the possibility of receiving RF burns or shocks. High impedance, low capacitance test probes should be used where appropriate for minimal interaction with the circuits under investigation. Particular care should be taken when probing the high impedance input pins of the NCP1653 power factor controller and the NCP1562 active clamp controller. As with all sensitive switchmode circuitry, the power supply under test should be switched off from the ac mains whenever the test probes are connected and/or disconnected.

The 3.3 V output does not have a minimum load requirement and a preload resistor is included in the -12 V output.

The NCP1027 standby flyback converter will be operational as long as there is ac mains voltage applied to the system. This auxiliary converter can be evaluated by merely applying the mains voltage to the board. The supervisory IC enable input and monitoring circuitry will have to be disabled. The supervisory circuitry will normally cause a shutdown of the PFC (and the main converter) if the 3.3 V, the 5 V and the 12 V outputs are not sensed at their nominal voltage.

The evaluating engineer should also be aware of the idiosyncrasies of constant current type electronic loads when powering up the ATX demonstration unit. If the loads are adjusted to be close to the ATX's maximum rated output power, the unit could shut down at turn on due to the instantaneous overloading effect of the constant current loads. As a consequence, electronic loads should be set to constant resistance mode or rheostats should be used for loads. The other alternative is to start the supply at light to medium load and then increase the constant current electronic loads to the desired level.

The board is designed to fit in a traditional ATX enclosure as shown in Figure 23.

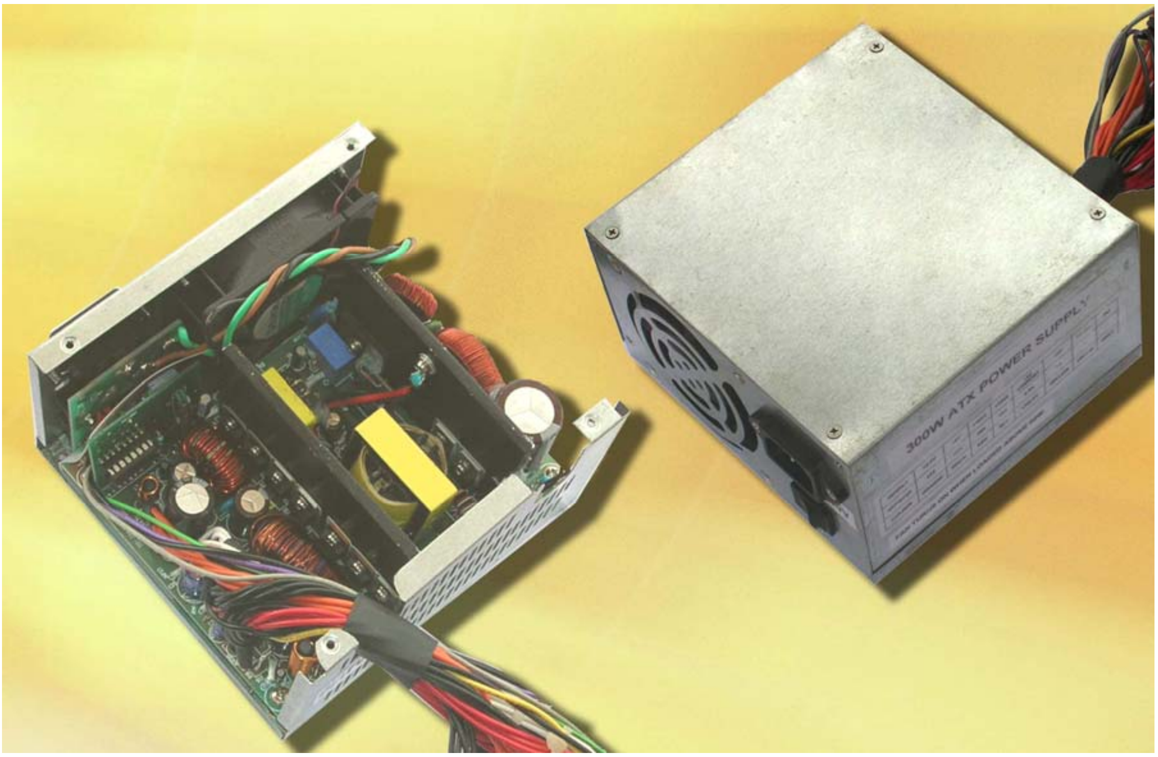


Figure 23: ATX solution boards in ATX enclosure

6. Schematics

The power supply is implemented using a single sided PCB board. Added flexibility is provided by using daughter cards for the PFC (NCP1653), active clamp (NCP1562) controllers. A PCB board is also used for the 3.3 V post regulator (NCP4330) and supervisory controllers. This allows the use of newer generation controllers without the need of a complete re-layout of the main board. An additional daughter card is used for EMC components. The individual PCB board schematics are shown in Figure 24 through Figure 27.

The schematic of the main PCB board is divided in three sections: PFC & standby section, active clamp section, and the post regulator section as shown in Figure 28 through Figure 30, respectively.

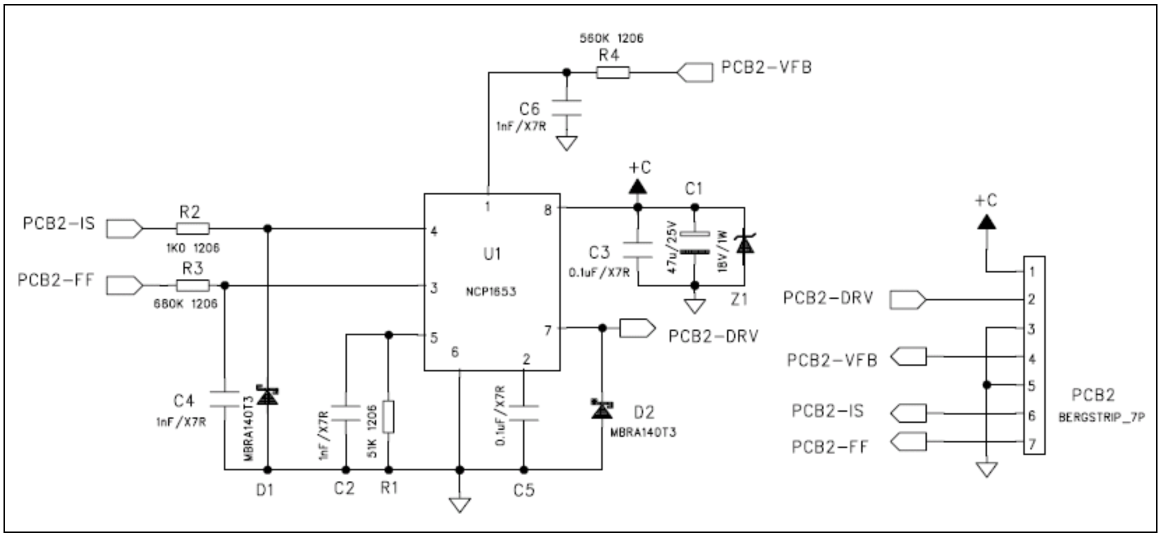


Figure 24: PFC controller PCB board schematic

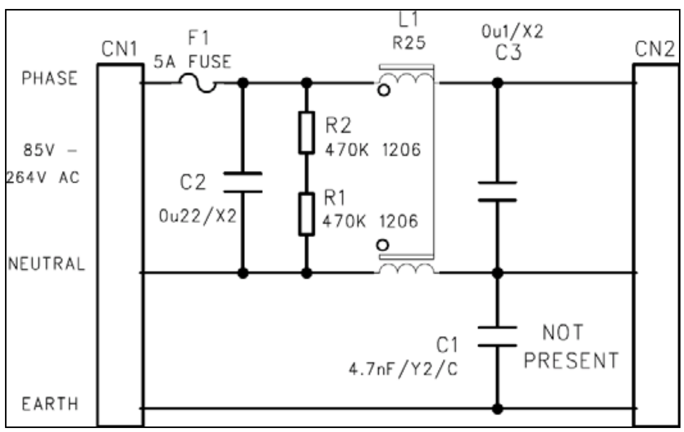


Figure 25: EMC component board

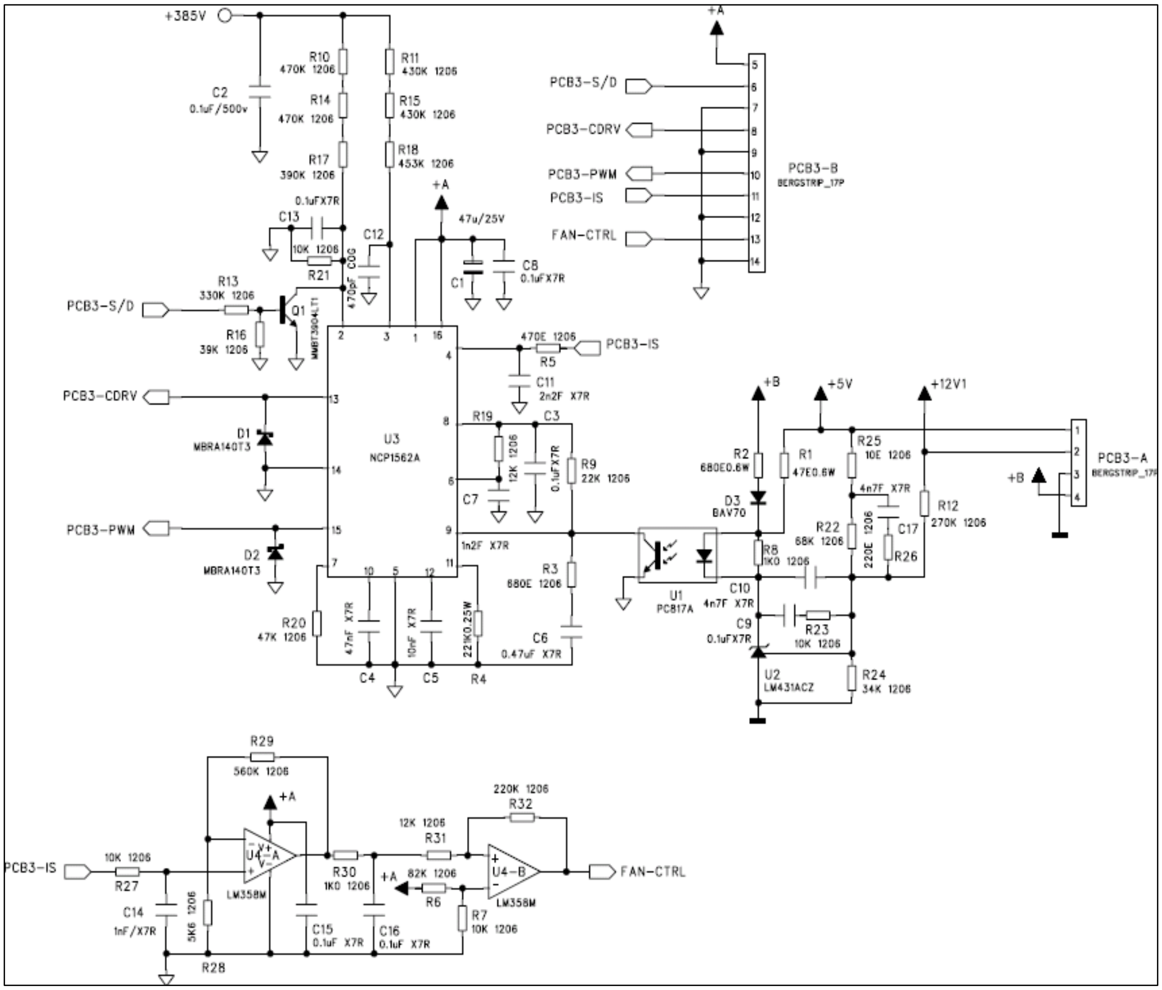


Figure 26: Active clamp controller PCB board schematic

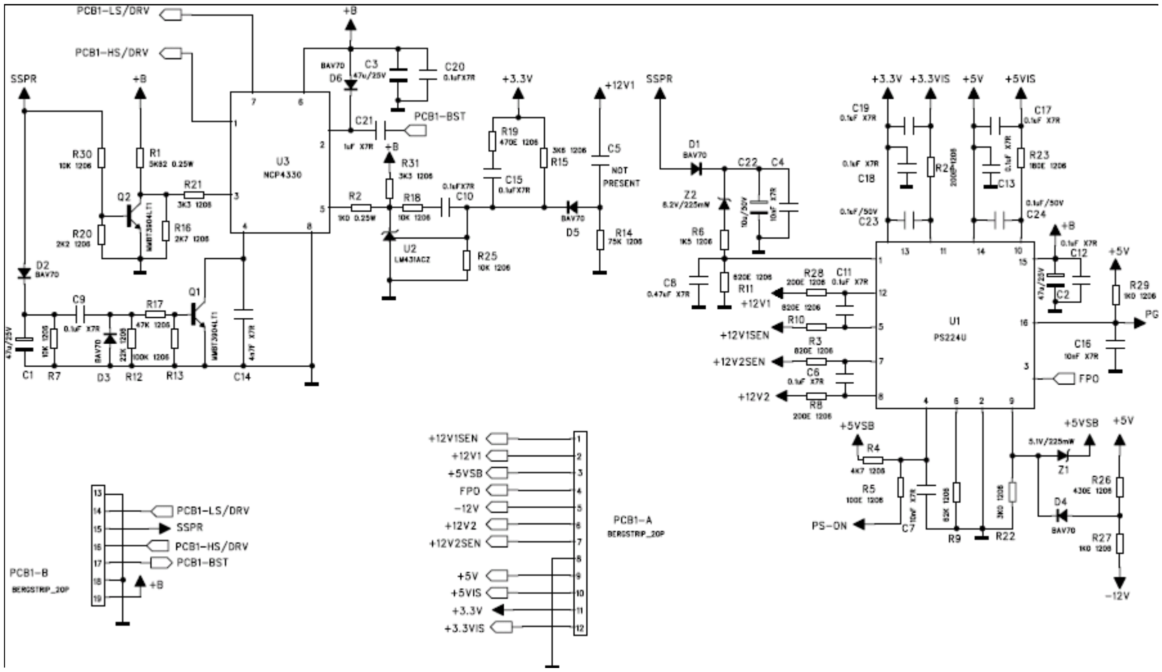


Figure 27: Supervisory and 3.3 V post regulator controller PCB board schematic

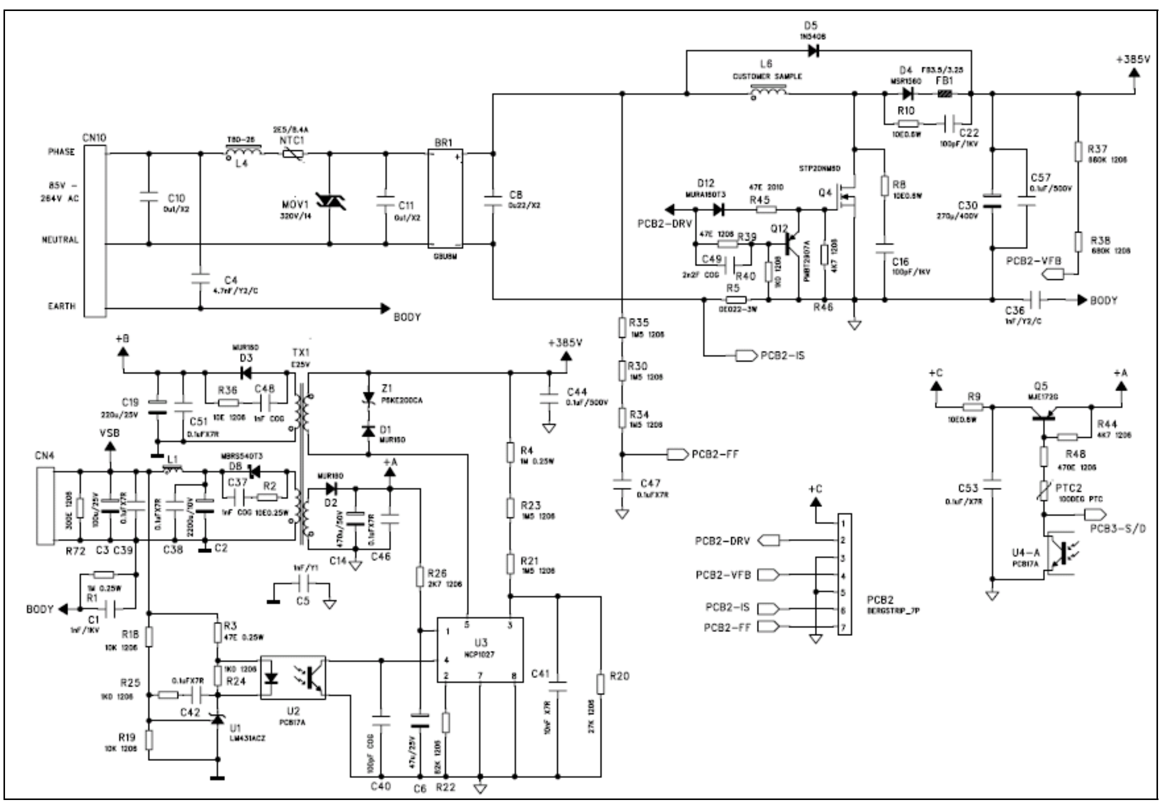


Figure 28: Main PCB board schematic PFC and standby section

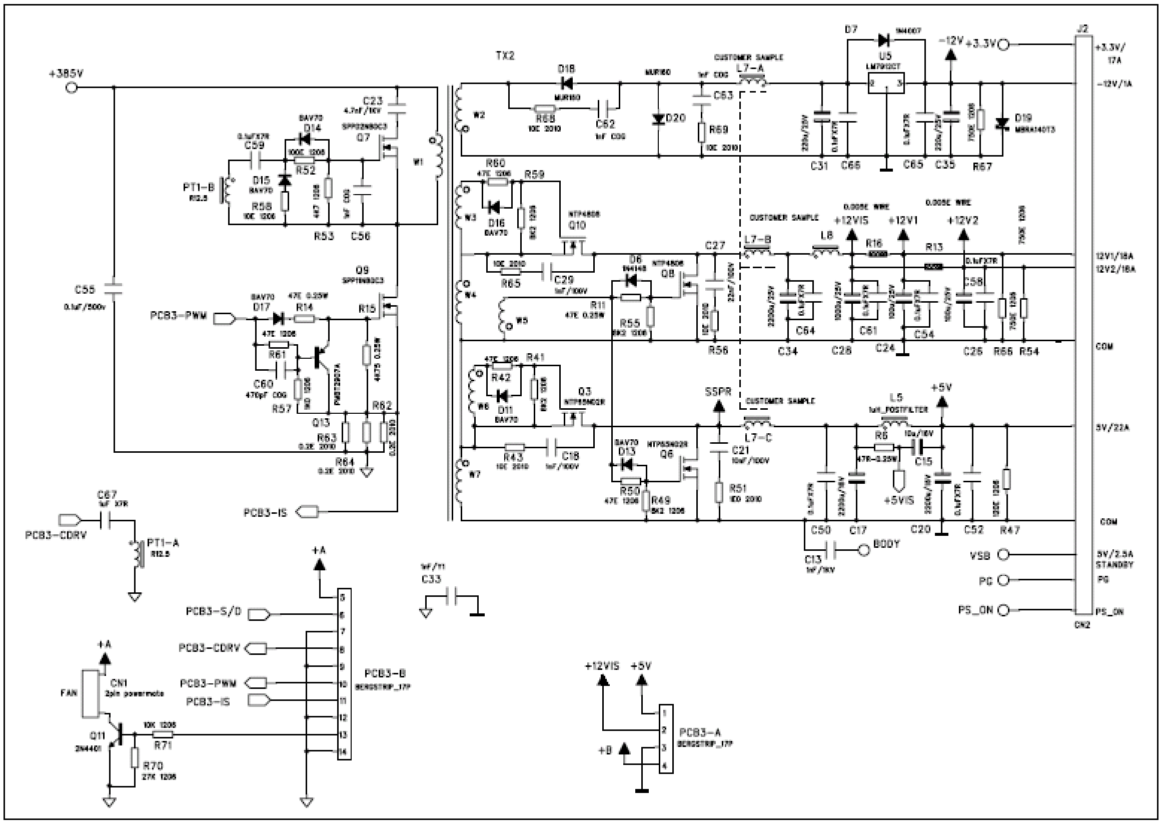


Figure 29: Main PCB board schematic active clamp stage section

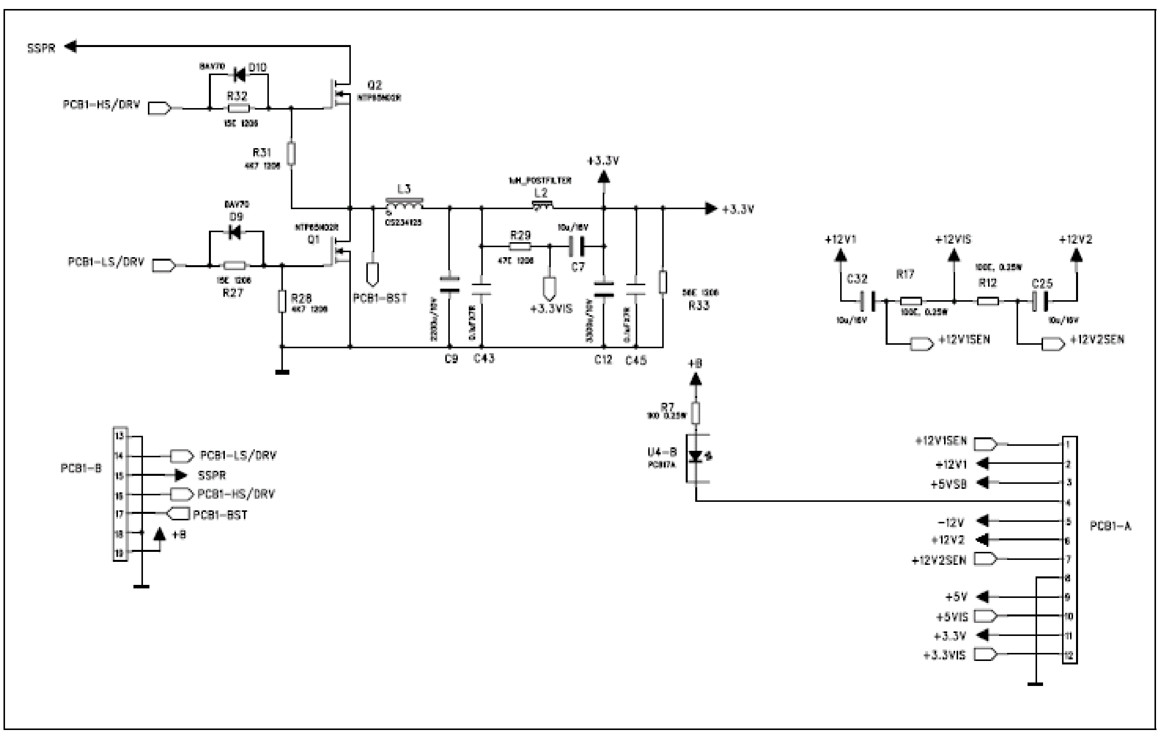


Figure 30: Main PCB board schematic 3.3 V post regulator section

7. Parts List

The bill of materials (BOM) for the design is provided in this section. To reflect the schematics shown in the previous section, the BOM have also been broken into different sections and provided in separate tables – Table 5 through Table 9.

It should be noted that a number of components used during the development cycle were based on availability. As a result, further cost reductions and better inventory management can be achieved by component standardization. IE, the unique part numbers can be **SIGNIFICANTLY** reduced by standardization and re-use of component values and case sizes. This will result in a lower cost BOM and better inventory management.

Description	Part Numbers	Qty
0.1µF, ±10%, 500V, X7R, Case Size 1812	VJ1812Y104KXEAT	3
0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	18
0.1µF, ±20%,300VAC, Interference Suppression CapX2	PHE840EB6100MB05R17	2
0.22uF, ±20% ,300VAC, Interference Suppression CapX2	PHE840EX6220MB06R17	1
270µF, ±20%, 400V, -40°C to +85°C, B43501 series , Snap-In, Pitch 10mm	B43501A9277M000	1
100pF, ±10%, 1kVDC,High voltage ceramic disc Capacitor, -25°C to +85°C	DEBB33A101KC1B	2
100pF, ±5%, 50V, COG, Case Size1206	B37871K5101J060	1
1nF, ±20% , 100V , Stacked-film capacitor, MMK series , 5mm Pitch	MMK5 102M100J01L4 BULK	2
1nF, ±10%, 1kVDC,High voltage ceramic disc Capacitor,-25°C to +85°C	DEBB33A102KA2B	2
1nF, ±20%,, 440VAC,Interference Suppression CapY1	PME294RB4100MR30	2
1nF,±20%, ,440/250VAC,Interference Suppression CapX1/Y2	2252 812 35 027	1
1nF, ±10%, 100V, COG, Case Size1206	B37871K1102J560	5
4.7nF, ±10%, 1kVDC, High voltage ceramic disc Capacitor, -25°C to +85°C	DEBB33A472KA3B	1
4.7nF,±10% ,440/250VAC,Interference Suppression CapX1/Y2	2252 812 35 427	1
10nF, ±20% , 100V , Stacked-film capacitor, MMK series , 5mm Pitch	MMK5 103M100J01L4 BULK	1
10nF, ±10%, 50V, X7R, Case Size1206	B37872K5103K060	1
22nF, ±20% , 100V , Stacked-film capacitor, MMK series , 5mm Pitch	MMK5 223M100J01L4 BULK	1
2n2F, ±5%, 50V, COG, Case Size1206	B37871K5222J060	1
470pF, ±5%, 50V, COG, Case Size1206	B37871K5471J060	1
10µF, ±20%, 16V,-40°C to +85°C, Type VR, Radial, Pitch 2mm, Pb Free	UVR1C100MDD	4
220µF, ±20%, 25V,-40°C to +85°C, Type VR, Radial, Pitch 3.5mm, Pb Free	UVR1E221MPD	1
3300µF, ±20%, 10V,-40°C to +85°C, Type VR, Radial, Pitch 5mm, Pb Free	UVR1A332MHD	1
47µF, ±20%, 25V,-40°C to +85°C, Type VR, Radial, Pitch 2mm, Pb Free	UVR1E470MDD	1
2200µF, ±20%, 10V,-40°C to +85°C, Type PM, Radial, Pitch 5mm, Pb Free	UPM1A222MHD	2
220µF, ±20%, 25V,-40°C to +85°C, Type PW, Radial, Pitch 3.5mm, Pb Free	UPW1E221MPD	2
470E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-4700	1
0.2E, ±1%,1W, Case Size 2010	CRL1206-FW-0R20E_	3
0E022, ±5%, 3W,Wire Wound Resister	BSI680E022±5%±100ppm/°C	1
100E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-1000	1
100E, ±1%, 0.25W, MFR	EROS2CHF1000	2
10E0, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-10R0	2
10E, ±1%, 0.5W, Case Size 2010	MCR50-JZH-J 10R0	5

10E,±1%, 0.25W, MFR	EROS2CHF10R0	1
10E,±1%, 0.6W, MFR	2322 186 3 1009	3
10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	3
120E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-1200	1
15E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-15R0	2
1E0, ±5%, 0.5W, Case Size 2010	MCR50-JZH-J 1R0	1
1K0, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1001	4
1K0, ±1%, 0.25W, MFR	EROS2CHF1001	1
1M5, ±5%, 0.25W,Case Size 1206	MCR18 EZP J-155	2
1M5, ±5%, 0.25W,Case Size 1206	MCR18 EZH J-155	3
1M, ±1%, 0.25W, MFR	EROS2CHF1004	2
27K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2702	2
47E, ±1%, 0.25W, Case Size 1206	MCR18 EZP F-47R0	1
47E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-47R0	5
47E, ±1%, 0.5W, Case Size 2010	MCR50-JZH-F 47R0	1
47E,±1%, 0.25W, MFR	EROS2CHF47R0	4
4K7, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4701	5
4K75,±1%, 0.25W, MFR	EROS2CHF4751	1
56E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-56R0	1
680K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-6803	2
750E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-7500	3
82K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-8202	1
8K2, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-8201	4
2K7, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2701	1
300E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-3000	1
0.005E, WIRE	CUSTOMER SAMPLE	2
If(av) = 1A, V(rrm) = 1000V, Standard Rectifier.DO-41 Package	1N4007	1
If(av) =200mA, V(rrm) =75V, Small Signal Diode,Axial Lead,DO-35 Pkg	1N4148	1
If(av) =3A, V(rrm) =1000V, Standard recovery Diode,DO-201AD Pkg	1N5408	1
If = 200mA, Vrrm = 70V, Dual Switching Diode,SOT-23 Package	BAV70LT1	2
If = 200mA, Vrrm = 70V, Dual Switching Diode,SOT-23 Package	BAV70	6
If = 1A, Vrrm = 40V, Schottky Diode, SMA Package	MBRA140T3	1
If = 5A,Vrrm = 40V, SMC Package, Schottky Diode	MBRS540T3	1
If(av) =15A,V(rrm) =600V,Soft recovery diode ,TO-220AC Package	MSR1560	1
If(av) = 1A,V(rrm) = 600V,Ultra Fast Rectifier, DO-41 Package	MUR160	5
If = 1A, Vrrm = 600V, Ultrafast Rectifier, SMA Package	MURA160T3	1
Vceo=80V, Ic=3A, PNP Comp plastic Silicon Power Tr, TO-225AA	MJE172G	1
Vdss=800V,Id=2A, Rds-on=2.7E,N-Channel Mosfet,TO-220AB Pkg	SPP02N80C3	1
Vdss=800V,Id=11A, Rds-on=0.45E, N-Channel Mosfet, TO-220 Pkg	SPP11N80C3	1
Vdss=600V,Id=20A, Rds-on=0.25E,N-Channel Mosfet,TO-220 Pkg	STP20NM60	1
Vdss=30 V, Rds-on=6 mE, N-Channel Mosfet,TO-220AB Pkg	_	2
Vdss=24V,Id=65A, Rds-on=0.0125E, N-Channel Mosfet, TO-220 Pkg	NTP65N02R	4
Vceo=60V, Ic=600mA, PNP Switching Transister, SOT-23 Pkg	MMBT2907A	2
Vceo=40V, Ic=600mA, NPN Switching Transistor, TO-92 Pkg	2N4401	1
1uH, POST FILTER	1uH_POSTFILTER	4
Powdered Torroidal core AL= 105,Weight 14.48gms-Post Reg	CS 234 125 E	1
Powdered Iron Core, AL=46-Input EMI Filter	T80-26	1
CUSTOMER SAMPLE - PFC Inductor	CUSTOMER SAMPLE	1

Powdered Torroidal core AL= 117,Weight 47gms-Ouput Coupled Inductor	CH 358 125 E	1
E25,10Pin, Vertical coil former,E25/13/7 Yoke - Standby TX	B66208J1110T001/A20100000	1
ETD39, 16 PIN VERTICAL BOBBIN, N87 CORE - Main TX		1
Ferrite Torroidal Core,R-12.5, AL= 2200 ± 25%, N30-Gate Drive TX	B64290L0044X830	1
Vbr=200V,Zener Transient Voltage Supressor, CASE 17-2.	P6KE200CA	1
100 deg celcius PTC Temperature senser	B59901D0100A040	1
2E5, 8.4A, ±20%, NTC Inrush Current Limiter	B57238S0259M000	1
EURO CONNECTOR ,DIN416 12 H15	AS PER APPROVED SOURCES	1
2pin powermate	CK	1
3 PIN MOLEX Connector	22-04-1.31	1
3 PIN MOLEX Connector	22-04-1.31	1
Vac=320V, Diameter14, Metal Oxide Varistor	B72214S0321K101	1
EMI Suppression Bead 3.5mm Diameter, 3.25mm Length	2673000101	1
8A,1000V, Bridge Rectifier, Peak Surge Curent=200A, GBU Pkg	GBU8M	1
Adjustable Precision Zener Shunt Reg,TO-92 Pkg, +/-2%	LM431ACZ	1
4 Pin Type Optocoupler,CTR 60% to 160%,DIP4 Pkg	PC817A	1
High-Voltage Switcher, PDIP-8 Package, 0°C to 125°C, Pb-Free	NCP1027P065G	1
4 Pin Type Optocoupler,CTR 60% to 160%,DIP4 Pkg,-30°C to 100°C	PC817A	1
1A , -12V 3-Terminal Fixed Voltage regulator, TO-220 Package	LM7912CT	1

Table 5: Main Section

Description	Part Numbers	Qty
47µF, ±20%, 25V,-40°C to +85°C, Type VR, Radial, Pitch 2mm, Pb Free	UVR1E470MDD	1
0.1µF, ±10%, 500V, X7R, Case Size 1812	VJ1812Y104KXEAT	1
0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	2
0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	4
0.47µF, ±10%, 50V, X7R, Case Size1206	B37872K5474K062	1
10nF, ±10%, 50V, X7R, Case Size1206	B37872K5103K060	1
1n2F, ±10%, 50V, X7R, Case Size1206	VJ1206Y122KXAAT	1
1nF, ±10%, 50V, X7R, Case Size1206	B37872K5102K060	1
2n2F, ±10%, 50V, X7R, Case Size1206	B37872K5222K060	1
470pF, ±5%, 50V, COG, Case Size1206	B37871K5471J060	1
47nF, ±10%, 50V, X7R, Case Size1206	B37872K5473K060	1
4n7F, ±10%, 50V, X7R, Case Size1206	B37872K5472K060	2
10E0, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-10R0	1
10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	4
12K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1202	2
1K0, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1001	2
220E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-2200	1
220K, ±1%, 0.25W,Case Size 1206	MCR18 EZP F-2203	1
221K,±1%, 0.25W, MFR	EROS2CHF2213	1
22K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2202	1
270K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2703	1
330K, ±1%, 0.25W,Case Size 1206	MCR18 EZP F-3303	1
34K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3402	1
390K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3903	1
39K, ±1%, 0.25W,Case Size 1206	MCR18 EZP F-3902	1
430K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4303	2
453K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4533	1
470E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-4700	1
470K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4703	2
47E,±1%, 0.6W, MFR	2322 186 3 4709	1
47K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4702	1
560K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-5603	1
5K6, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-5601	1
680E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-6800	1
680E,±1%, 0.6W, MFR	2322 186 3 6801	1
68K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-6802	1
82K, ±1%, 0.25W,Case Size 1206	MCR18 EZP F-8202	1
If = 200mA, Vrrm = 70V, Dual Switching Diode,SOT-23 Package	BAV70LT1	1
Dual Operational Amplifier,SO-8 Package, 0°C to 70°C	LM358M	1
Adjustable Precision Zener Shunt Reg,TO-92 Pkg, -0°C to 70°C, +/-2%	LM431ACZ	1
If = 1A, Vrrm = 40V, Schottky Diode, SMA Package	MBRA140T3	2
Vceo=40V, Ic=200mA, NPN General Purpose Transistor, SOT-23 Pkg	MMBT3904LT1	1
Active Clamp Mode PWM Controller , SO-16Package	NCP1562A	1
4 Pin Type Optocoupler,CTR 60% to 160%,DIP4 Package,-30°C to 100°C	PC817A	1

Table 6: Active Clamp Section

Description	Part Numbers	Qty
47µF, ±20%, 25V,-40°C to +85°C, Type VR, Radial, Pitch 2mm, Pb Free	UVR1E470MDD	1
1nF, ±10%, 50V, X7R, Case Size1206	B37872K5102K060	3
0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	2
1K0, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1001	1
51K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-5102	1
560K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-5603	1
680K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-6803	1
18V,1W,Zenerdiode ,DO-41 package	1N4746A	1
If = 1A, Vrrm = 40V, Schottky Diode, SMA Package	MBRA140T3	2
Fixed-Frequency Current-Mode Power Factor Correction Controller	NCP1653	1

Table 7: PFC Section

Description	Part Numbers	Qty
0.1µF, ±20%,300VAC, Interference Suppression CapX2,	PHE840EB6100MB05R17	1
0.22uF, ±20% ,300VAC, Interference Suppression CapX2 , -55°C to +105°C	PHE840EX6220MB06R17	1
3 PIN MOLEX Connector	22-04-1.31	2
4.7nF,±10% ,440/250VAC,Interference Suppression CapX1/Y2	2252 812 35 427	1
470K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4703	2
11.4 X 9.4 X 24.4mm,Semi Enclosed Fuse Holder	Cat No: 4628	1
Ferrite Torroidal Core,R-25, AL= 4620 ± 25%, EMI Choke	B64290L0618X830	1

Table 8: EMC Section

Description	Part Numbers	Qty
0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	8
0.1µF, ±10%, 50V, X7R, Case Size1206	B37872K5104K060	3
0.47µF, ±10%, 50V, X7R, Case Size1206	B37872K5474K062	1
10nF, ±10%, 50V, X7R, Case Size1206	B37872K5103K060	3
4n7F, ±10%, 50V, X7R, Case Size1206	B37872K5472K060	1
47µF, ±20%, 25V,-40°C to +85°C, Type VR, Radial, Pitch 2mm, Pb Free	UVR1E470MDD	3
10µF, ±20%, 50V,-40°C to +85°C, Type PW, Radial, Pitch 1.5mm, Pb Free	UPW1H100MPD6	1
0.1uF, ±10%,50V,X7R Multilayered Ceramic Capacitor, -55°C to +125°C	C322C104K5R5CA	2
100E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-1000	1
100K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1003	1
10K, ±1%, 0.25W,Case Size 1206	MCR18 EZP F-1002	1
10K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1002	3
180E, ±1%, 0.25W, Case Size 1206	MCR18 EZP F-1800	1
1K0, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1001	2
1K5, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-1501	1
1K0, ±1%, 0.25W, MFR	EROS2CHF1001	1
200E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-2000	2
200E, ±1%, 0.25W, Case Size 1206	MCR18 EZP F-2000	1
22K, ±1%, 0.25W,Case Size 1206	MCR18 EZP F-2202	1
2K2, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2201	1
2K7, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-2701	1
3K0, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3001	1
3K3, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3301	2
3K6, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-3601	1
430E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-4300	1
470E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-4700	1
47K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4702	1
4K7, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-4701	1
5K62,±1%, 0.25W, MFR	EROS2CHF5621	1
620E, ±1%, 0.25W, Case Size 1206	MCR18 EZH F-6200	1
62K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-6202	1
75K, ±1%, 0.25W,Case Size 1206	MCR18 EZH F-7502	1
820E, ±1%, 0.25W, Case Size 1206	MCR18 EZP F-8200	2
5.1V,225mW,Zenerdiode ,SOT-23 package	BZX84C5V1LT1	1
8.2V,0.225W,Zenerdiode, SOT-23 package	BZX84C8V2LT1	1
If = 200mA, Vrrm = 70V, Dual Switching Diode,SOT-23 Package	BAV70LT1	6
Vceo=40V, Ic=200mA, NPN General Purpose Transistor, SOT-23 Pkg	MMBT3904LT1	2
4 Channel Secondary Monitoring IC, DIP-16 Package, -30°C to 90°C	PS224	1
Adjustable Precision Zener Shunt Reg,TO-92 Pkg, -0°C to 70°C, +/-2%	LM431ACZ	1
Post Regulation Driver	NCP4330	1

Table 9: Post Regulation Section

8. Critical Component Information

It is shown that an active clamp forward converter provides a higher efficiency compared to a traditional forward converter. However, special attention has to be provided to several blocks of the circuit to ease design. The areas are described below:

1. Power transformer: Contrary to traditional forward converters, a low magnetizing inductance is required to achieve zero- or near-zero volt switching. This is easily achieved by gapping the transformer. In this design, a 6.7 mH primary inductance is used. The transformer datasheet is included in the Appendix.
2. Active clamp capacitor: The active clamp capacitor stores voltage to reset the transformer during the power switch off time. This capacitor sees the magnetizing current. Therefore, the ESR of this capacitor should be considered when selecting this capacitor. A high quality low ESR capacitor should be used to prevent overheating. Ceramic or propylene are good options.
3. Coupled inductor: A coupled inductor is used to regulate the 5 V, 12 V and -12 V outputs. Good cross regulation is achieved by using the same number of turns on the inductor as in the transformer winding.
4. High side transformer for active clamp switch: High primary inductance is required to reduce magnetizing current on the high side transformer and provide adequate voltage to drive the active clamp switch. The control signal for the active clamp switch is 1-D. Therefore, the high side transformer is designed to operate at large duty cycles or volt-seconds without saturating. The transformer datasheet is included in the Appendix.

9. Resources/Contact Information

Data sheets, applications information and samples for the ON Semiconductor components are available at www.onsemi.com. Links to the datasheets of the main components used in this design are included in the Appendix.

10. Appendix

Link to ON Semiconductor's web site:

- ON Semiconductor Home Page

Industry Information Links

- ENERGY STAR
- 80 PLUS Efficiency Requirements
- IEC1000-3-2 Requirements
- ATX 12 V Form Factor
- International Energy Agency
- China Standard Certification Center (formerly CECP)
- European Union (EU) Energy Star Page

MAGNETICS DESIGN DATA SHEET

Project / Customer: ON Semiconductor ATX project

Part Description: 300 W PFC choke - 4 A rms, 6 A pk, 600 uH, Rev. 2

Schematic ID: L4

Core Type: PQ32/30 (Mag Inc 43230), 100 kHz material

Core Gap: 0.075" (1.9 mm) total gap

Inductance: 550 - 650 uH

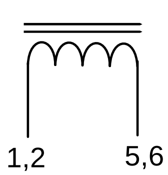
Bobbin Type: PC-B3230-LA (12 pin vertical mount)

Windings (in order):

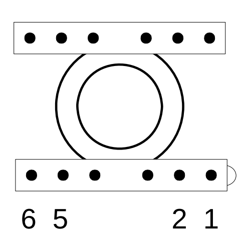
Winding # / type	Turns / Material / Gauge / Insulation Data
1,2 - 5,6	73 turns of 4 strands of #26HN (or equiv. of #21 Litz). Approx. 1 twist per inch; self terminate to pins. Insulate with layer of mylar tape.

Hipot: NA

Schematic



Lead Breakout / Pinout



MAGNETICS DESIGN DATA SHEET

Project / Customer: ON Semiconductor ATX project

Part Description: Aux/standby flyback transformer; 65 kHz, Rev. 2

Schematic ID: T1

Core Type: E25/10/6 (E24-25)

Core Gap: 0.01" (0.25 mm) total

Inductance: 2.5 - 2.8 mH (primary)

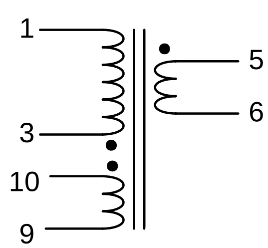
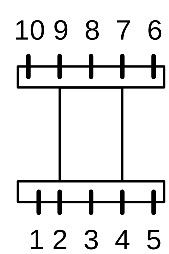
Bobbin Type: Ferroxcube # E24-25PCB1-10 (10 pin horizontal mount)

Windings (in order):

Winding # / type	Turns / Material / Gauge / Insulation Data
30 V Secondary (10 - 9)	29 turns of #30HN over 1 layer; self-leads to pins; Insulate with 1 or 2 layers of mylar tape.
Primary (3 - 1)	105 turns of #32HN, 35TPL x 3 layers; self-leads to pins.
5 V Secondary (5 - 6)	5 turns of #22 triple insulated wire OR two strands of #24HN spiral wound over window. Cuff ends with tape if latter method is used for proper isolation from primary.

Vacuum varnish

Hipot: 2.7 kV from 5 V secondary to primary and 30 V secondary

Schematic	Lead Breakout / Pinout
	(top view) 

MAGNETICS DESIGN DATA SHEET

Project / Customer:ON Semiconductor - ATX Project

Part Description: Main output choke; 3 output coupled inductor, 250 kHz, Rev. 2

Schematic ID: LX1

Core Type: PQ3230

Core Gap: 0.020" total (all in center leg preferred)

Inductance: 1.6 uH minimum on 5 V (foil) winding; 10 uH on 12 V windings

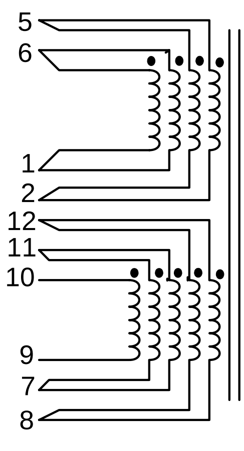
Bobbin Type: 12 pin vertical pc mount

Windings (in order):

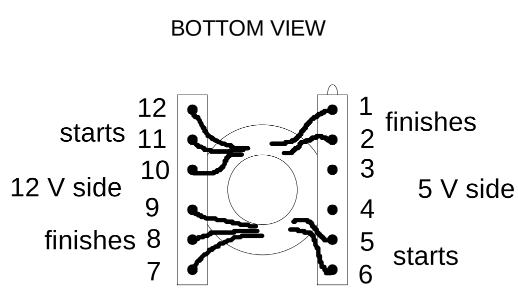
Winding # / type	Turns / Material / Gauge / Insulation Data
5 volt winding (5, 6 - 1, 2)	Two turns of 4 strands of #20HN spiral wound over 1 layer. Terminate 2 wires per pin at both start and finish as shown below.
+12 volt winding (12, 11 - 8, 7) - 12 volt winding (10 - 9)	Five turns of 5 strands of #20 HN with one strand a different color for the -12 V winding. Terminate the +12V windings at 2 wires per pin and the -12 V winding ends to just one pin as shown below.

Hipot: 200 V between all windings clusters.Vacuum varnish

Schematic



Lead Breakout / Pinout



MAGNETICS DESIGN DATA SHEET

Project / Customer: ON Semiconductor ATX project

Part Description: 3.3 V, 18 A output choke, 250 kHz, Rev. 2

Schematic ID: LX2

Core Type: E25/10/6 (E24-25)

Core Gap: 0.020" (0.51 mm) total; 10 mil thick paper across all legs

Inductance: 4.0 +/- 0.5 uH

Bobbin Type: Ferroxcube # E24-25PCB1-10 (10 pin horizontal mount)

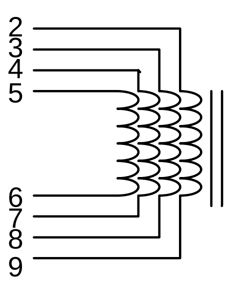
Windings (in order):

Winding # / type	Turns / Material / Gauge / Insulation Data
Pins 2, 3, 4, 5 to 6, 7, 8, 9 respectively	6 turns of 4 strands of #20HN wound quadrafilar on bobbin with ends terminated as shown in drawings below.

Vacuum varnish

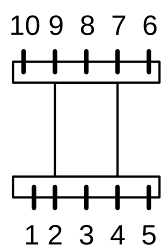
Hipot: NA

Schematic



Lead Breakout / Pinout

(top view)



Pins 1 and 10 not used

MAGNETICS DESIGN DATA SHEET

Project / Customer: ON Semiconductor - ATX Project

Part Description: 250 kHz forward converter transformer; 4 output, Rev. 2

Schematic ID: TX1

Core Type: PQ3230 (Ae = 1.6)

Core Gap: Gap to 550 to 650 uH

Inductance: 550 - 650 uH

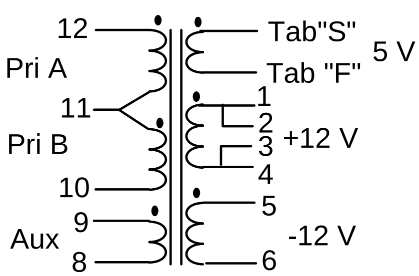
Bobbin Type: Vertical 12 pin pcb mount

Windings (in order):

Winding # / type	Turns / Material / Gauge / Insulation Data
"A" Primary	28 turns of 3 strands of #30HN over one layer; Self-leads to pins; insulate for 2.7 kV to next layer.
5 V Secondary	2 turns of 0.65" wide by 10 mil thick cu foil with cuffed ends. Terminate with copper tabs.
+12/-12 V Secondary	5 turns of 13 strands of #28HN with one strand being a different color for the -12 V winding. Self-leads to the pins with 6 strands per pin for the +12 V strands. Wind over 1 layer. Insulate for 2.7 kV to next winding.
"B" Primary	28 turns of 3 strands of #30HN over one layer. Self-leads to pins. Insulate for 1 kV to next layer.
Aux winding	3 turns of # 28HN spiral wound over "B" primary. Self-leads to pins.

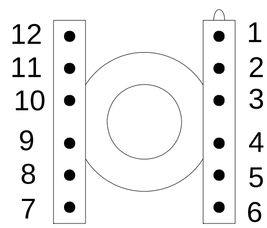
Hipot: 2.7 kV primary/aux to all secondaries. Vacuum varnish.

Schematic



Lead Breakout / Pinout

Bottom (pin side) view



MAGNETICS DESIGN DATA SHEET

Project / Customer: ON Semiconductor ATX Project

Part Description: Active clamp gate driver transformer; 250 kHz, Rev 2

Schematic ID: TX2

Core Type: Ferrite toroid; approx 0.4" dia (OD)

Core Gap: NA

Inductance: 1.5 mH nominal

Bobbin Type: 6 pin header; 0.4" x 0.4" (existing Mesa Power Systems design)

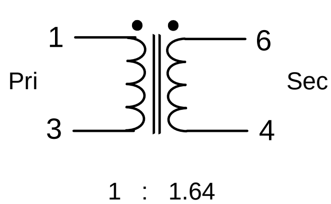
Windings (in order):

Winding # / type	Turns / Material / Gauge / Insulation Data
Primary (1 - 3)	25 turns of #30 insulated wire, spread evenly over entire core. Self-leads to pins.
Secondary (6 - 4)	41 turns of #32HN, spread evenly over entire core. Self-leads to pins.

Varnish or epoxy coat.

Hipot: 1.5 kV between pri and sec. Note: Both winding are on primary side circuit

Schematic



Lead Breakout / Pinout

Top View