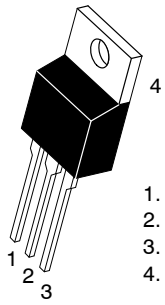
Plastic Medium-Power Complementary Silicon Transistors

TIP110, TIP111, TIP112 (NPN); TIP115, TIP116, TIP117 (PNP)

Designed for general−purpose amplifier and low−speed switching applications.



1. Base
2. Collector
3. Emitter
4. Collector

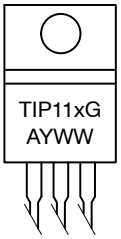
TO−220AB
CASE 221A
STYLE 1

DARLINGTON 2 AMPERE COMPLEMENTARY SILICON POWER TRANSISTORS 60−80−100 VOLTS, 50 WATTS

Features

- High DC Current Gain −
  h_{FE} = 2500 (Typ) @ I_C
  = 1.0 Adc
- Collector−Emitter Sustaining Voltage − @ 30 mAdc
  $V_{CEO(sus)}$ = 60 Vdc (Min) − TIP110, TIP115
  = 80 Vdc (Min) − TIP111, TIP116
  = 100 Vdc (Min) − TIP112, TIP117
- Low Collector−Emitter Saturation Voltage −
  $V_{CE(sat)}$ = 2.5 Vdc (Max) @ I_C
  = 2.0 Adc
- Monolithic Construction with Built−in Base−Emitter Shunt Resistors
- Pb−Free Packages are Available*−

MARKING DIAGRAM



TIP11x	= Device Code
x	= 0, 1, 2, 5, 6, or 7
A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 8.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MAXIMUM RATINGS

Symbol	Rating	TIP110, TIP115	TIP111, TIP116	TIP112, TIP117	Unit
V_{CEO}	Collector−Emitter Voltage	60	80	100	Vdc
V_{CB}	Collector−Base Voltage	60	80	100	Vdc
V_{EB}	Emitter−Base Voltage	5.0			Vdc
I_C	Collector Current − Continuous − Peak	2.0 4.0			Adc
I_B	Base Current	50			mAdc
P_D	Total Power Dissipation @ T_C = 25°C Derate above 25°C	50 0.4			W W/°C
P_D	Total Power Dissipation @ T_A = 25°C Derate above 25°C	2.0 0.016			W W/°C
E	Unclamped Inductive Load Energy − Figure 13	25			mJ
T_J, T_{stg}	Operating and Storage Junction	−65 to +150			°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Characteristics	Max	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Characteristic		Min	Max	Unit
OFF CHARACTERISTICS					
$V_{CEO(sus)}$	Collector−Emitter Sustaining Voltage (Note 1) (I_C = 30 mAdc, I_B = 0)	TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	 60 80 100	 − − −	Vdc
I_{CEO}	Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0) (V_{CE} = 40 Vdc, I_B = 0) (V_{CE} = 50 Vdc, I_B = 0)	 TIP110, TIP115 TIP111, TIP116 TIP112 ,TIP117	 − − −	 2.0 2.0 2.0	mAdc
I_{CBO}	Collector Cutoff Current (V_{CB} = 60 Vdc, I_E = 0) (V_{CB} = 80 Vdc, I_E = 0) (V_{CB} = 100 Vdc, I_E = 0)	 TIP110, TIP115 TIP111, TIP116 TIP112, TIP117	 − − −	 1.0 1.0 1.0	mAdc
I_{EBO}	Emitter Cutoff Current (V_{BE} = 5.0 Vdc, I_C = 0)		−	2.0	mAdc
ON CHARACTERISTICS (Note 1)					
h_{FE}	DC Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		 1000 500	 − −	−
$V_{CE(sat)}$	Collector−Emitter Saturation Voltage (I_C = 2.0 Adc, I_B = 8.0 mAdc)		−	2.5	Vdc
$V_{BE(on)}$	Base−Emitter On Voltage (I_C = 2.0 Adc, V_{CE} = 4.0 Vdc)		−	2.8	Vdc
DYNAMIC CHARACTERISTICS					
h_{fe}	Small−Signal Current Gain (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)		25	−	−
C_{ob}	Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz)	 TIP115, TIP116, TIP117 TIP110, TIP111, TIP112	 − −	 200 100	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

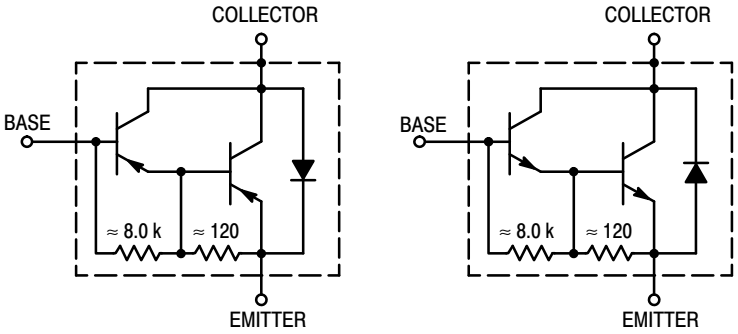


Figure 1. Darlington Circuit Schematic

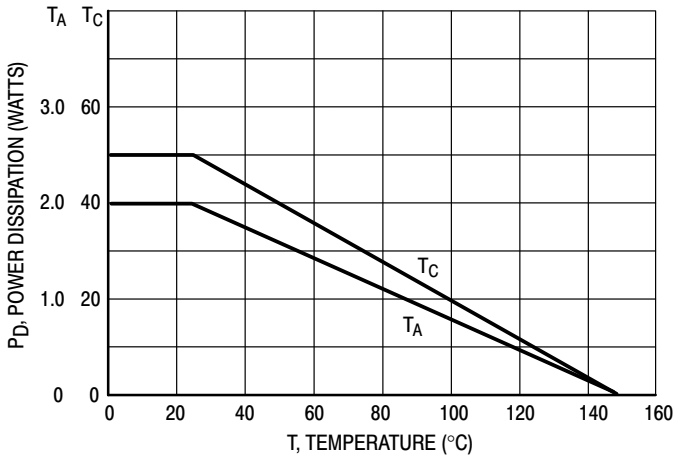


Figure 2. Power Derating

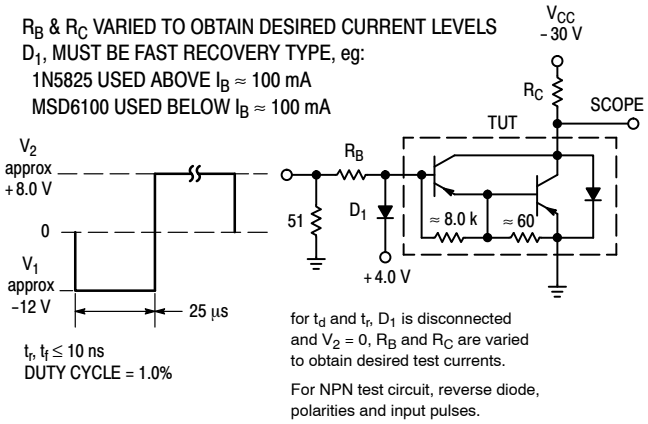


Figure 3. Switching Times Test Circuit

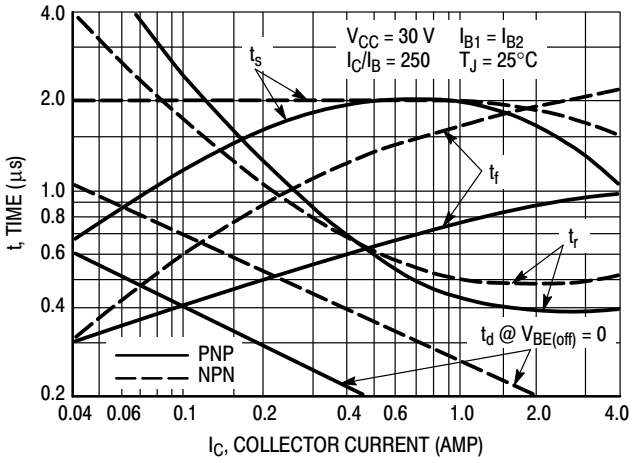


Figure 4. Switching Times

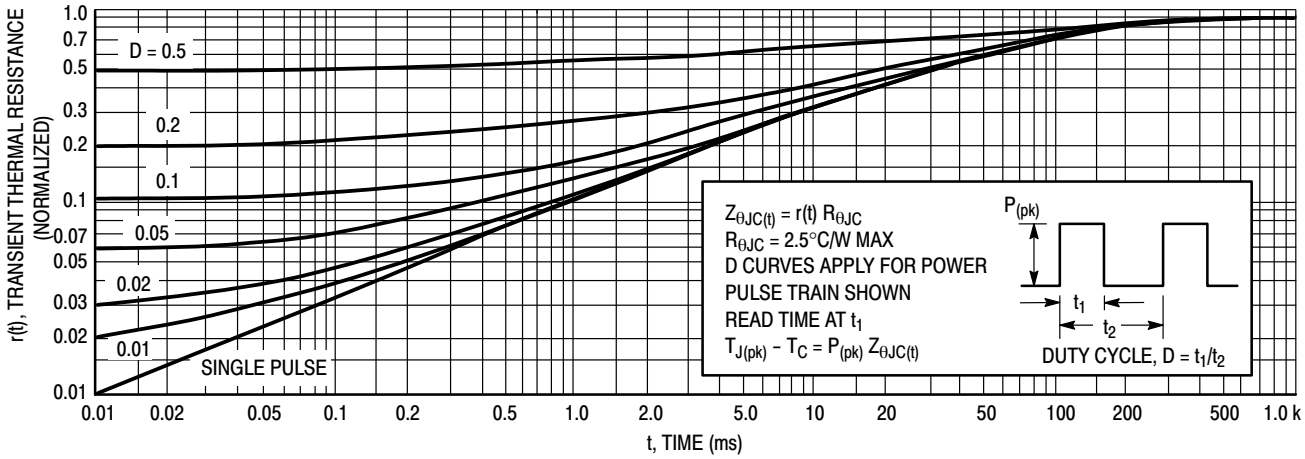


Figure 5. Thermal Response

ACTIVE−REGION SAFE−OPERATING AREA

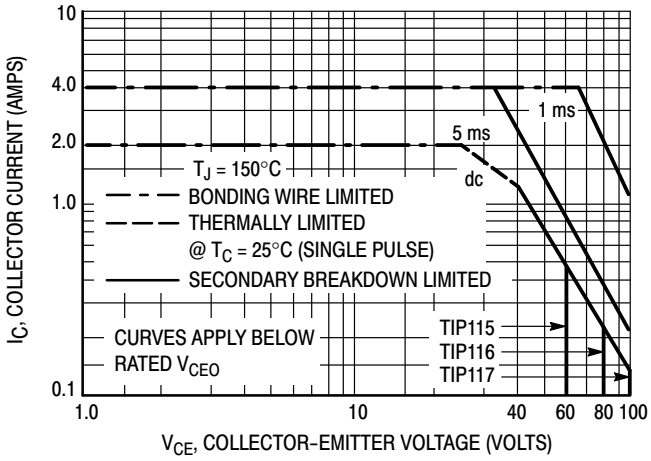


Figure 6. TIP115, 116, 117

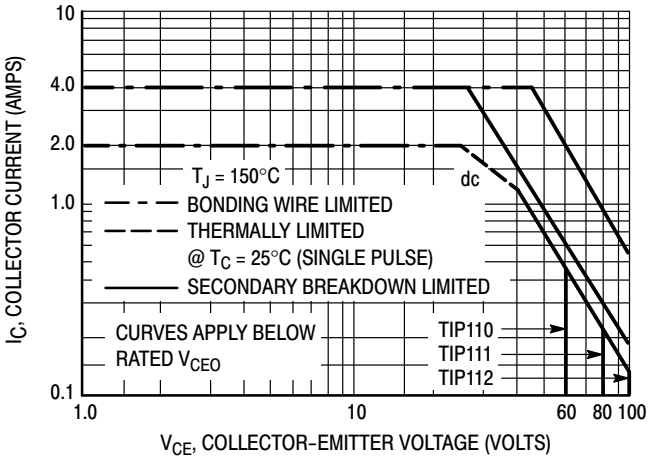


Figure 7. TIP110, 111, 112

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 6 and 7 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

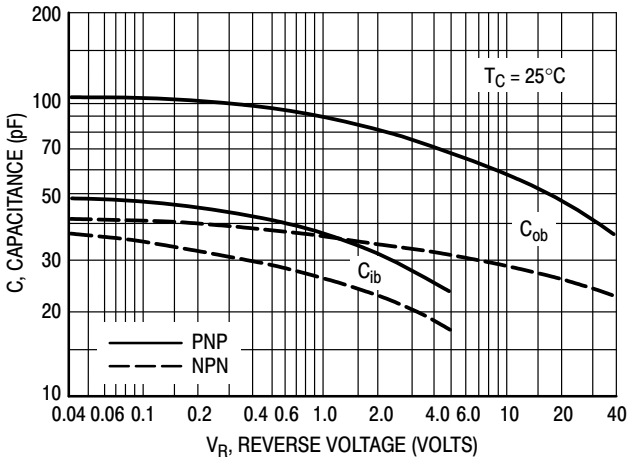


Figure 8. Capacitance

NPN
TIP110, 111, 112

PNP
TIP115, 116, 117

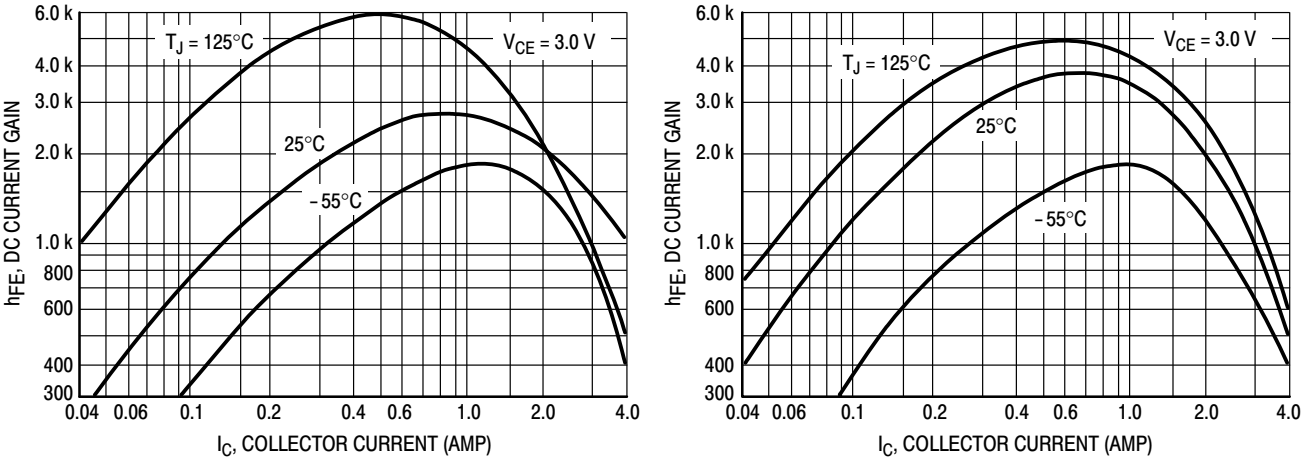


Figure 9. DC Current Gain

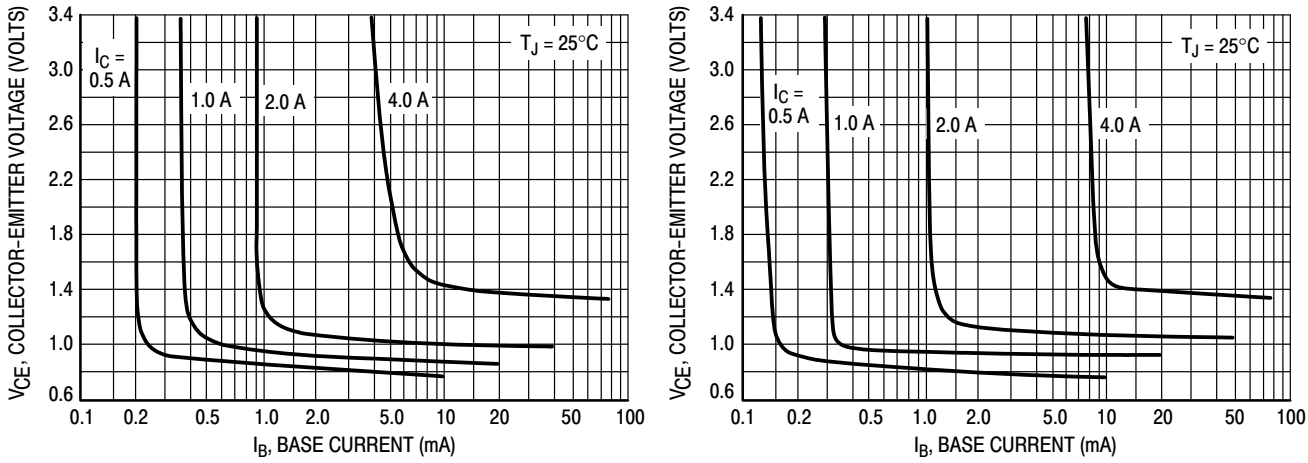


Figure 10. Collector Saturation Region

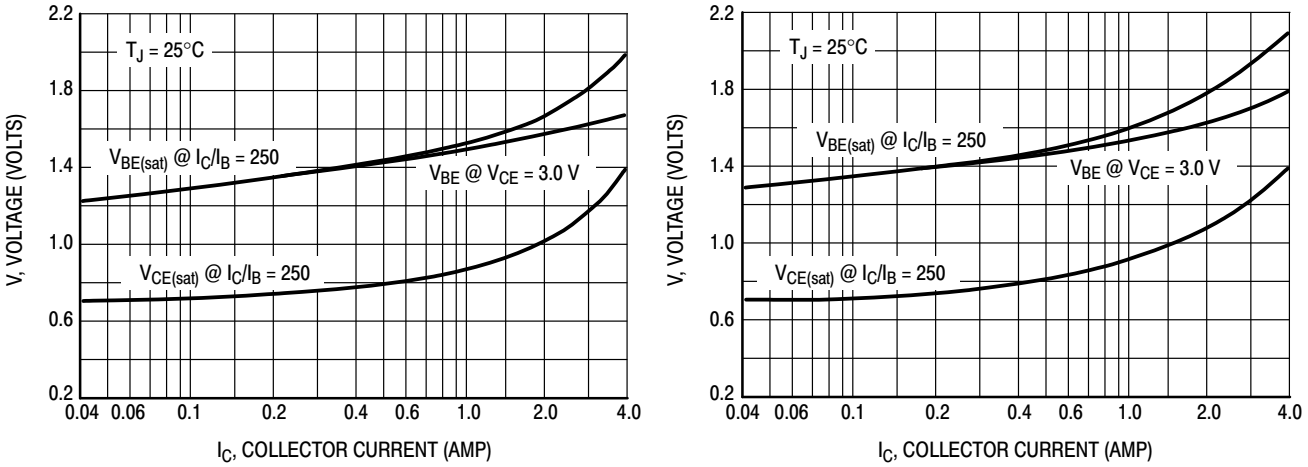
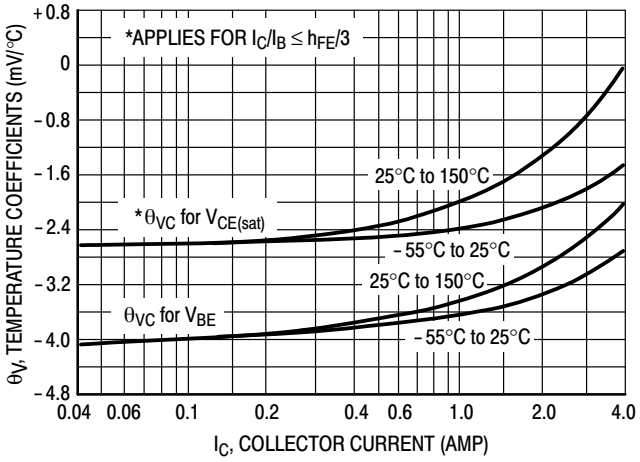


Figure 11. “On” Voltages

NPN
TIP110, 111, 112



PNP
TIP115, 116, 117

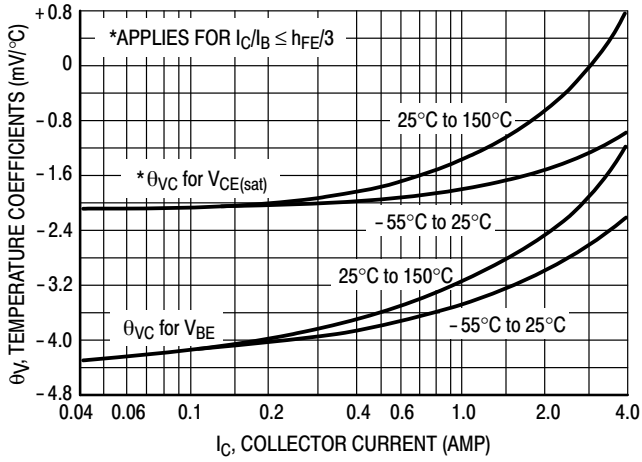
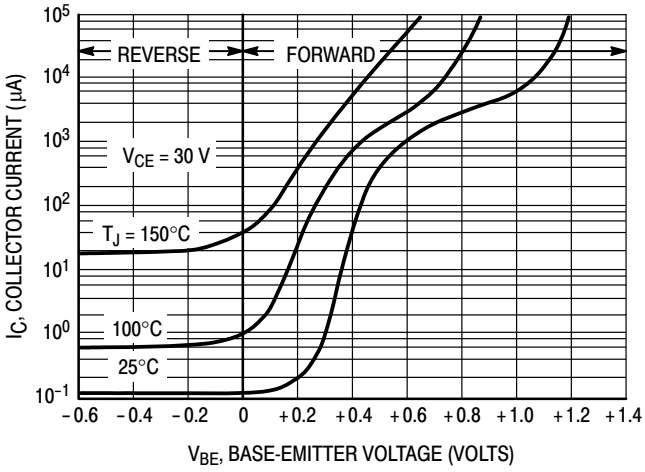


Figure 12. Temperature Coefficients



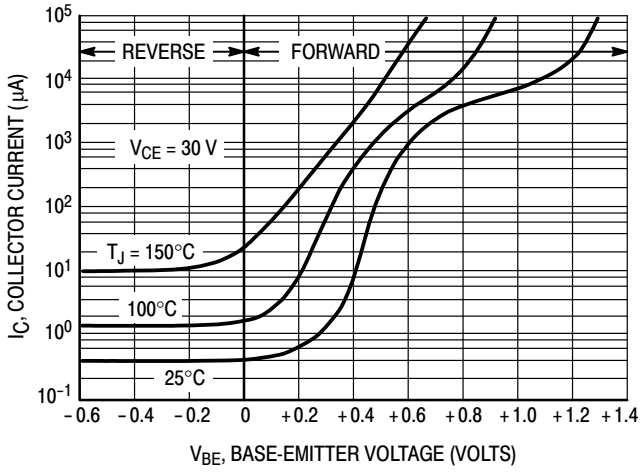
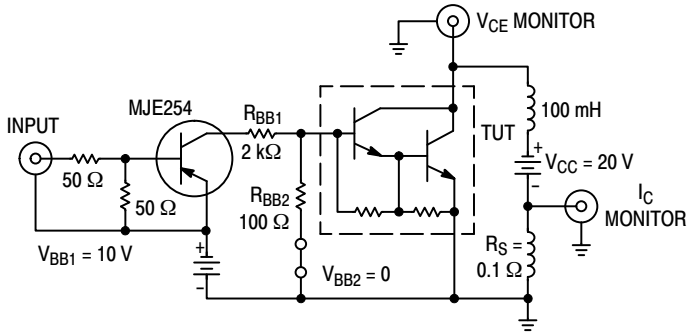
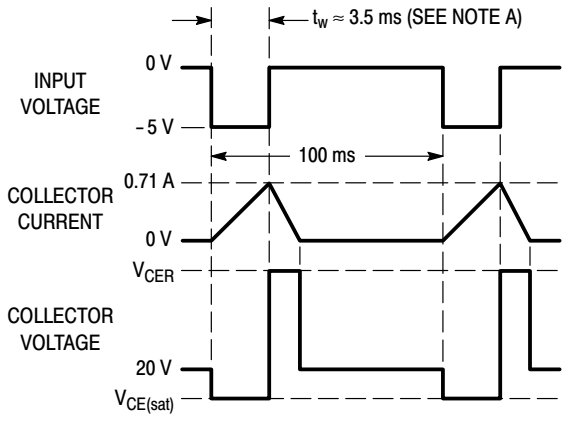


Figure 13. Collector Cut-Off Region

TEST CIRCUIT



VOLTAGE AND CURRENT WAVEFORMS



Note A: Input pulse width is increased until I_{CM} = 0.71 A,
NPN test shown; for PNP test
reverse all polarity and use MJE224 driver.

Figure 14. Inductive Load Switching

ORDERING INFORMATION

Device	Package	Shipping
TIP110G	TO−220 (Pb−Free)	50 Units / Rail
TIP111G	TO−220 (Pb−Free)	50 Units / Rail
TIP112G	TO−220 (Pb−Free)	50 Units / Rail
TIP115G	TO−220 (Pb−Free)	50 Units / Rail
TIP117G	TO−220 (Pb−Free)	50 Units / Rail

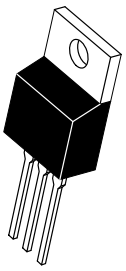
DISCONTINUED (Note 2)

TIP110	TO−220	50 Units / Rail
TIP111	TO−220	50 Units / Rail
TIP112	TO−220	50 Units / Rail
TIP115	TO−220	50 Units / Rail
TIP116	TO−220	50 Units / Rail
TIP117	TO−220	50 Units / Rail
TIP116G	TO−220 (Pb−Free)	50 Units / Rail

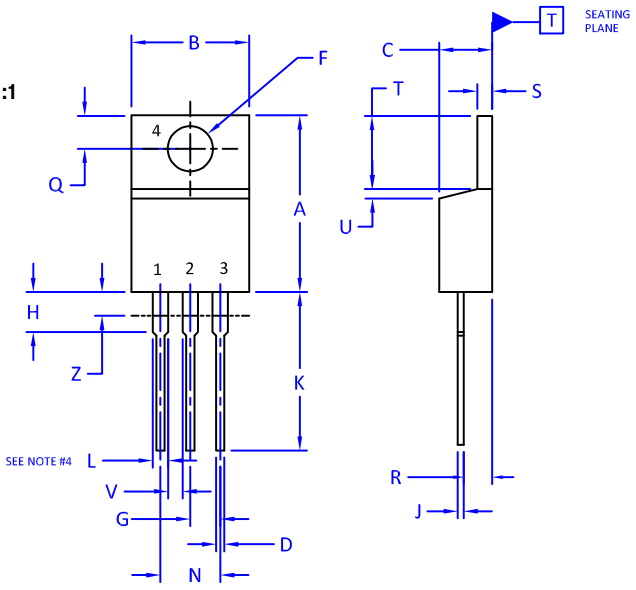
2. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

TO−220
CASE 221A
ISSUE AK

DATE 13 JAN 2022



SCALE 1:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	----	1.15	---
Z	----	0.080	---	2.04

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. BASE
2. EMITTER
3. COLLECTOR
4. EMITTER

STYLE 3:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 4:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. MAIN TERMINAL 2

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 8:
PIN 1. CATHODE
2. ANODE
3. EXTERNAL TRIP/DELAY
4. ANODE

STYLE 9:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 10:
PIN 1. GATE
2. SOURCE
3. DRAIN
4. SOURCE

STYLE 11:
PIN 1. DRAIN
2. SOURCE
3. GATE
4. SOURCE

STYLE 12:
PIN 1. MAIN TERMINAL 1
2. MAIN TERMINAL 2
3. GATE
4. NOT CONNECTED

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