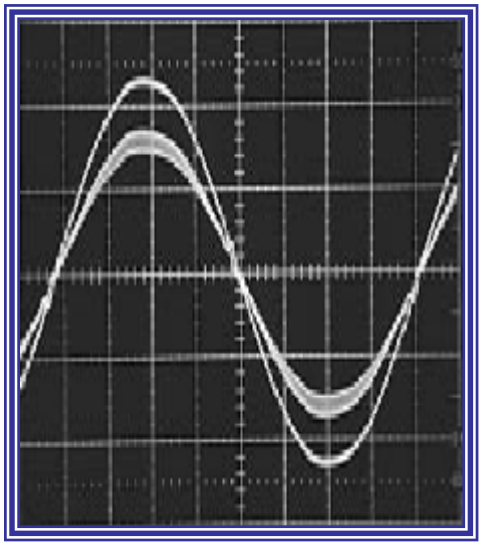
安森美半导体
ON Semiconductor®

先进的功率因数校正

Advanced Power Factor Correction

议程 Agenda

- 引言 Introduction
  - 功率因数校正的基本解决方案 Basic solutions for power factor correction
  - 要满足的新需求 New needs to address
- 交错式的功率因数校正 Interleaved PFC
  - 基本的特征 Basic characteristics
  - 分立的解决方案 A discrete solution
  - 性能 Performance
- 无桥PFC Bridgeless PFC
  - 为什么我们应当关注输入桥路
    Why should we care of the input bridge?
  - 主要的解决方案 Main solutions
  - Ivo Barbi解决方案 Ivo Barbi solution
  - 宽市电的800 W应用的性能 Performance of a wide mains, 800 W application
- 结论 Conclusion



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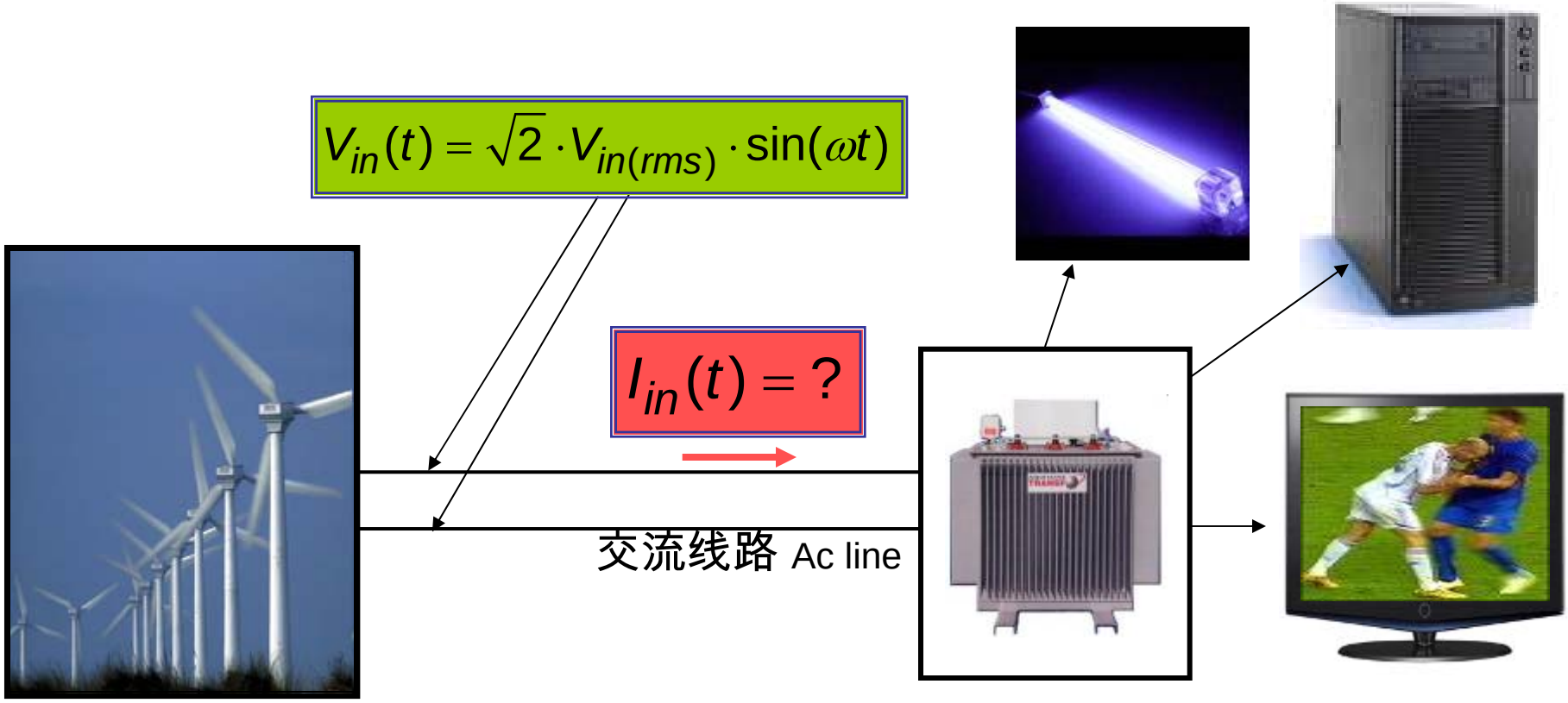
Harmonic	Class-A Amp	Class-B Amp	Class-C % of Fund	Class-D mA/Watt
2	1.08	1.62	2	
3	2.30	3.45	30*PF	3.4
4	0.43	0.65		
5	1.44	2.16	10	1.9
6	0.30	0.45		
7	0.77	1.12	7	1
8	0.23	0.35		
9	0.40	0.60	5	0.5
10	0.18	0.28		
11	0.33	0.50	3	0.35
12	0.15	0.23		
13	0.21	0.32	3	0.296
14/40 (even)	1.84/n	2.76/n		
15/39 (odd)	2.25/n	3.338/n	3	3.85/n

Table -1 EN/IEC61000-3-2 Harmonic current limits

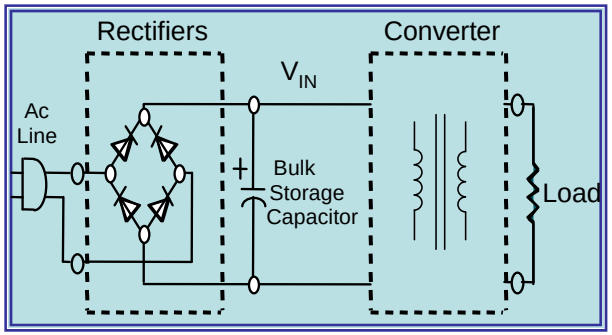
为什么要进行功率因数校正 Why implement PFC?



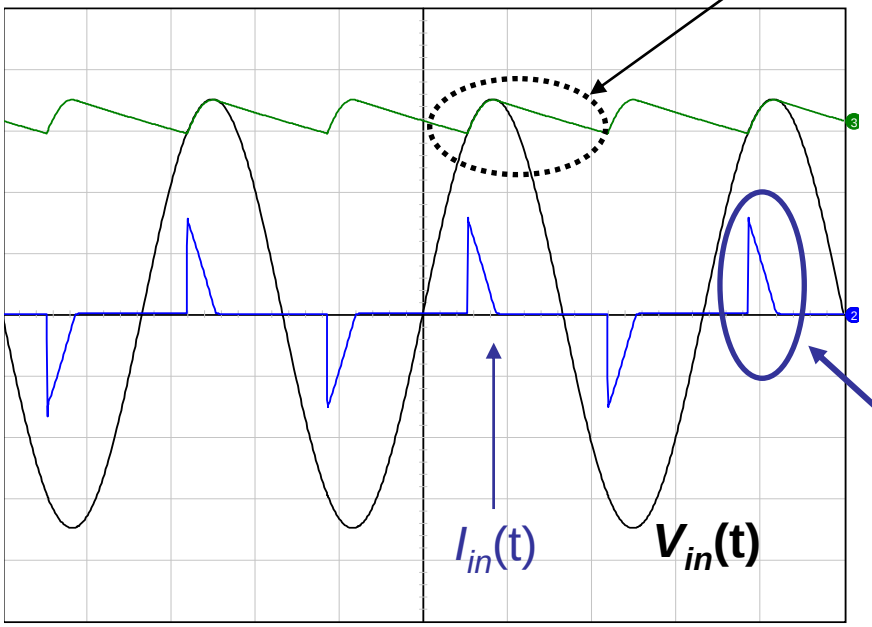
- 市电供电设施提供了一个正弦电压 The mains utility provides a sinusoidal voltage $V_{in}(t)$.
- $I_{in}(t)$的形状和相位取决于负载 The shape and phase of $I_{in}(t)$ depend on the load.

交流线路整流导致电流尖峰…

AC Line Rectification Leads to Current Spikes…



当$V_{in}(t) > V_{out}$时，C_{bulk}充电
C_{bulk} is refueled when $V_{in}(t) > V_{out}$



高电流尖峰
High current spike!

- 只有基波分量产生有功功率 Only the fundamental component produces real power
- 谐波电流毫无用处地循环(无功功率) Harmonic currents circulate uselessly (reactive power)
- 线电流有效值增加 The line rms current increases

太高的有效值电流!... Too High rms Currents!...

❑ 高有效值电流会降低输出端口的容量

High rms currents reduce outlet capability

n°1
- $P_{in(avg)}$ = 119 W, $V_{in(rms)}$ = 85 V
- $I_{in(rms)}$ = 2.5 A

n°2
- $P_{in(avg)}$ = 119 W, $V_{in(rms)}$ = 85 V
- $I_{in(rms)}$ = 1.4 A

PF = 0.56

PF = 1.00

相同功率 (W)
Same power (W)

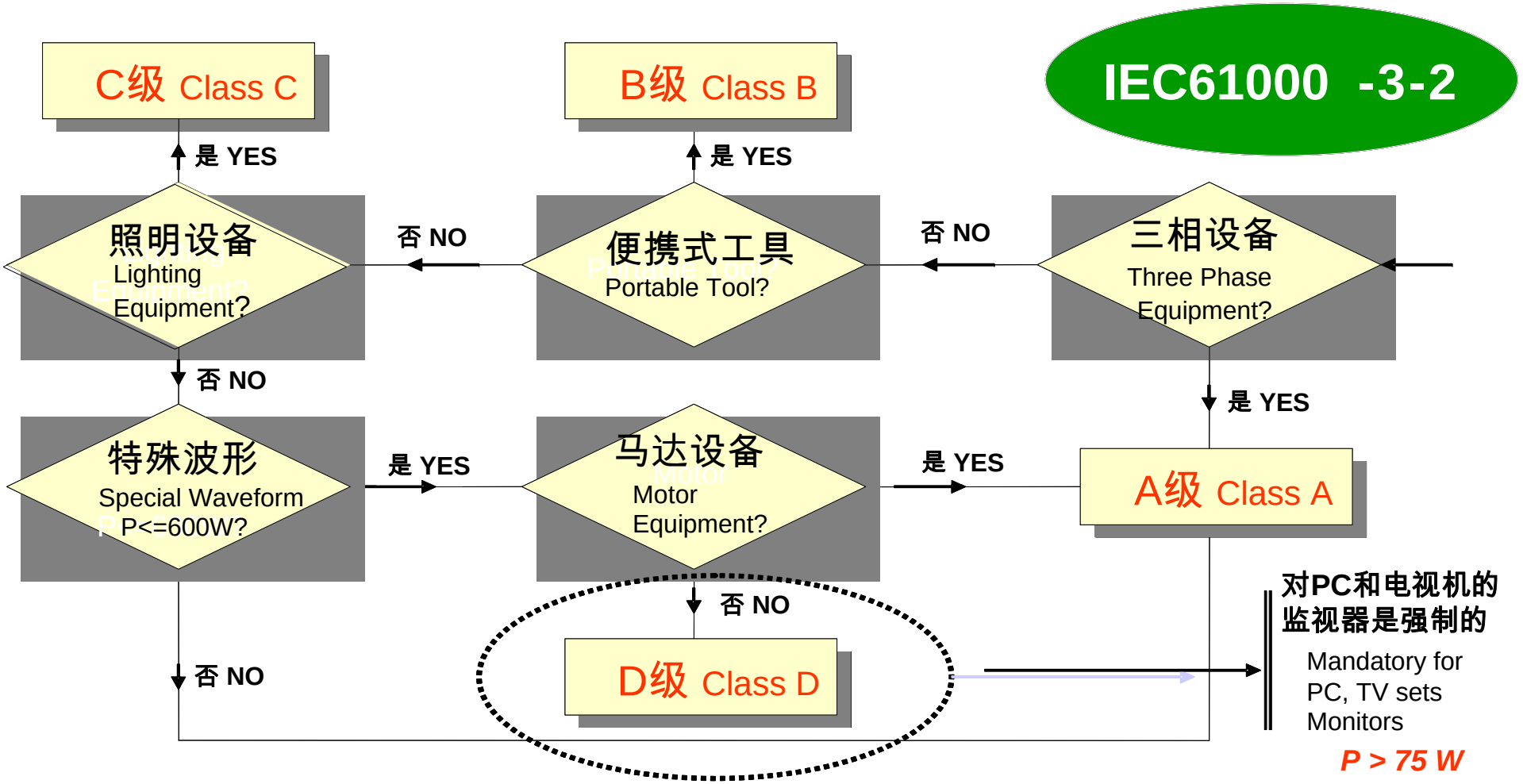
n°1 ← 16/2.5 = **6** 监视器 monitors

n°2 ← 16/1.4 = **11** 电阻 resistors

$$I_{in(rms)} = \frac{P_{in(avg)}}{V_{in(rms)} \cdot PF}$$

$(I_{in(rms)})_{max}$ = 16 A

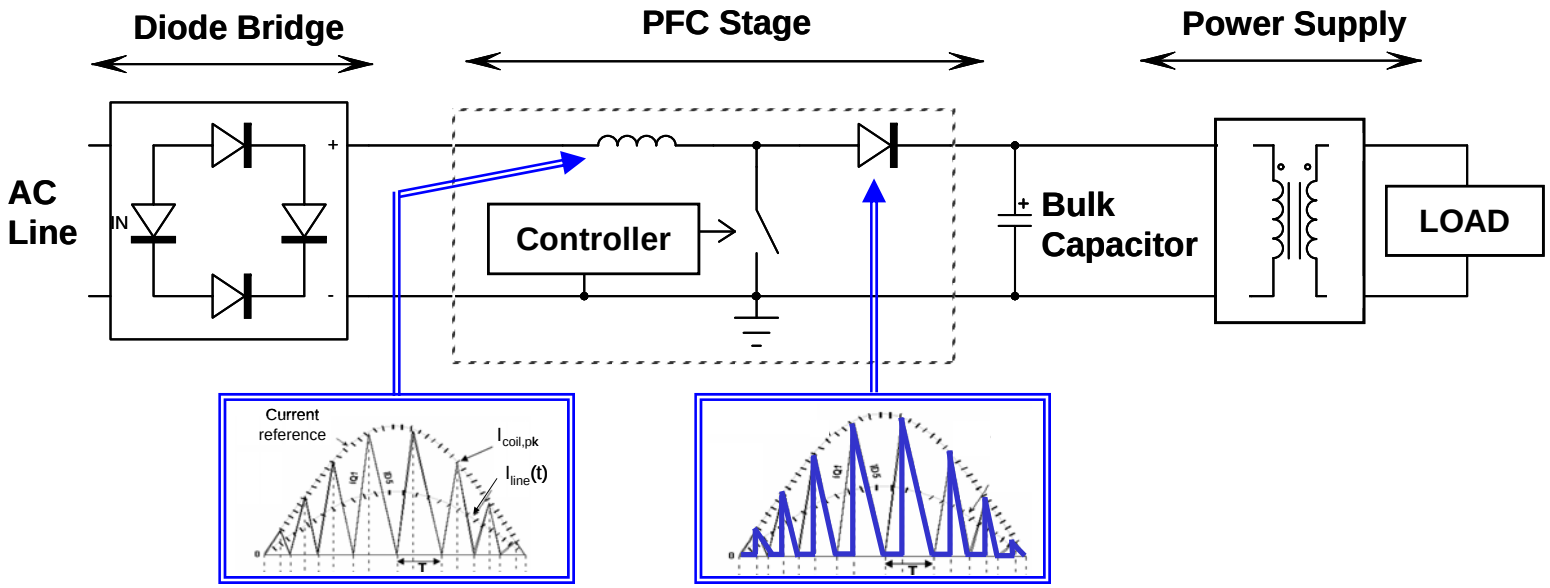
功率因数标准 Power Factor Standard



- 标准规定了谐波的最大级别数量为39

  The standard specifies a maximum level up to harmonic 39

需要一个功率因数校正段
Need for a PFC Stage



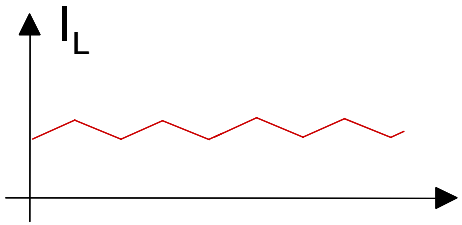
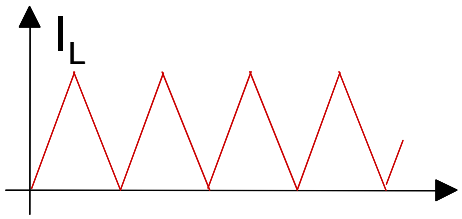
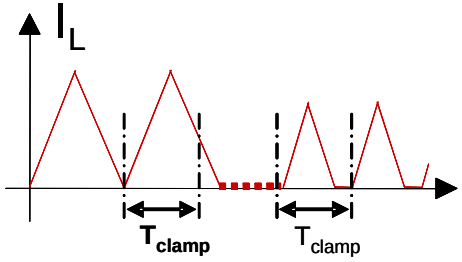
- 升压预转换器从线路抽取正弦电流以提供一个直流电压(bulk电压)

  A boost pre-converter draws a sinusoidal current from the line to provide a dc voltage (bulk voltage)
- 线圈内的电流通过以下两种方式被正弦化：The current within the coil is made sinusoidal by:
  - 迫使它遵照一个正弦基准(电流模式) Forcing it to follow a sinusoidal reference (current mode)
  - 适当地控制占空比(电压模式) Controlling the duty-cycle appropriately (voltage mode)

工作模式概述 Operating modes overview

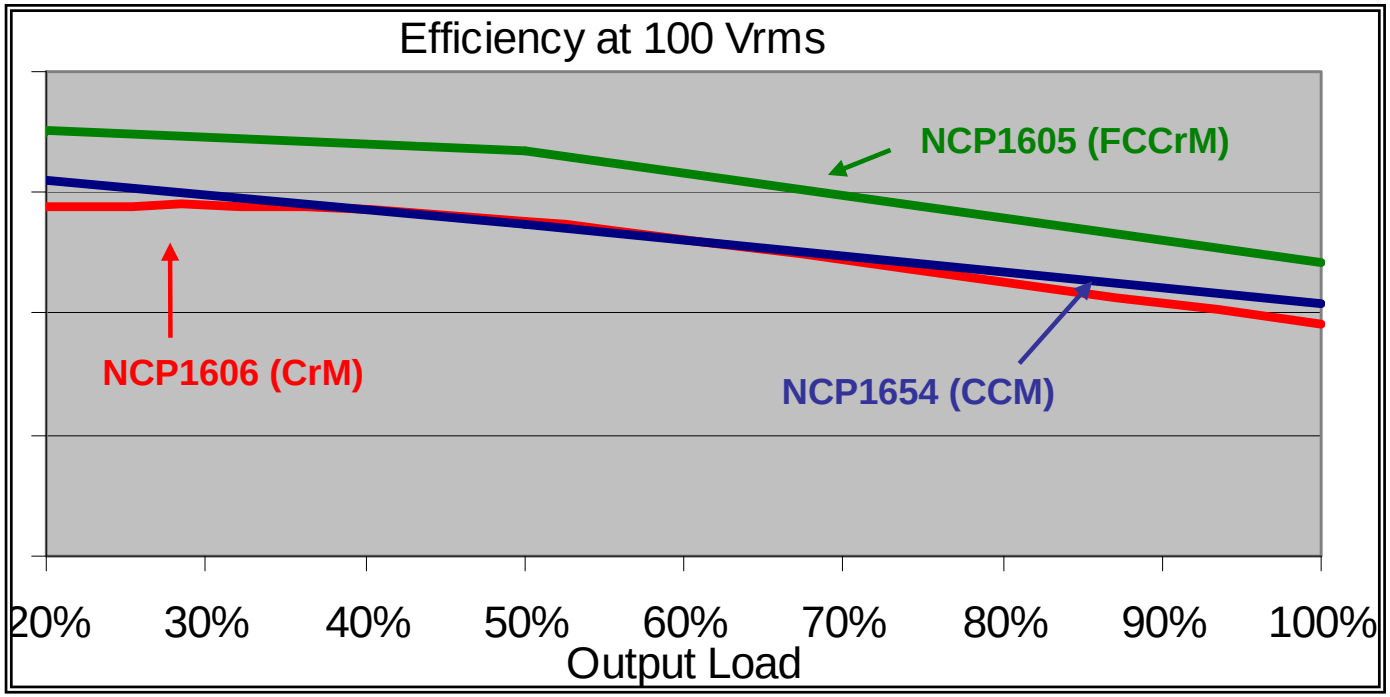
- 安森美半导体提供三种模式的解决方案

  ON Semiconductor offers solutions for three modes

	工作模式 Operating Mode	主要特征 Main Feature
	连续导通模式 Continuous Conduction Mode(**CCM**)	总是硬开关 Always hard-switching 电感值最大 Inductor value is largest 有效值电流最小 Minimized rms current **例如: NCP1654**
	临界导通模式 Critcial Conduction Mode(**CrM**)	有效值电流大 Large rms current 开关平率不固定 Switching frequency is not fixed **例如: NCP1606**
	频率钳制临界导通模式 Frequency Clamped Critcial Conduction Mode(**FCCrM**)	有效值电流大 Large rms current 频率被限制 Frequency is limited 线圈电感减小 Reduced coil inductance **例如：NCP1605**

FCCrM：一种高效的模式 FCCrM: an Efficient Mode

- 频率钳制临界导通模式似乎是最高效的解决方案 Frequency Clamped CrM seems the most efficient solution
- 300 W、宽市电输入的PFC的效率测量如下：Efficiency of a 300 W, wide mains PFC has been measured:



完整的研究结果将刊登在2009年一季度出版的PFC手册修订本上
The complete study will be published in the PFC handbook revision that will be released in Q1 2009.

要满足的新需求 New Needs to Address

- ATX电源所需的高效率： High efficiency for ATX power supplies:
  - 在以下负载点测量效率：Efficiency is measured at:
    - 20 % $P_{out(max)}$
    - 50 % $P_{out(max)}$
    - 100 % $P_{out(max)}$

- 纤薄型液晶电视 Slim LCD TVs:
  - 元器件高度受限制 Components height is limited

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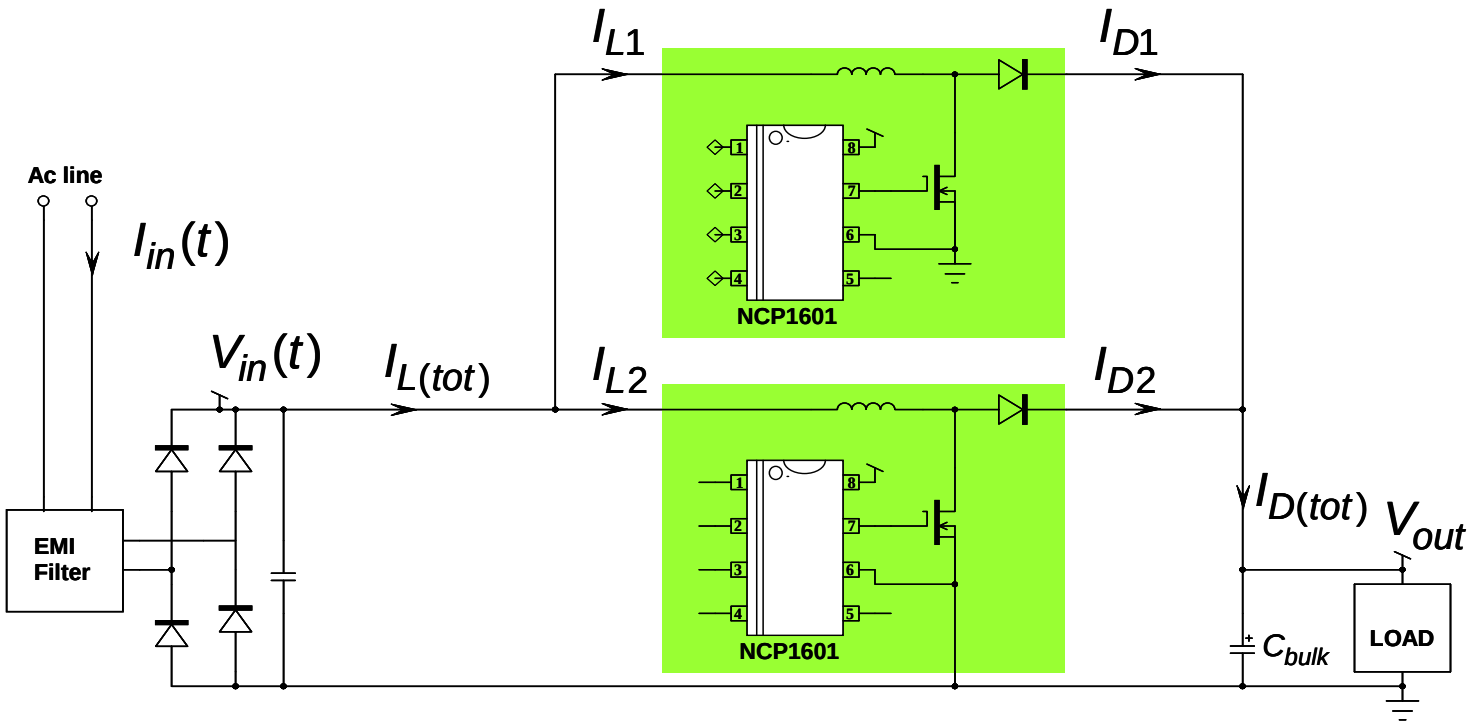
交错式的PFC Interleaved PFC

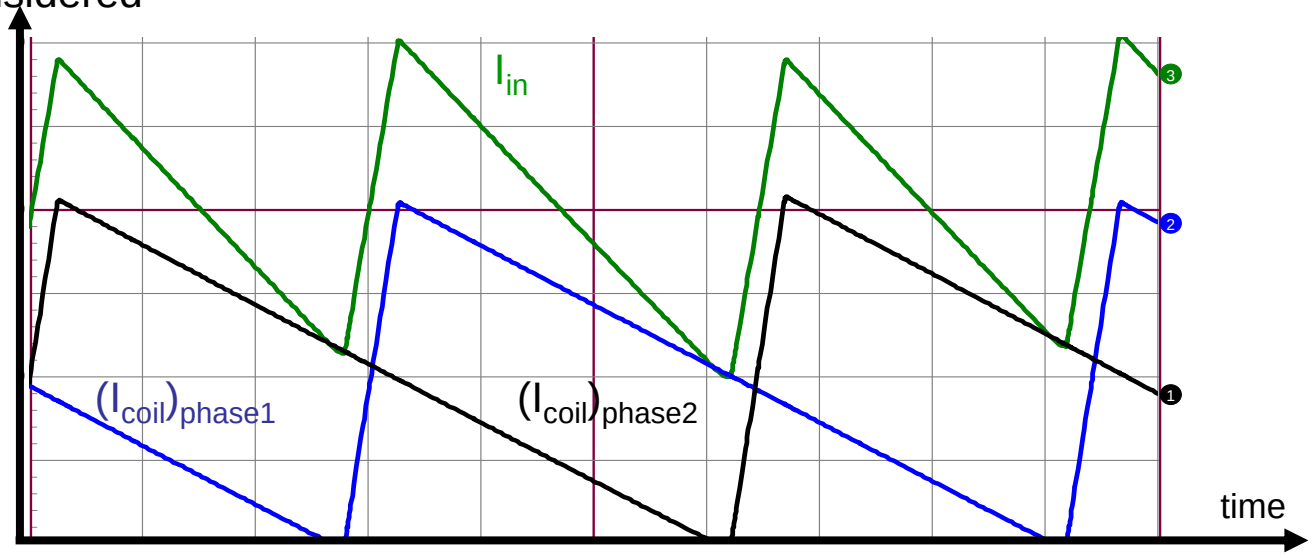
- 产生($P_{in(avg)}$/2)的两个小PFC段代替一个单一的大PFC段 Two small PFC stages delivering ($P_{in(avg)}$ / 2) in lieu of a single big one



- 如果两个相位为异相，则会使电流($I_{L(tot)}$)和($I_{D(tot)}$)纹波极大地减小 If the two phases are out-of-phase, the resulting currents ($I_{L(tot)}$) and ($I_{D(tot)}$) exhibit a dramatically reduced ripple.

交错式的好处 Interleaved Benefits

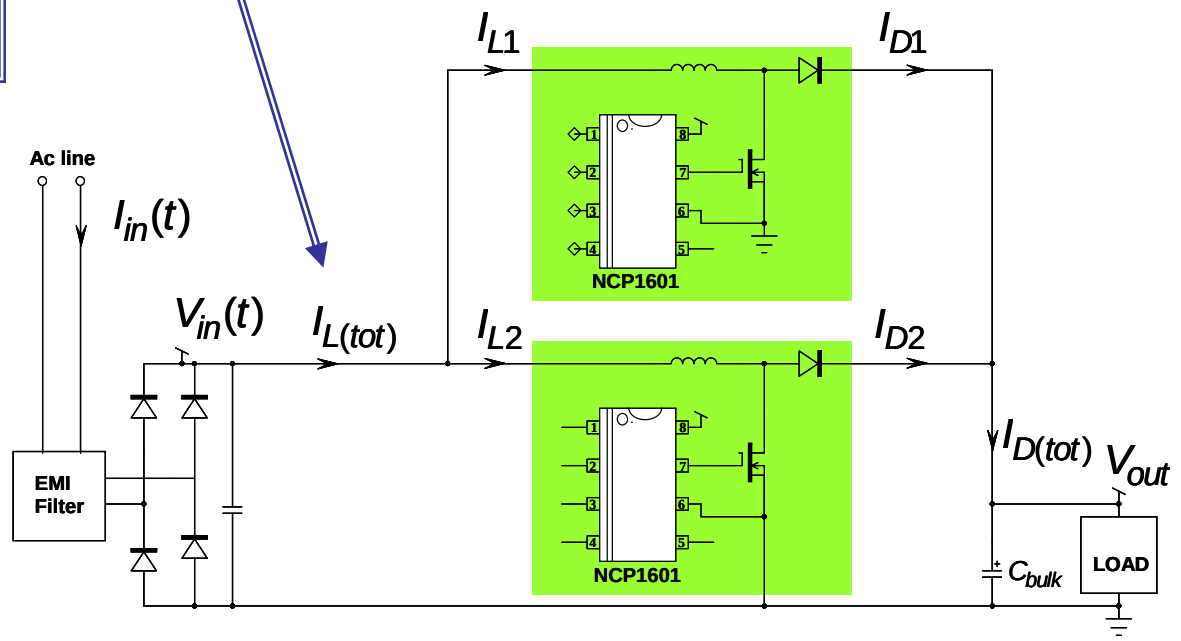
- 需要更多元器件但是： More components but:
  - 150 W的PFC比300 W的PFC更容易设计 A 150 W PFC is easier to design than a 300 W one
  - 模块化的方案 Modular approach
  - 两个非连续导通模式(DCM) PFC就像一个CCM PFC转换器 Two DCM PFCs look like a CCM PFC converter…
    - 使EMI滤波更容易且减小了输出有效值电流 Eases EMI filtering and reduces the output rms current
- 只有DCM PFC交错式方案将推崇 Only interleaving of DCM PFCs will be considered



输入电流纹波 Input Current Ripple

什么是$I_{L(tot)}$总输入电流的纹波

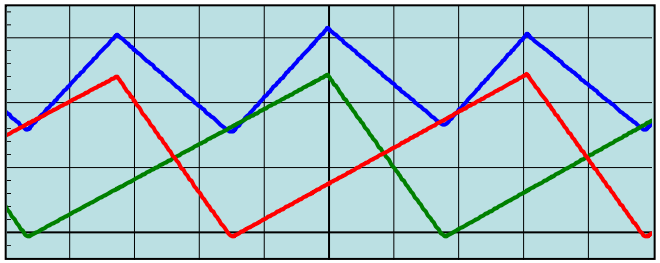
What is the ripple of the $I_{L(tot)}$ total input current?



计算输入电流纹波 Computing the Input Current Ripple

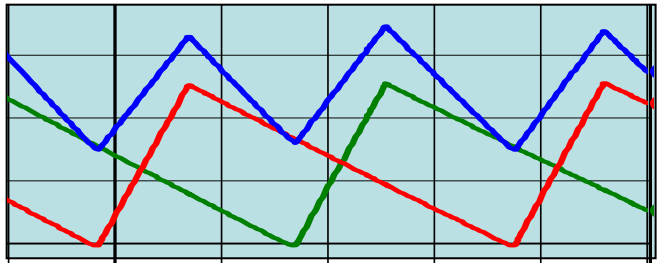
- 假设如下：Let's assume that:
  - V_{in} 和开关时段在几个周期内是不变的 V_{in} and the switching period are constant over few cycles
  - 两个分支以临界导通模式工作 The two branches operate in CrM
- 这里有两种情况： There are two cases:
  - **$V_{in}<V_{out}/2$ (或者 or d>0.5)**:

    两者开关时段的导通时间重叠。输入电流在导通间隔的结尾达到峰值 The on-times of the two phases overlap. The input current peaks at the end of the conduction intervals.



  - **$V_{in}>V_{out}/2$ (或者 or d<0.5)**:

    这里没有重叠但输入电流仍在每个导通时间的结尾达到峰值 There is no overlap but still, the input current peaks at the end of the each conduction time



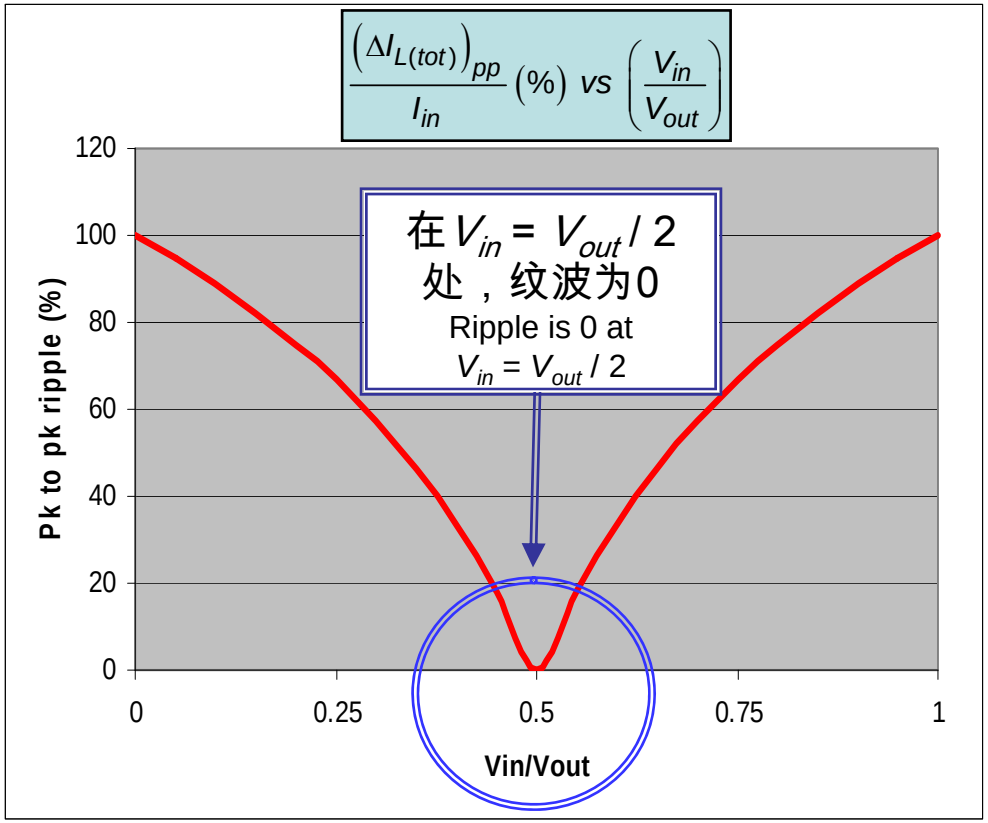
- 使用公式 $\left(d=\frac{t_{on}}{T_{sw}}=1-\frac{V_{in}}{V_{out}}\right)$ 我们可以得出电流纹波值 Using $\left(d=\frac{t_{on}}{T_{sw}}=1-\frac{V_{in}}{V_{out}}\right)$, we can derive the current ripple

最终，... Finally,...

	$V_{in}(t) \le \frac{V_{out}}{2}$	$V_{in}(t) \ge \frac{V_{out}}{2}$
平均输入电流 (线电流) Averaged input current (line current)	$I_{in}(t) = \langle I_{L(tot)} \rangle_{T_{sw}} = \frac{V_{in}}{R_{in}} = \frac{V_{in} \cdot P_{in(avg)}}{V_{in(rms)}^2}$	
峰峰值纹波 Peak to peak ripple	$\left(\Delta I_{L(tot)}\right)_{pp} = I_{in} \cdot \left(1 - \frac{V_{in}}{V_{out} - V_{in}}\right)$	$\left(\Delta I_{L(tot)}\right)_{pp} = I_{in} \cdot \left(2 - \frac{V_{out}}{V_{in}}\right)$
峰值电流包络 Peak Current envelop	$\left(I_{L(tot)}\right)_{pk} = 2 \cdot I_{in} \cdot \left(1 - \frac{V_{out}}{4 \cdot (V_{out} - V_{in})}\right)$	$\left(I_{L(tot)}\right)_{pk} = 2 \cdot I_{in} \cdot \left(1 - \frac{V_{out}}{4 \cdot V_{in}}\right)$
谷值电流包络 Valley Current envelop	$\left(I_{L(tot)}\right)_{v} = I_{in} \cdot \frac{V_{out}}{2 \cdot (V_{out} - V_{in})}$	$\left(I_{L(tot)}\right)_{v} = \frac{P_{in(avg)} \cdot V_{out}}{2 \cdot V_{in(rms)}^2}$

输入电流的峰峰值纹波

Peak to Peak Ripple of the Input Current

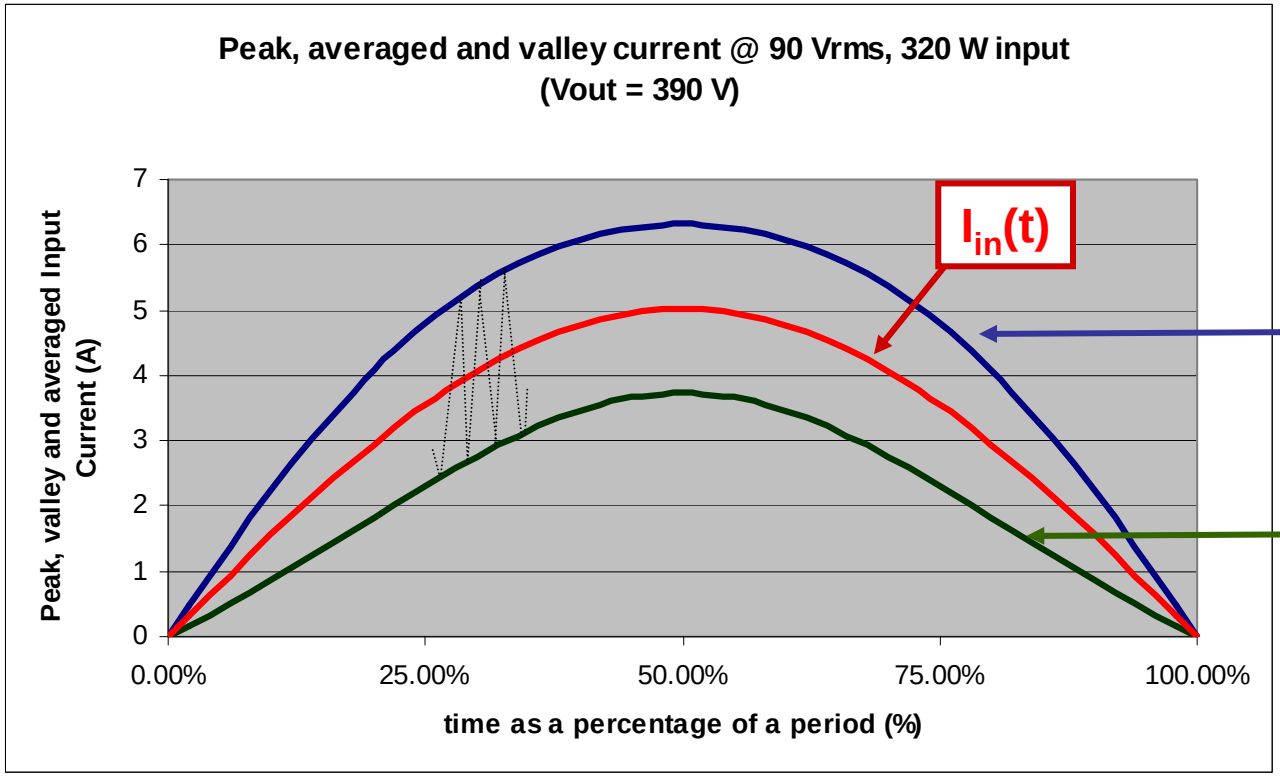


- 输入纹波仅取决于(V_{in}/V_{out})的比值 The input ripple only depends on the ratio (V_{in}/V_{out}):
- 不像在连续导通模式中 Unlike in CCM：
  - 电感不起作用 L plays no role
  - 纹波百分比不会取决于负载

    The ripple percentage does not depend on the load
- 在低压线路(V_{in}/V_{out}=0.3)中，纹波为+/-28%(在正弦曲线的顶点，假设相移为180°工作在临界导电模式下) At low line (V_{in}/V_{out} = 0.3), the ripple is +/-28% (at the sinusoid top, assuming 180° phase shift and CrM operation)

低压线路的输入纹波 Input Current Ripple at Low Line

- 当V_{in}保持低于V_{out}/2时 ，输入电流就像连续导通模式阻尼PFC的电流
  When V_{in} remains lower than V_{out} / 2, the input current looks like that of a CCM, hysteretic PFC
- $I_{L(tot)}$在两个近似正弦曲线的包络线之间振荡
  ($I_{L(tot)}$) swings between two nearly sinusoidal envelops

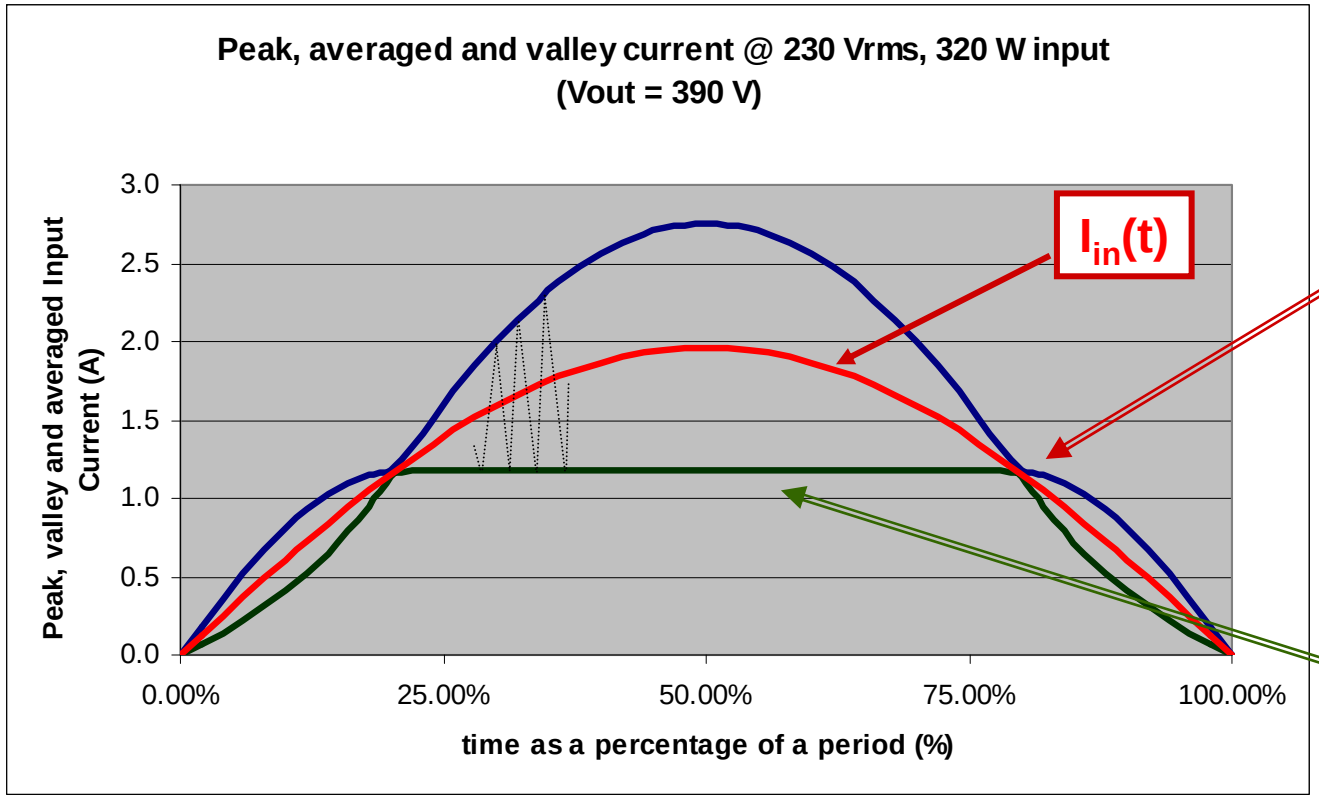


峰值电流包络线
Envelop for the peak currents

谷值电流包络线
Envelop for the valley currents

高压线路的输入电流纹波 Input Current Ripple at High Line

- 当V_{in}超过(V_{out}/2)时, 谷值电流是恒定的! When V_{in} exceeds (V_{out} / 2), the valley current is constant!
- 它等于$\left(\frac{V_{out}}{2 \cdot R_{in}}\right)$, 是PFC输入阻抗 It equates $\left(\frac{V_{out}}{2 \cdot R_{in}}\right)$ where R_{in} is the PFC input impedance

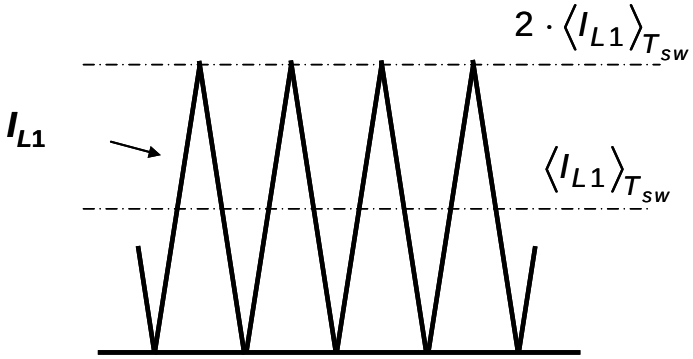


当$V_{in}=V_{out}/2$时
无纹波
No ripple when
$V_{in} = V_{out} / 2$

$$\frac{P_{in(avg)} \cdot V_{out}}{2 \cdot V_{in(rms)}^{2}} = \frac{V_{out}}{2 \cdot R_{in}}$$

线路输入电流 Line Input Current

- 对于每个分支，在正弦波的某处 For each branch, somewhere within the sinusoid:



- 两个平均的正弦相电流之和就是总线电流 The sum of the two averaged, sinusoidal phases currents gives the total line current:

$$I_{in} = \left\langle I_{L(tot)} \right\rangle_{\frac{T_{sw}}{2}} = \langle I_{L1} \rangle_{T_{sw}} + \langle I_{L2} \rangle_{T_{sw}}$$

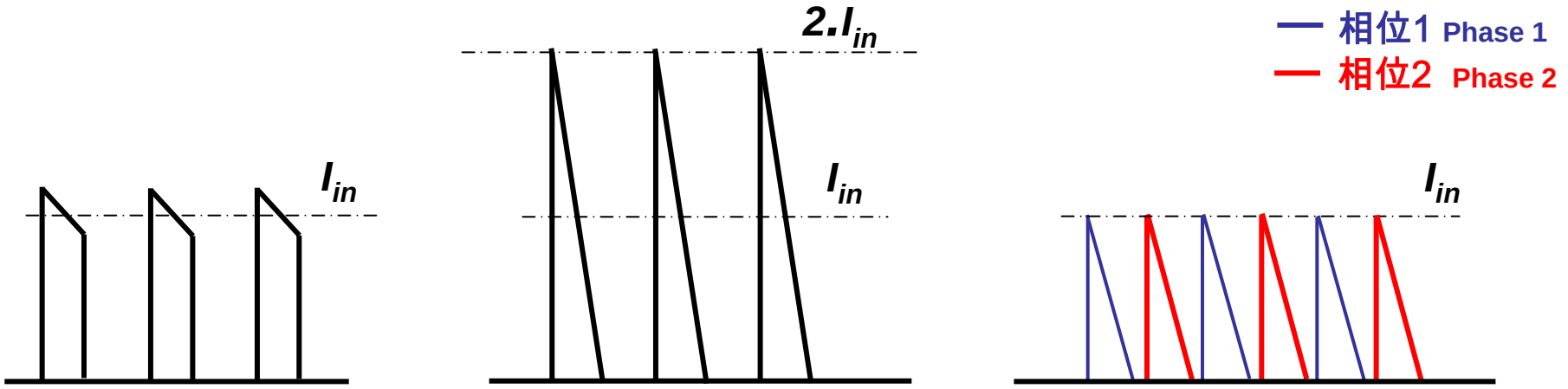
- 假设存在完美的电流平衡 Assuming a perfect current balancing:

$$2 \cdot \langle I_{L1} \rangle_{T_{sw}} = 2 \cdot \langle I_{L2} \rangle_{T_{sw}} = I_{in}$$

- **每个分支的峰值电流就是 I_{in}(t)**
  The peak current in each branch is I_{in}(t)

充电电流的交流成分 AC Component of the Refueling Current

- 充电电流(输出二极管电流)与工作模式相关：The refueling current (output diode(s) current) depends on the mode:



单相CCM Single phase CCM

T_{sw}时间内的有效值
rms value over T_{sw}

$$I_{in} \cdot \sqrt{\frac{V_{in}}{V_{out}}}$$

单相CrM Single phase CrM

T_{sw}时间内的有效值
rms value over T_{sw}

$$\frac{2}{\sqrt{3}} \cdot I_{in} \sqrt{\frac{V_{in}}{V_{out}}}$$

交错式CrM Interleaved CrM

T_{sw}时间内的有效值
rms value over T_{sw}

$$\sqrt{\frac{2}{3}} \cdot I_{in} \sqrt{\frac{V_{in}}{V_{out}}}$$

减小了大电容有效值电流

A Reduced Rms Current in the Bulk Capacitor

- 正弦曲线整合带来(电阻性负载)：Integration over the sinusoid leads to (resistive load):

	单相CCM PFC Single phase CCM PFC	单相CrM或FCCrM PFC Single phase CrM or FCCrM PFC	交错式CrM或FCCrM PFC Interleaved CrM or FCCrM PFC
二极管有效值电流($I_{D(rms)}$) Diode(s) rms current ($I_{D(rms)}$)	$\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$	$\frac{2}{\sqrt{3}}\cdot\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$	$\sqrt{\frac{2}{3}}\cdot\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}}$
电容有效值电流($I_{C(rms)}$) Capacitor rms current ($I_{C(rms)}$)	$\sqrt{\frac{8\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{3\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$	$\sqrt{\frac{32\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{9\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$	$\sqrt{\frac{16\sqrt{2}\cdot\left(\frac{P_{out}}{\eta}\right)^2}{9\pi\cdot V_{in(rms)}\cdot V_{out}}-\left(\frac{P_{out}}{V_{out}}\right)^2}$
300-W, V_{out}=390V $V_{in(rms)}$=90 V	$I_{D(rms)}$ = 1.9 A $I_{C(rms)}$ = 1.7 A	$I_{D(rms)}$ = 2.2 A $I_{C(rms)}$ = 2.1 A	$I_{D(tot)(rms)}$ = 1.5 A $I_{C(rms)}$ = 1.3 A

- 交错式极大地减小了有效值电流 Interleaving dramatically reduces the rms currents
  - ➔ 从而减少了损耗、发热，提高了可靠性 **reduced losses, lower heating, increased reliability**

总结 Summary

	Single FCCrM stage		Interleaved FCCrM stage		Single CCM stage	
	General	300-W, wide mains	General	300-W, wide mains	General	300-W, wide mains
$\Delta I_{in(max)}$ (A)	Independent on L	10.0 A	Independent on L	2.6 A	Depends on L	2.6 A (at 90 V_{rms}, full load if L = 250 µH)
Inductor	1 coil 	75 µH $I_{L,pk(max)}$ = 10 A $I_{L,rms(max)}$ = 4.1 A $L*I_{pk}^2$ = 7.5 mJ	2 coils 	150 µH $I_{L,pk(max)}$ = 5.0 A $I_{L,rms(max)}$ = 2.0 A $L*I_{pk}^2$ = 3.7 mJ	1 coil 	250 µH $I_{L,pk(max)}$ = 6.3 A $I_{L,rms(max)}$ = 3.5 A $L*I_{pk}^2$ = 9.9 mJ
Total MOSFET conduction losses (with below MOSFETs)	$\frac{4 \cdot R_{DS(on)}}{3} \cdot \left(\frac{P_{in(avg)}}{V_{in(rms)}}\right)^2 \cdot \left(1 - \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi \cdot V_{out}}\right)\right)$	4.6 W	$\frac{2 \cdot R_{DS(on)}}{3} \cdot \left(\frac{P_{in(avg)}}{V_{in(rms)}}\right)^2 \cdot \left(1 - \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi \cdot V_{out}}\right)\right)$	4.6 W	$R_{DS(on)} \cdot \left(\frac{P_{in(avg)}}{V_{in(rms)}}\right)^2 \cdot \left(1 - \left(\frac{8\sqrt{2} \cdot V_{in(rms)}}{3\pi \cdot V_{out}}\right)\right)$	3.5 W
MOSFETs		1 * SPP20N60 or 2* SPP11N60		2 * SPP11N60		1 * SPP20N60 or 2* SPP11N60
Diode	Ultrafast	MUR550 (TO220) 	2 * Ultrafast	2 * MUR550 (axial) 	Low t_{rr} diode	High speed diode (SiC..) 
$I_{C(rms)(max)}$ (A)	$\sqrt{\frac{32\sqrt{2} \cdot \left(\frac{P_{out}}{\eta}\right)^2}{9\pi \cdot V_{in(rms)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}}\right)^2}$	2.0	$\sqrt{\frac{16\sqrt{2} \cdot \left(\frac{P_{out}}{\eta}\right)^2}{9\pi \cdot V_{in(rms)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}}\right)^2}$	1.3	$\sqrt{\frac{8\sqrt{2} \cdot \left(\frac{P_{out}}{\eta}\right)^2}{3\pi \cdot V_{in(rms)} \cdot V_{out}} - \left(\frac{P_{out}}{V_{out}}\right)^2}$	1.7
EMI complexity	DM: high CM: moderate		DM: moderate CM: moderate		DM: moderate CM: high	
Characteristics	Compact design		Low profile designs		Compact design	

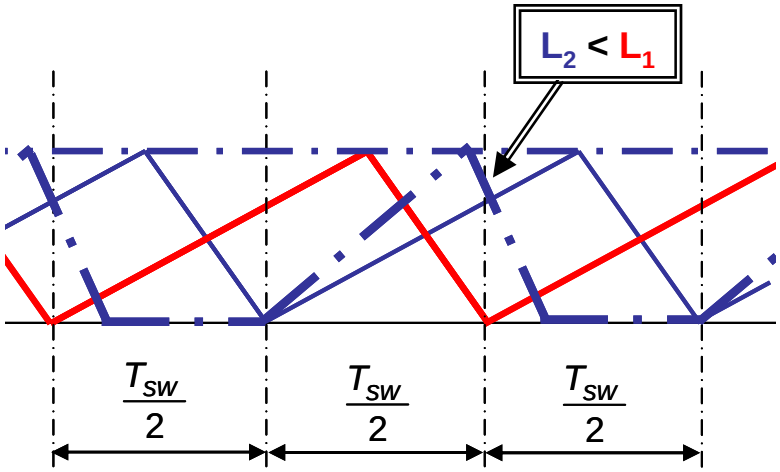
Compared to CrM, FCCrM allows the use of smaller inductances (due to frequency clamp)
The inductance for the single and interleaved FCCrM stages is based on a 130 kHz frequency clamp (high frequency design).
The switching frequency is also supposed to be 130 kHz for the CCM stage.

议程 Agenda

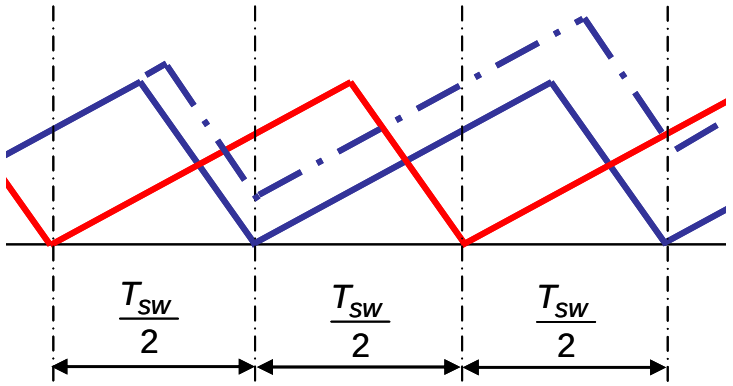
- 引言 Introduction
  - 功率因数校正的基本解决方案 Basic solutions for power factor correction
  - 要满足的新需求 New needs to address
- **交错式的功率因数校正** Interleaved PFC
  - 基本的特征 Basic characteristics
  - **分立的解决方案** A discrete solution
  - 性能 Performance
- 无桥PFC Bridgeless PFC
  - 为什么我们应当关注输入桥路
    Why should we care of the input bridge?
  - 主要的解决方案 Main solutions
  - Ivo Barbi解决方案 Ivo Barbi solution
  - 广域的800 W应用的性能 Performance of a wide mains, 800 W application
- 结论 Conclusion

交错式：主/从方案… Interleaving: Master/Slave Approach…

- 主分支自由地工作 The master branch operates freely
- 从分支遵照180°相移 The slave follows with a 180°phase shift
- 主要挑战：保持CrM工作模式(无CCM、无死区)Main challenge: maintaining the CrM operation (no CCM, no dead-time)



电流模式：电感不平衡
Current mode: inductor unbalance

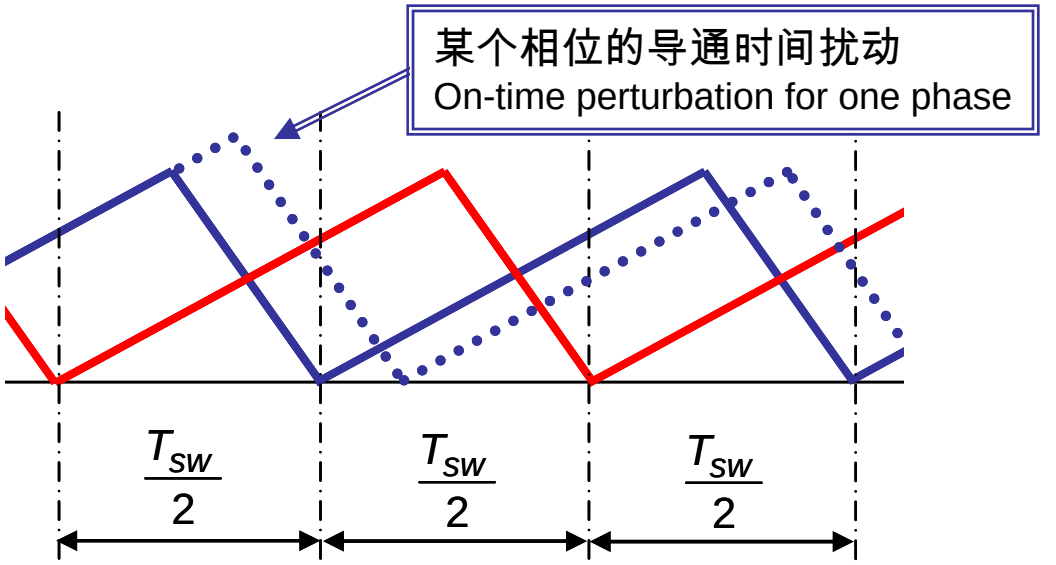


电压模式：导通时间移动
Voltage mode: on-time shift

交错式：独立相位方案 Interleaving:

Independent Phases Approach…

- 每个相位恰当地工作于CrM或FCCrM模式 Each phase properly operates in CrM or FCCrM.
- 两个分支相互配合以设定180°相移 The two branches interact to set the 180° phase shift
- 主要的挑战：保持准确的相移 Main challenge: to keep the proper phase shift



CrM工作模式可保持但导通时间的一个扰动可以使180°相移偏位
CrM operation is maintained but a perturbation of the on-time may degrade the 180°phase shift

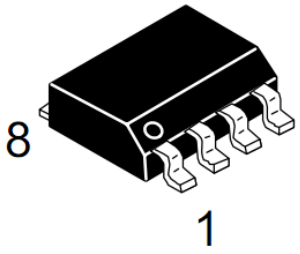
- **我们选择了这种方案 We selected this approach**

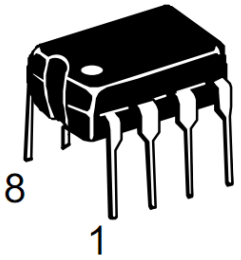
双NCP1601方案的总体原理

General

Principle on a Two-NCP1601 Solution

- 该解决方案基于由安森美半导体开发的一种独特机制—频率钳制临界导电模式(NCP1601) The solution lies on the Frequency Clamp Critical Conduction mode, unique scheme developed by ON Semiconductor (NCP1601)





- 两个NCP1601 驱动两个独立的PFC分支：Two NCP1601 drive two independent PFC branches:
  - 辅助绕组用于检测每个分支的磁芯复位 Auxiliary windings are used to detect the core reset of each branch
  - 过流保护时，两个级共享电流采样The current sensing is shared by the two stages for protection only (Over Current Limitation)

- 两个分支工作于电压模式 The two branches are operating in voltage mode

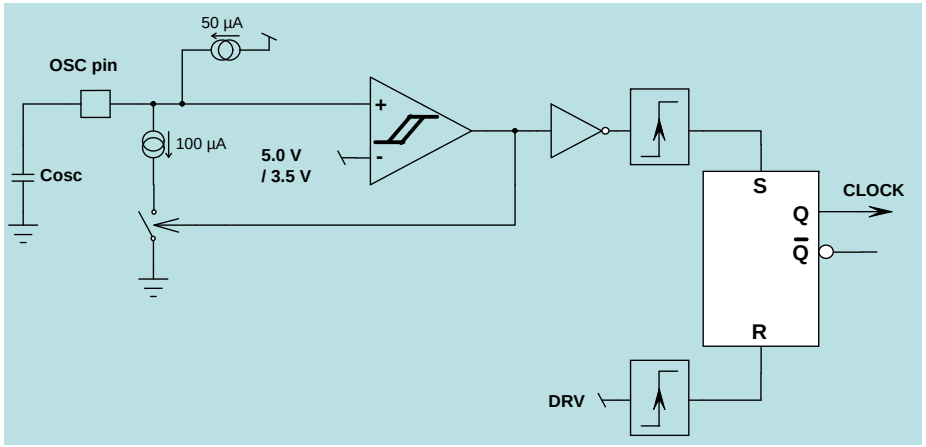
同步：主要挑战 Synchronization: the Main Challenge

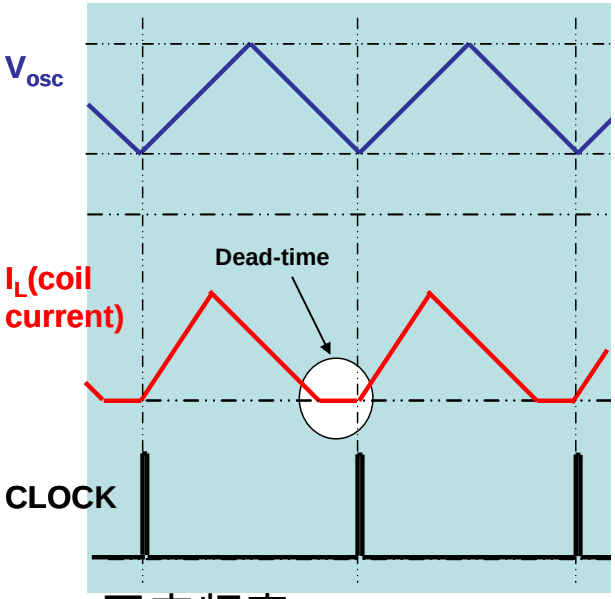
- 一个驱动器(DRV2)同步两个分支以致： One driver (DRV2) synchronizes the two branches so that:
  - 分支1 (DRV1)直到时间t过去后才能变为高 Branch 1 (DRV1) cannot turn high until a time t has elapsed
  - 分支2 (DRV2)在2t内不能指挥一个新的导通相位 Branch 2 (DRV2) cannot dictate a new conduction phase within 2t
- 因此： Hence:
  - 在固定频率工作模式中，每个分支的开关时间为2t ，两个相位天生是交错式的

    In fixed frequency operation, the switching period for each branch is 2t and the two phases are naturally interleaved
  - 在CrM模式中，开关频率是由电流周期强制决定的，必须使异相稳固

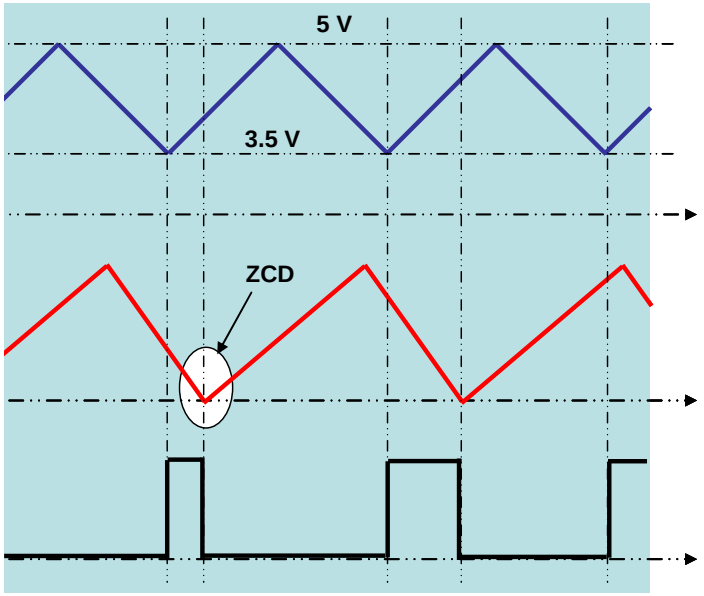
    In CrM, the switching frequency is that imposed by the current cycle (T_{sw}>2t) and must stabilize out of phase.
- 相位补偿电路包含可能的漂移(可登录www.onsemi.com参考2008年第四季度推出的详细的应用笔记) Possible slippages are contained by a phase compensation circuitry (refer to www.onsemi.com for detailed AN available in Q4 2008).

NCP1601 的同步性能 NCP1601 Synchronization Capability





固定频率 Fixed Frequency

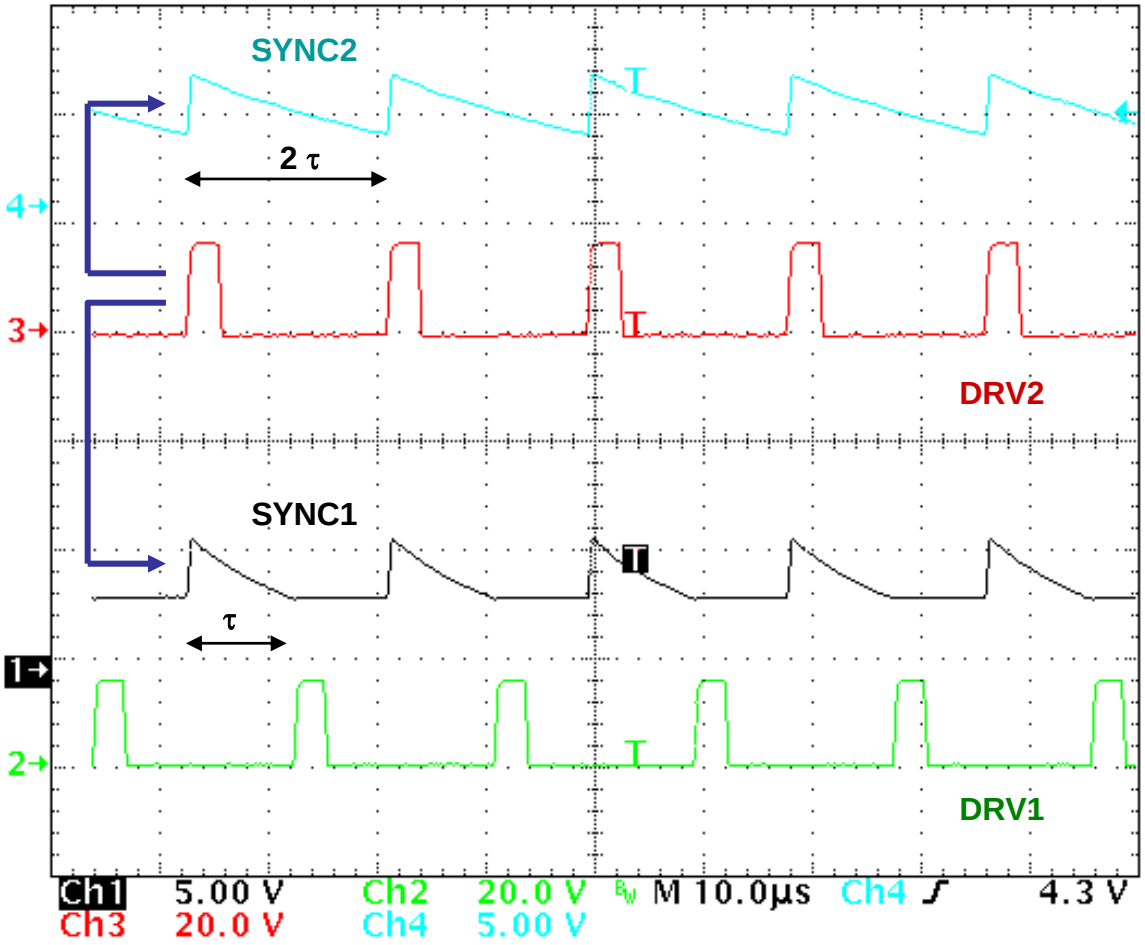


临界导电模式 Critical Conduction Mode

- 振荡器在3.5和5 V之间振荡 The oscillator oscillates between 3.5 and 5 V
- 当振荡器走向低于5 V时，NCP1601产生一个时钟 The NCP1601 generates a clock when the oscillator goes below 3.5 V
- 时钟信号被储存直到零电流被检测到 The clock signal is stored until ZCD is detected

工作于230 V_{rms}，中等负载情况

Operation @ 230 V_{rms}, Medium Load

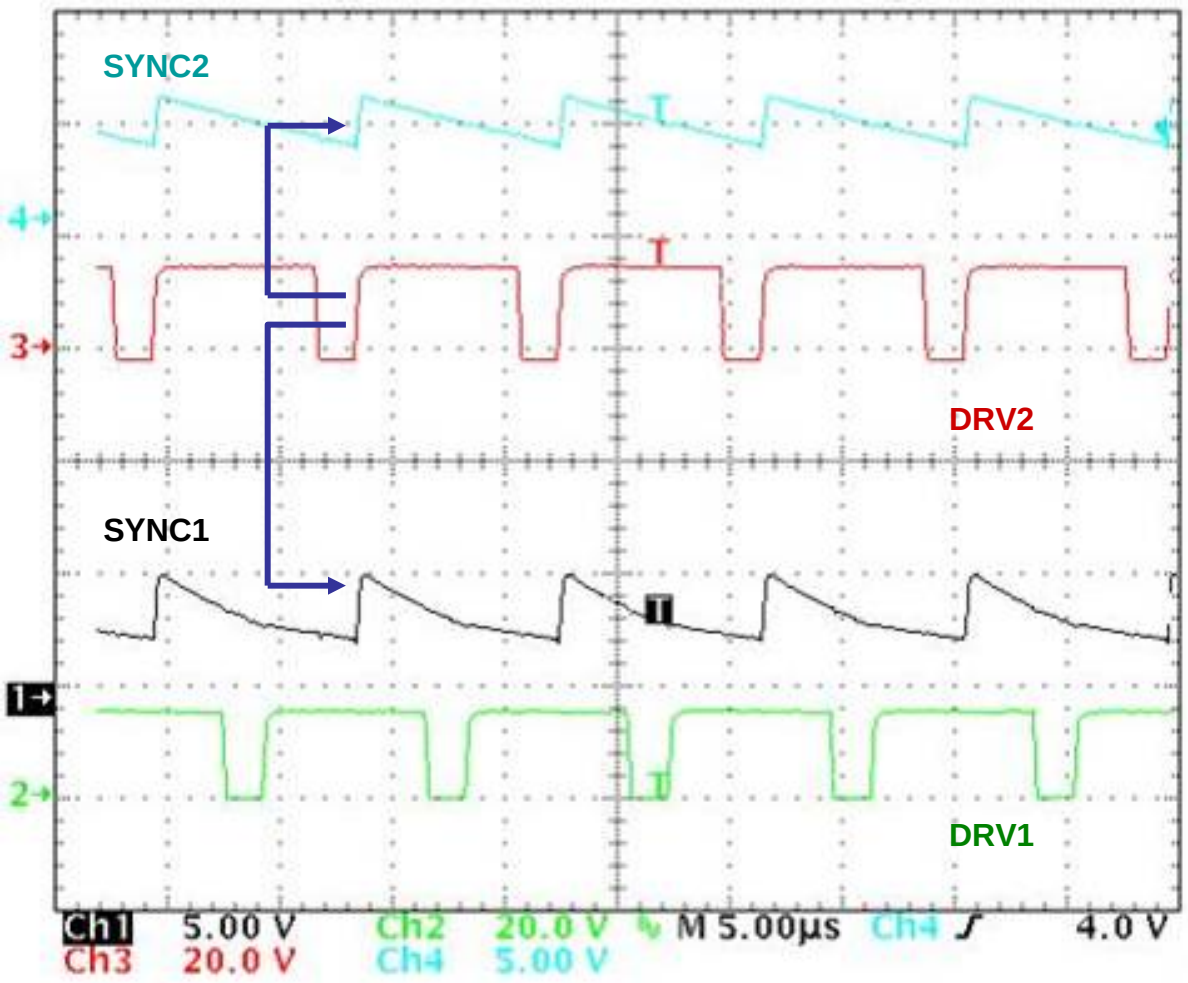


- 每个级以固定频率工作
  Each stage operates in fixed frequency mode
- 两个分支都被同步到DRV2 Both branches are synchronized to DRV2
- 2τ 过后可以发生一个新的DRV2脉冲 A new DRV2 pulse can take place after 2τ
- τ过后可以发生一个新的DRV1脉冲 A new DRV1 pulse can occur after τ
- 每个分支的开关周期是2τ并且它们是异相工作的
  The switching period for each branch is then 2τ and they operate out of phase.

- 只要SYNC信号保持高于3.5 V(见NCP1601工作过程)，一个新的驱动序列就不能发生

A new drive sequence cannot take place as long as the SYNC signal remains higher than 3.5 V (see NCP1601 operation).

低电压、满负载工作情况 Operation at Low Line Full load

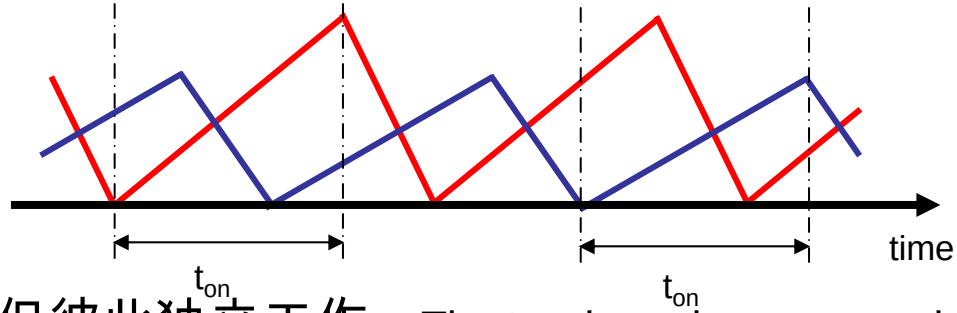


- 电路工作于临界导通模式 The circuit operates in critical conduction mode
- 两个分支都被同步到DRV2 Both branches are synchronized to DRV2
- 2τ 过后可以发生一个新的DRV2脉冲，但MOSFET打开被延迟直到磁芯被复位 A new DRV2 pulse can take place after 2τ, but the MOSFET turn on is delayed until the core is reset
- τ 过后可以发生一个新的DRV1脉冲，但MOSFET打开被延迟直到磁芯被复位 A new DRV1 pulse can occur after τ, but again, the MOSFET turn on is delayed until the core is reset

对该解决方案的一些备注 Remarks on the Solution

- NCP1601 工作域电压模式 The NCP1601 operates in voltage mode
- 两个分支具有相同的导通时间因而具有相同的开关周期 Same on-time and hence switching period in the two branches
- 线圈不平衡 A coil imbalance
  - 不影响开关周期 Does not affect the switching period
  - “只”造成每个分支的功率值存在差异 “Only” causes a difference in the power amount conveyed by each branch

$$\frac{I_{in(1)}}{I_{in(2)}} = \frac{L_2}{L_1}$$

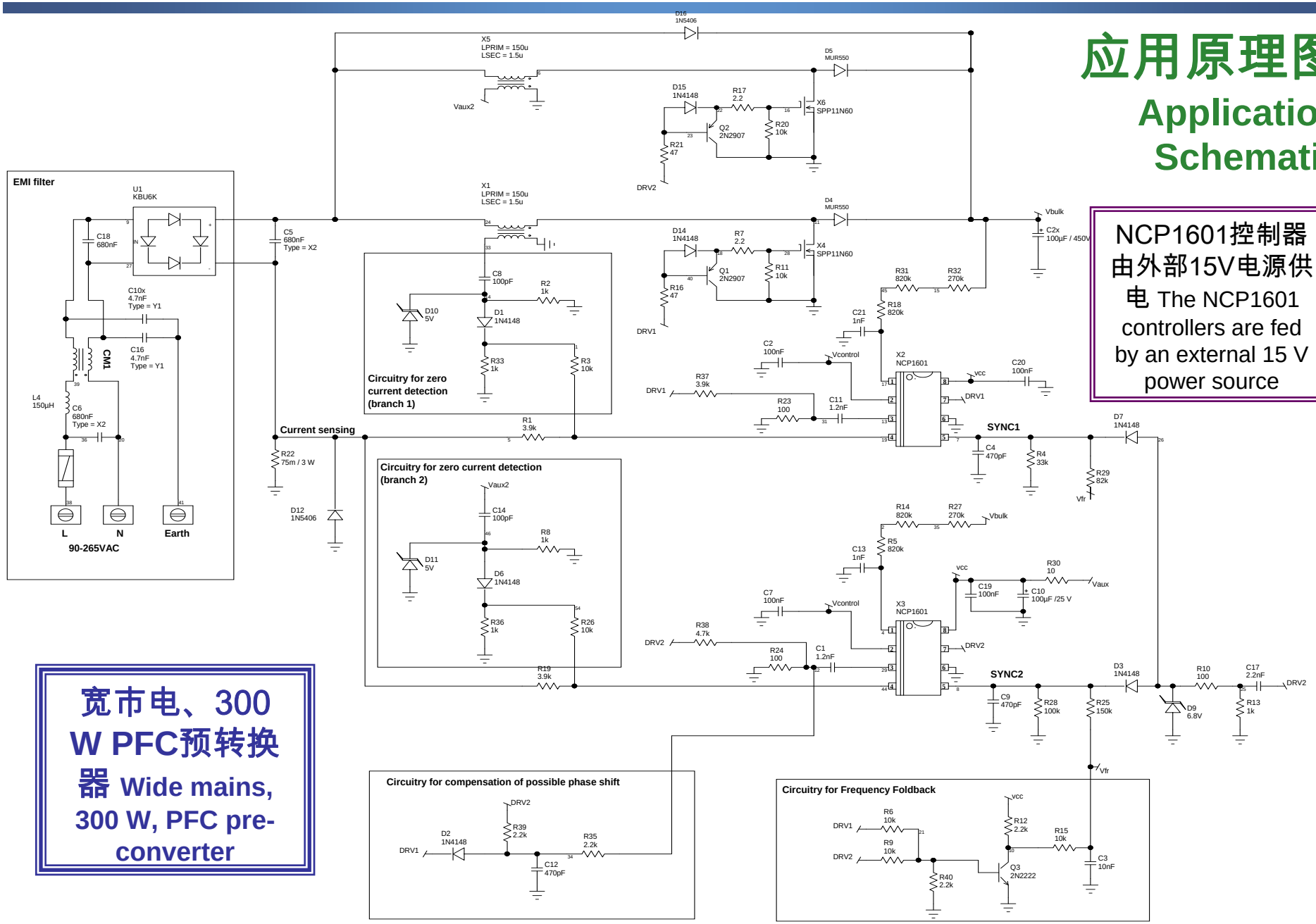


$L_1 > L_2$

相位1 Phase 1
相位2 Phase 2

- 两个分支同步但彼此独立工作：The two branches are synchronized but they operate independently:
  - 保证了非连续导电工作模式(零电流检测) Discontinuous conduction mode is guaranteed (zero current detection)
  - 没有CCM工作模式风险 No risk of CCM operation
  - 在满负载下两个分支都进入CrM工作模式 Both branches enter CrM at full load

应用原理图
Application Schematic

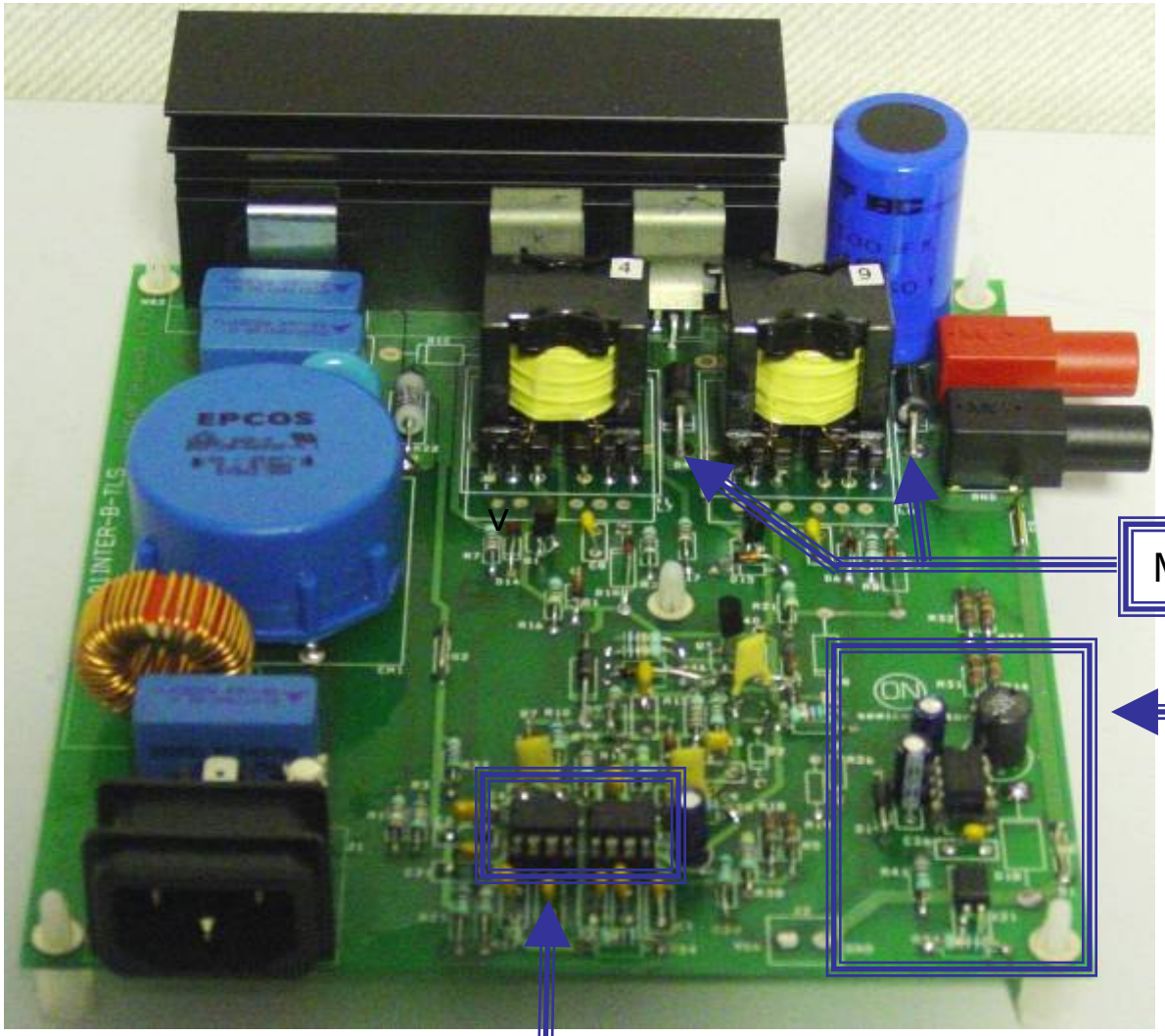


NCP1601控制器由外部15V电源供电 The NCP1601 controllers are fed by an external 15 V power source

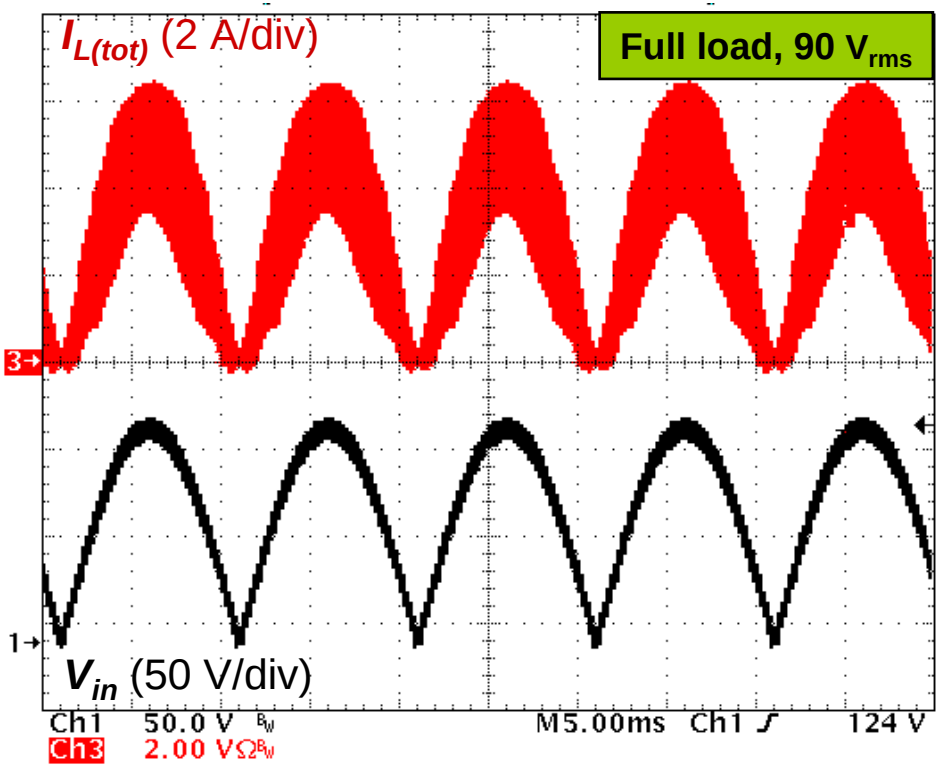
宽市电、300 W PFC预转换器 Wide mains, 300 W, PFC pre-converter

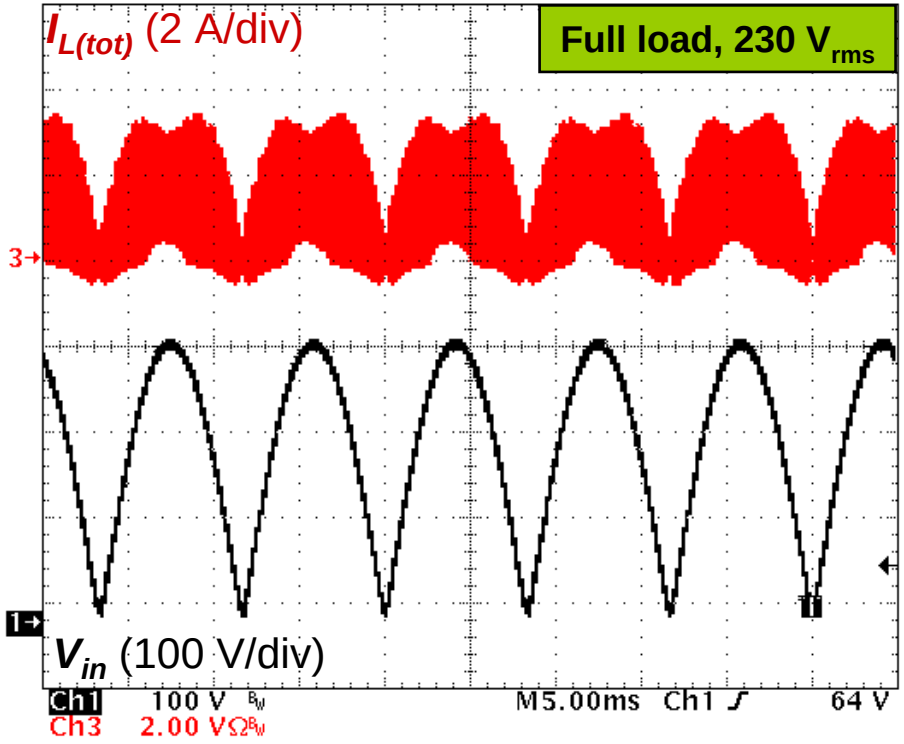
电路板 … The board…

宽市电、300 W PFC预转换器 Wide mains, 300 W, PFC pre-converter



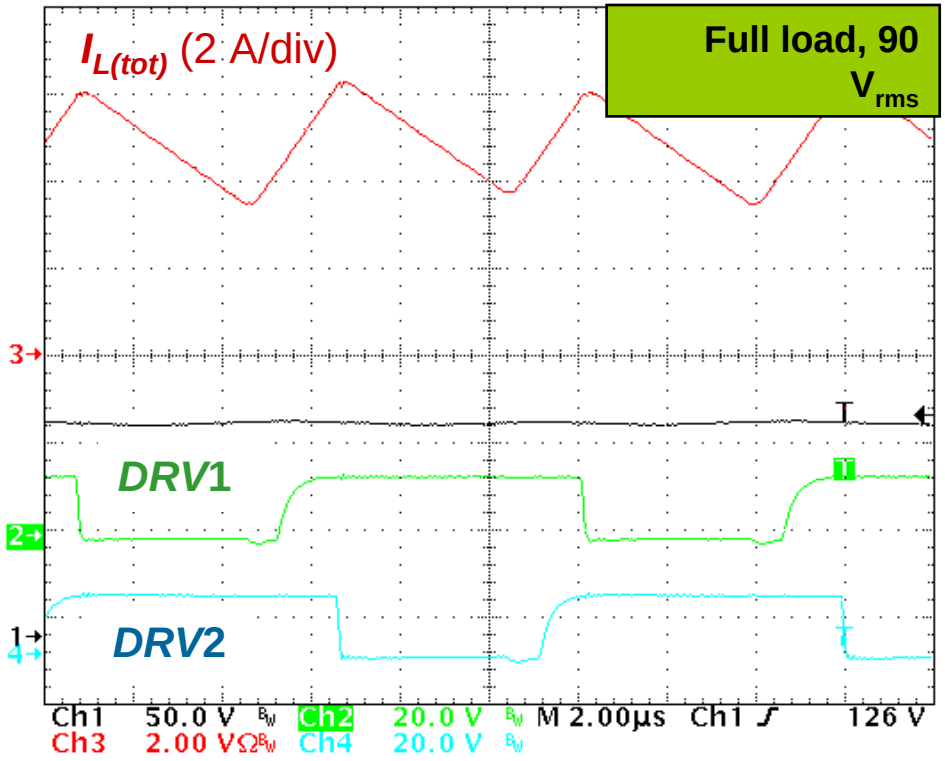
输入电压和电流 Input Voltage and Current

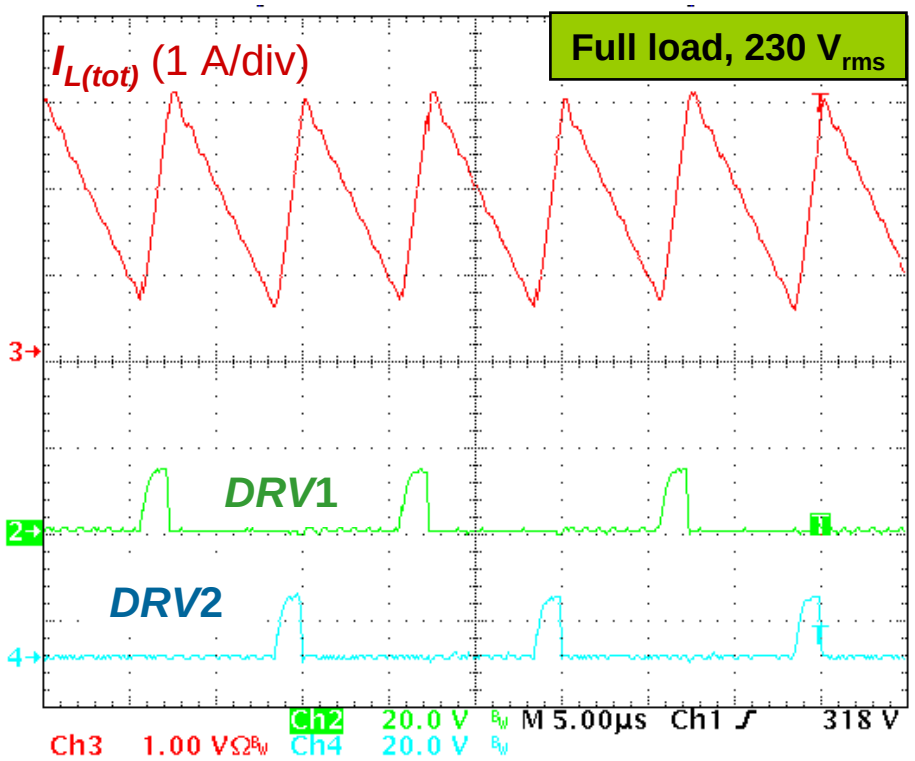




- 如预期的，输入电流看上去像CCM电流 As expected, the input current looks like a CCM one
- 在高压线路，频率反馈机制影响了纹波 At high line, frequency foldback influences the ripple

波形图 Zoom of the Precedent Plots

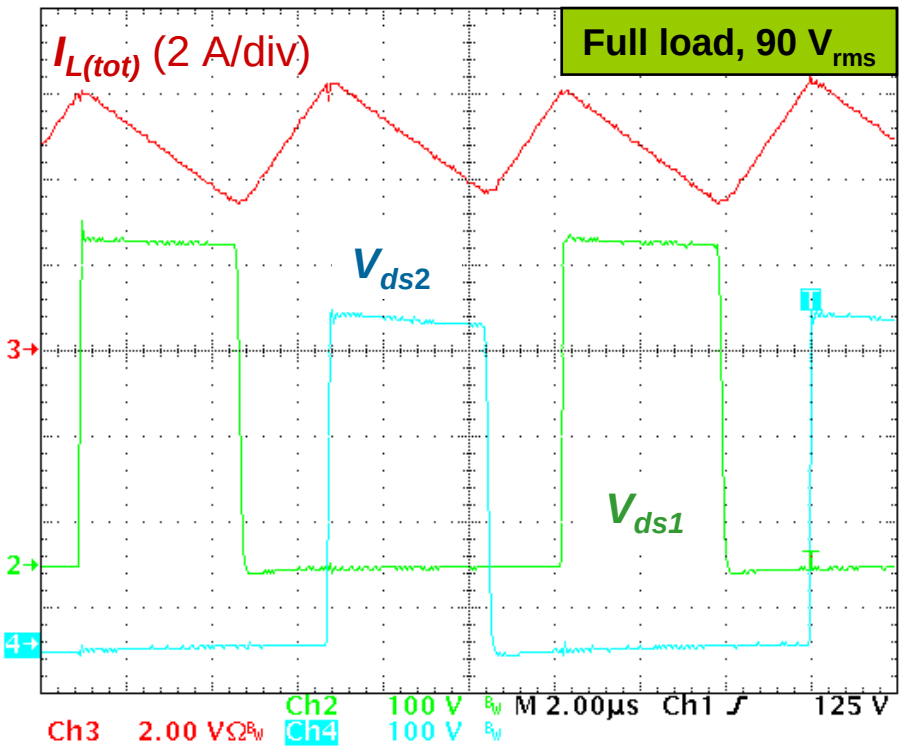


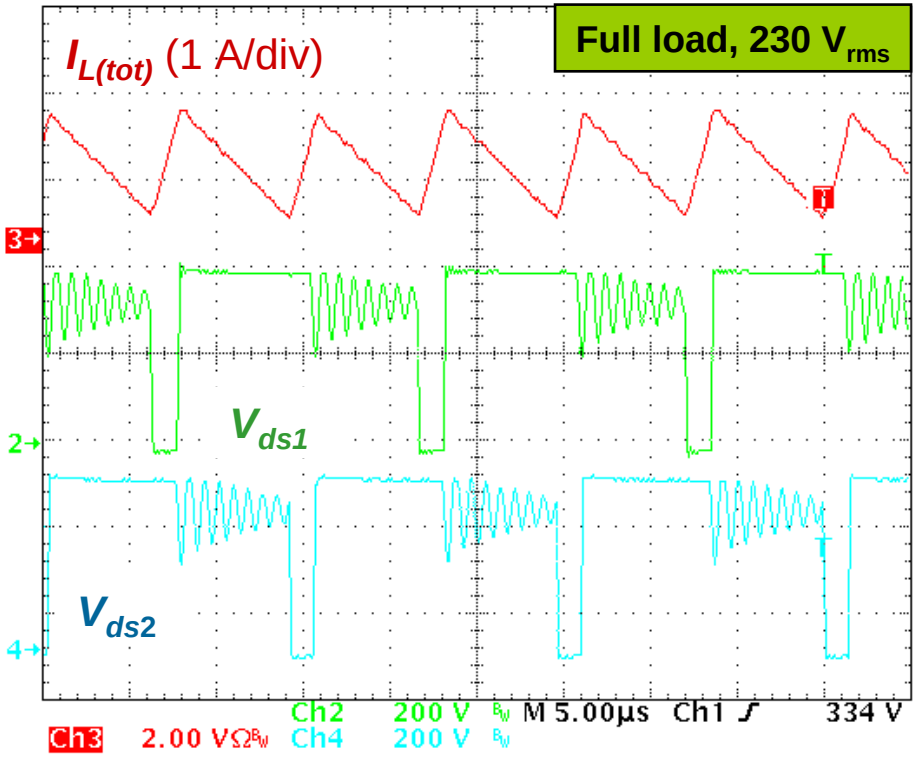


- 这些迹线在正弦曲线顶部获得 These plots were obtained at the sinusoid top
- 电流以每个开关周期频率两倍振荡 The current swings at twice the frequency of each phase
- 在低压和高压线路， 相移基本上为180° At low and high line, the phase shift is substantially 180°

在两个充电序列之间无重叠

No Overlap between the Refueling Sequences





- 低压线路采用CrM、谷值开关模式 CrM at low line with valley switching
- 高压线路采用固定频率工作模式(频率反馈机制) Fixed frequency operation at high line (frequency foldback)
- 两种情况下在上升阶段都无重叠 No overlap between the demag. phases in both cases

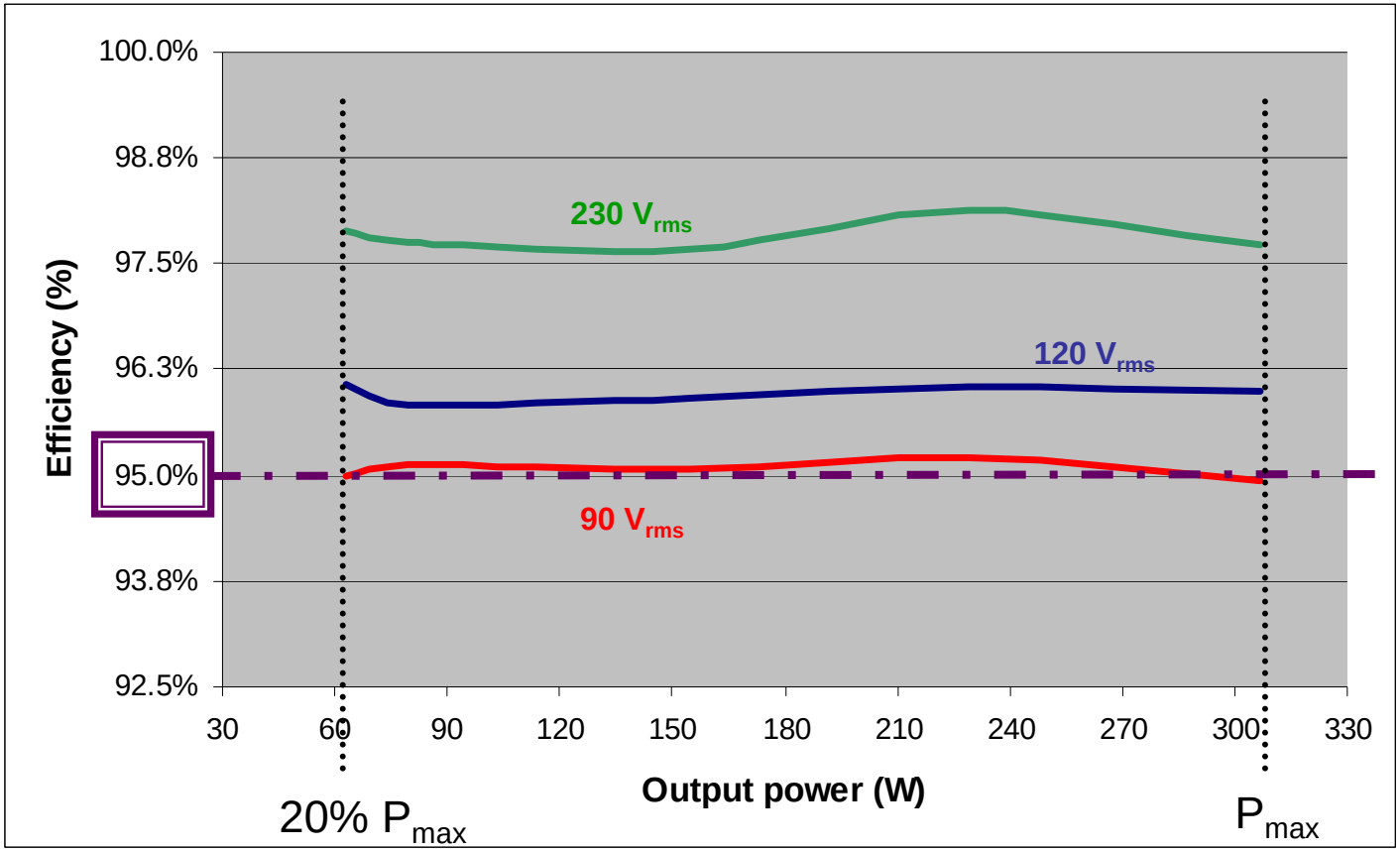
性能测定 Performance Measurements

- 测量条件如下： Conditions for the measurements:
  - 电路板在满负载、低电压线路下工作了30分钟后进行测量 The measurements were made after the board was 30 mn operated full load, low line
  - 所有测量是在没有中断的情况下连续进行的 All the measurements were made consecutively without interruption
  - 采用电能表PM1200对PF、THD、$I_{in(rms)}$进行测量 PF, THD, $I_{in(rms)}$ were measured by a power meter PM1200
  - 采用HP 34401A 万用表在电路输出端直接测量$V_{in(rms)}$ $V_{in(rms)}$ was measured directly at the input of the board by a HP 34401A multimeter
  - 采用HP 34401A 万用表测量V_{out} V_{out} was measured by a HP 34401A multimeter
  - 输入功率根据如下公式计算： The input power was computed according to:

$$P_{in(avg)} = V_{in(rms)} \cdot I_{in(rms)} \cdot PF$$

  - **机箱打开、室温、无风扇 Open frame, ambient temperature, no fan**

效率 vs 负载 Efficiency versus Load



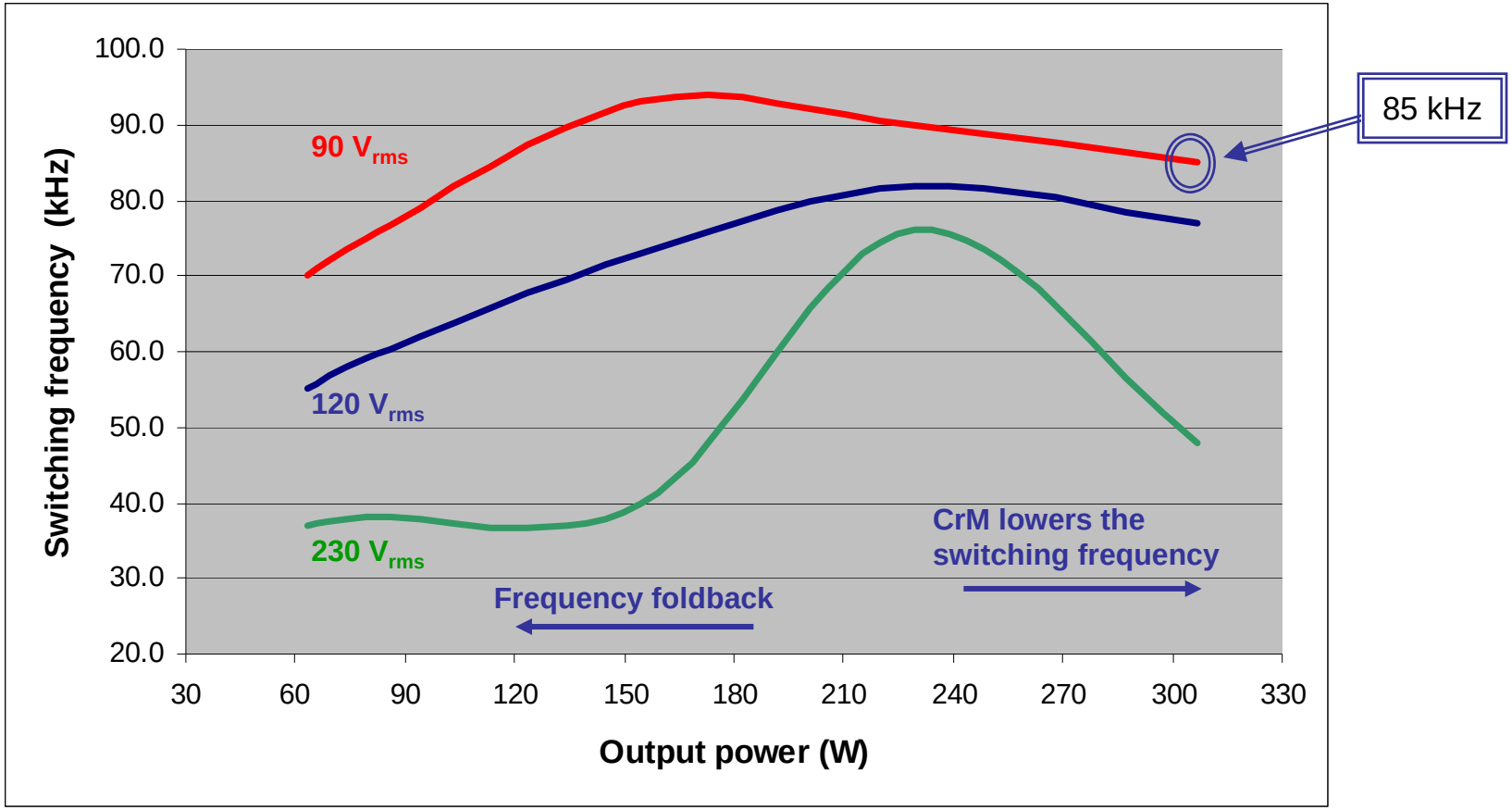
这些结果是在一种相对高频的应用中获得的，该应用可使用小型电感：(90 V_{rms} 下每个周期频率 85 kHz ，满负载，$L_1 = L_2$ =150 µH)

Results obtained in a relatively high frequency application allowing the use of small inductors: (85 kHz in each phase at 90 V_{rms}, full load, $L_1 = L_2$ =150 µH)

❑ 迹线显示了线电压范围内从20%到100%负载之间的效率 The plot portrays the efficiency over the line range, from 20% to 100% of the load

❑ **效率始终高于95% ！** The efficiency remains higher than 95%!

开关频率(在正弦曲线的顶部)
frequency (at the Sinusoid Top)



❑ 迹线显示了线电压范围内开关频率f_{SW} (在正弦曲线的顶部)与负载的函数关系 The plot portrays f_{sw} (sinusoid top) over the line range, as a function of the load

❑ PFC段工作于满负载CrM模式下 The PFC stages operate in CrM at full load

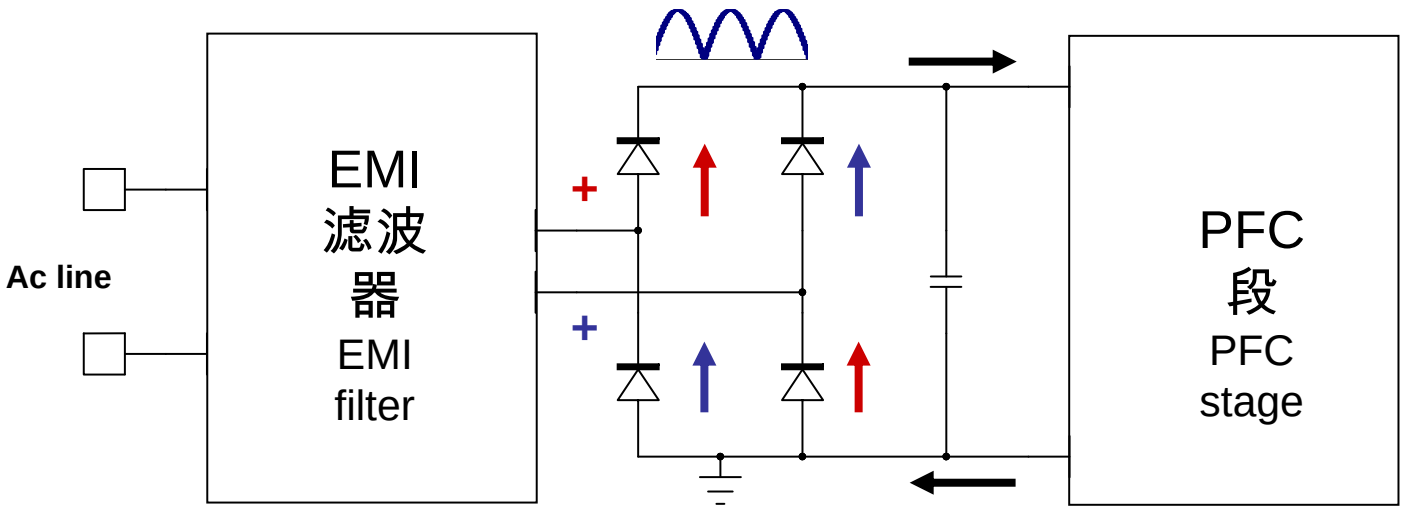
小结 Conclusion

- 交错式的PFC Interleaved PFCs
  - 减小了输入电流纹波 Reduce the input current ripple
  - 降低了大容量电容有效值电流 Lower the bulk capacitor rms current
- 两个NCP1601提供一种高效的交错式解决方案 Two NCP1601 provide an efficient solution for interleaving
- 除了是交错式，但此解决方案也受益于：Besides interleaving, this solution takes benefit of:
  - FCCrM模式优化了效率 The FCCrM mode that optimizes the efficiency
  - 为DCM PFC而优化的MUR550二极管 MUR550 diodes optimized for DCM PFC applications
  - 频率反馈(轻载) Frequency foldback (light load)
- 该解决方案已在一个300 NW、宽市电的电路板上进行了测试 The solution has been tested on a 300 NW, wide mains board
- **在一个很宽的负载范围内(从20%到100%)，在90 V_{rms}下实现了95%的效率**
  95% efficiency at 90 V_{rms} over a large load range (from 20% to 100% load)
- 16引脚的交错式PFC控制器正在开发中 A 16-pin interleaved PFC controller is under development

议程 Agenda

- 引言 Introduction
  - 功率因数校正的基本解决方案 Basic solutions for power factor correction
  - 要满足的新需求 New needs to address
- 交错式的功率因数校正 Interleaved PFC
  - 基本的特征 Basic characteristics
  - 分立的解决方案 A discrete solution
  - 性能 Performance
- **无桥PFC Bridgeless PFC**
  - **为什么我们应当关注输入桥路**
    Why should we care of the input bridge?
  - **主要的解决方案** Main solutions
  - **Ivo Barbi解决方案** Ivo Barbi solution
  - **广域的800 W应用的性能** Performance of a wide mains, 800 W application
- 结论 Conclusion

二极管桥 The diodes bridge



- 二极管桥对交流线路电压进行整流 The diodes bridge rectifies the ac line voltage
- 两个二极管同步导通 Two diodes conduct simultaneously
- PFC输入电流流经两个串联二极管 The PFC input current flows through two series diodes

由二极管桥引起的效率损耗
Efficiency Loss Caused by the Diodes Bridge

- 流经输入二极管的平均电流： Average current flowing through the input diodes:

$$\left\langle I_{bridge} \right\rangle_{T_{line}} = \left\langle I_{line}(t) \right\rangle_{T_{line}} = \frac{2\sqrt{2}}{\pi} \cdot \frac{P_{out}}{\eta \cdot V_{in(rms)}}$$

- 二极管桥的功耗： Dissipation in the diodes bridge:

$$P_{bridge} = 2 \cdot V_f \cdot I_{bridge} \approx 2 \cdot V_f \cdot \frac{2\sqrt{2} \cdot P_{out}}{\eta \cdot \pi \cdot V_{in(rms)}}$$

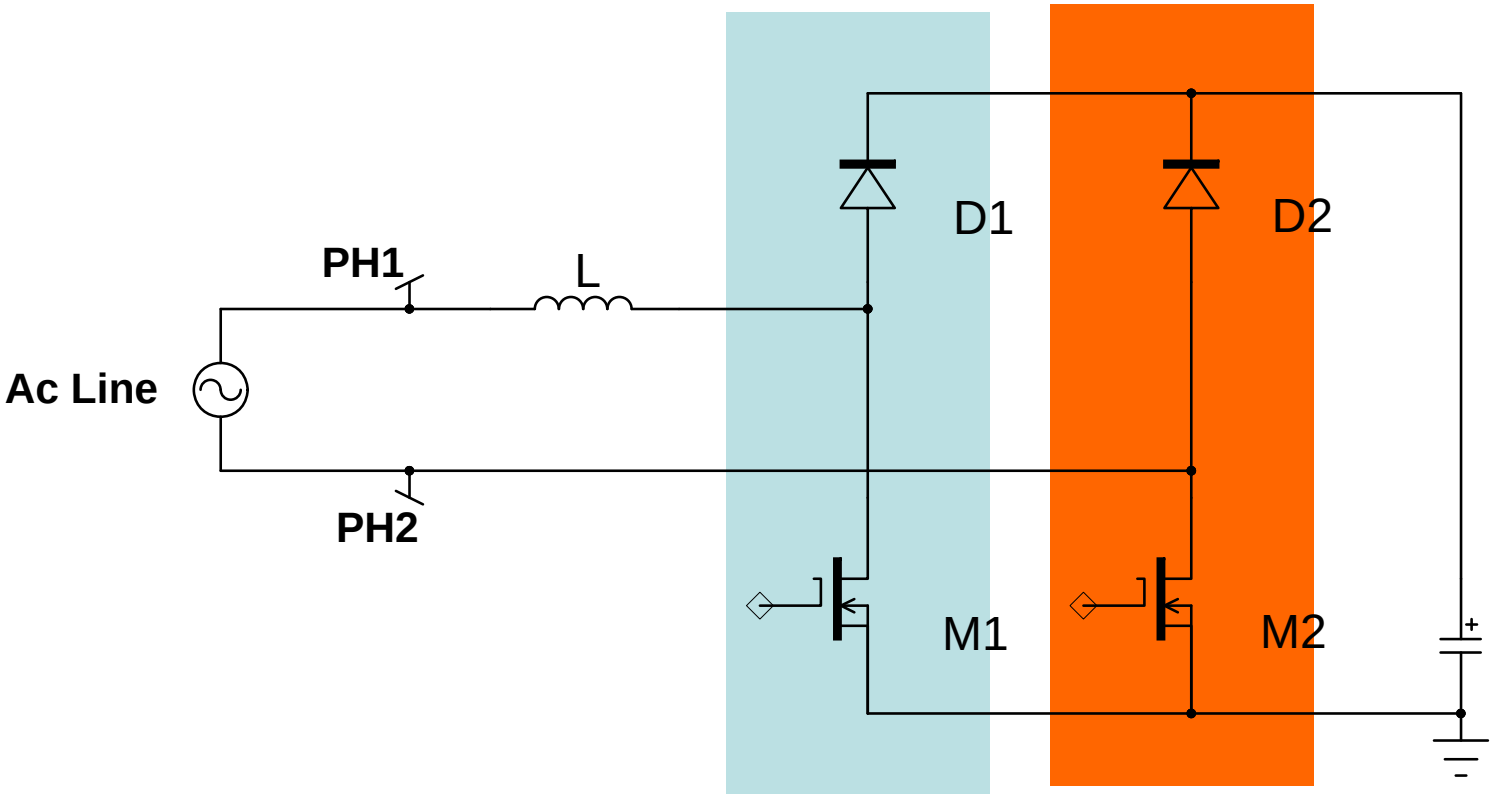
- 如果V_f = 1 V和$(V_{in(rms)})_{LL}$ = 90 V： If V_f = 1 V and $(V_{in(rms)})_{LL}$ = 90 V:

$$P_{bridge} \approx 2\% \cdot \frac{P_{out}}{\eta}$$

➔**在低市电应用(@ 90 V_{rms})中，二极管桥浪费大约2%的效率 In low mains applications (@ 90 V_{rms}), the diodes bridge wastes about 2% efficiency!**

基本的无桥PFC Basic Bridgeless PFC

开关单元当PH2为高M1关断
Switching cell when PH2 is high
M1 is off



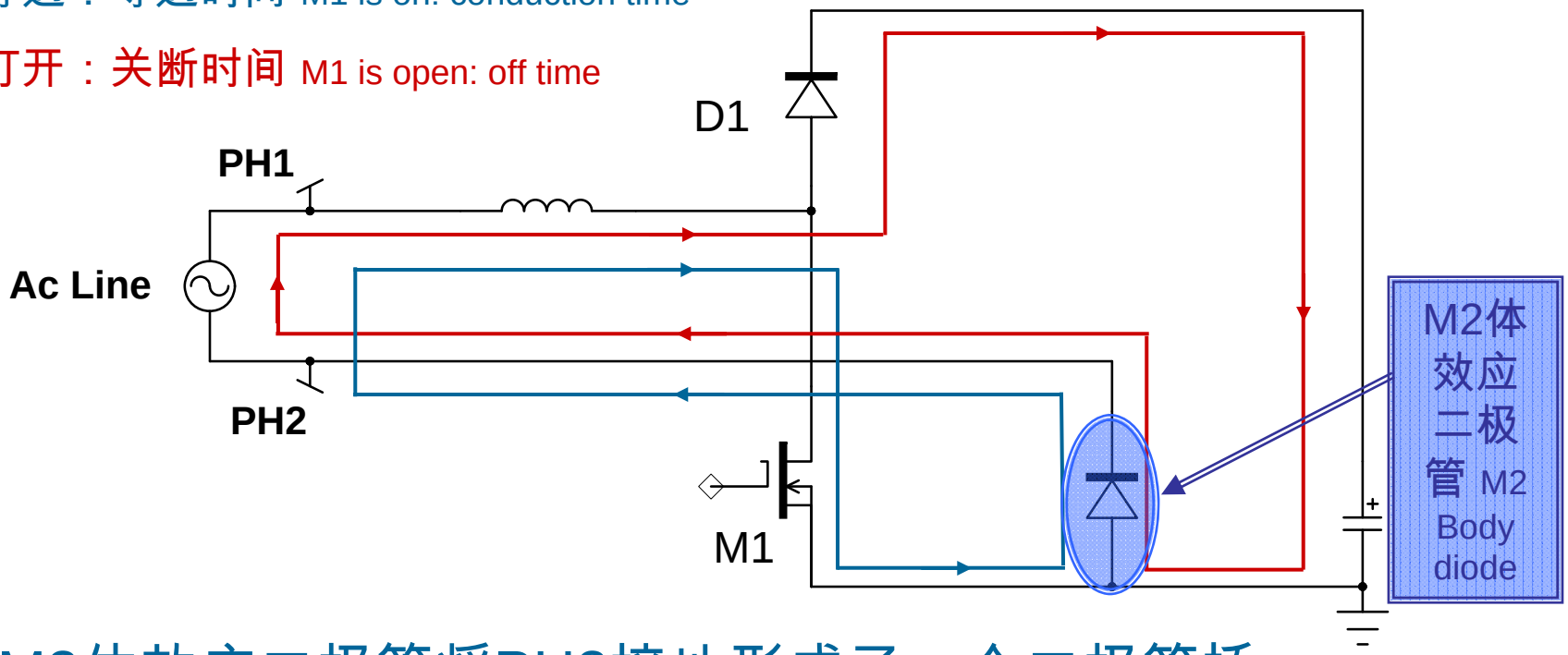
开关单元当PH1为高M2关断
Switching cell when PH1is high
M2 is off

以正半波工作 Operation with Positive Half-Wave

❑ PH1为高，PH2为低： PH1 is high, PH2 is low:

M1导通：导通时间 M1 is on: conduction time

M1打开：关断时间 M1 is open: off time



❑ M2体效应二极管将PH2接地形成了一个二极管桥

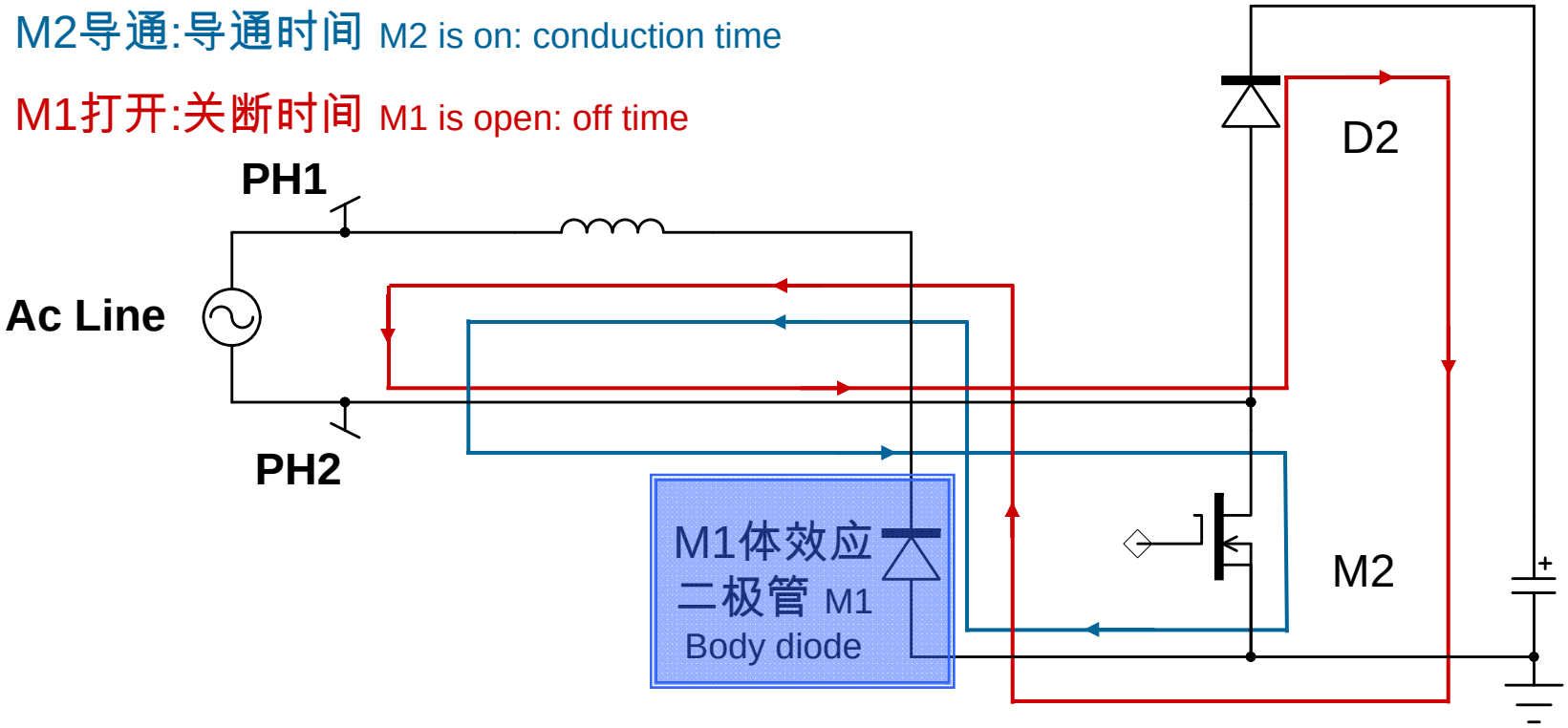
M2 body diode grounds PH2 as would a diode bridge.

以负半波工作 Operation With Negative Half-wave

❑ PH1为低，PH2为高： PH1 is low, PH2 is high:

M2导通:导通时间 M2 is on: conduction time

M1打开:关断时间 M1 is open: off time

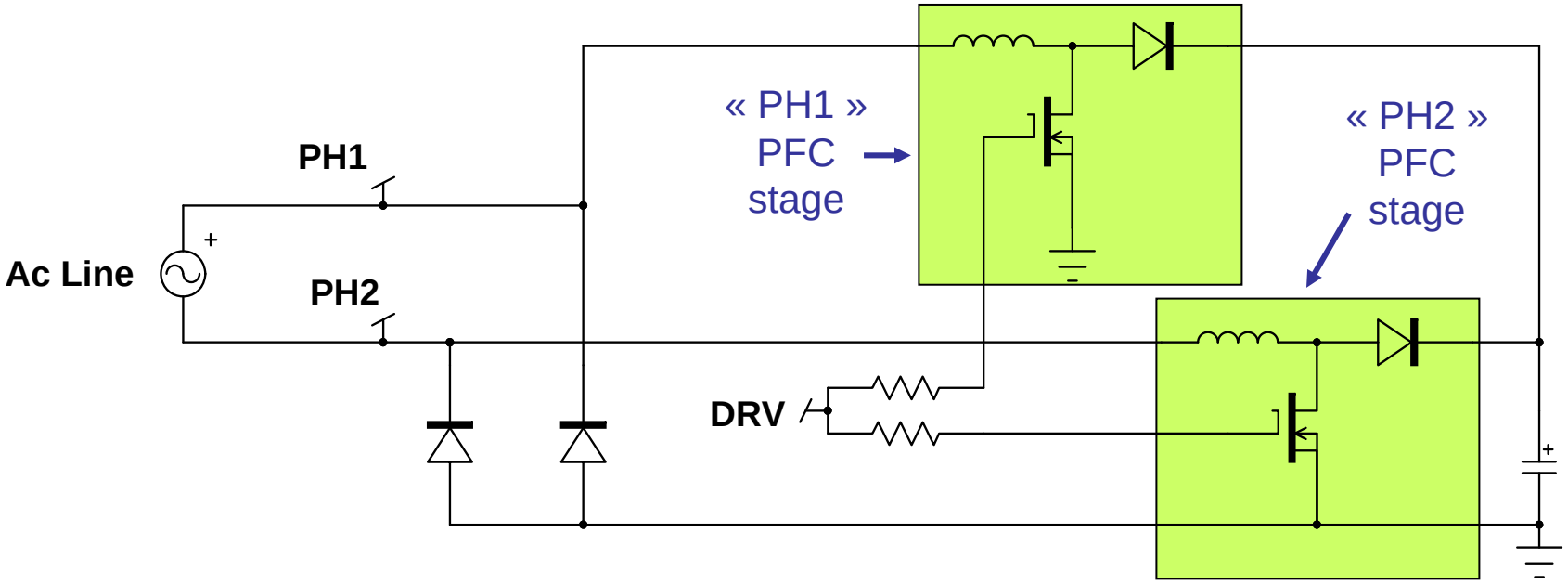


❑两个线路终端都以开关频率振动 Both line terminals are pulsating at the switching frequency

❑振动幅度很高(V_{OUT}) The pulsation swing is high (V_{OUT})

❑高频噪声需要进行繁琐的EMI滤波 HF noise that leads to a tedious EMI filtering

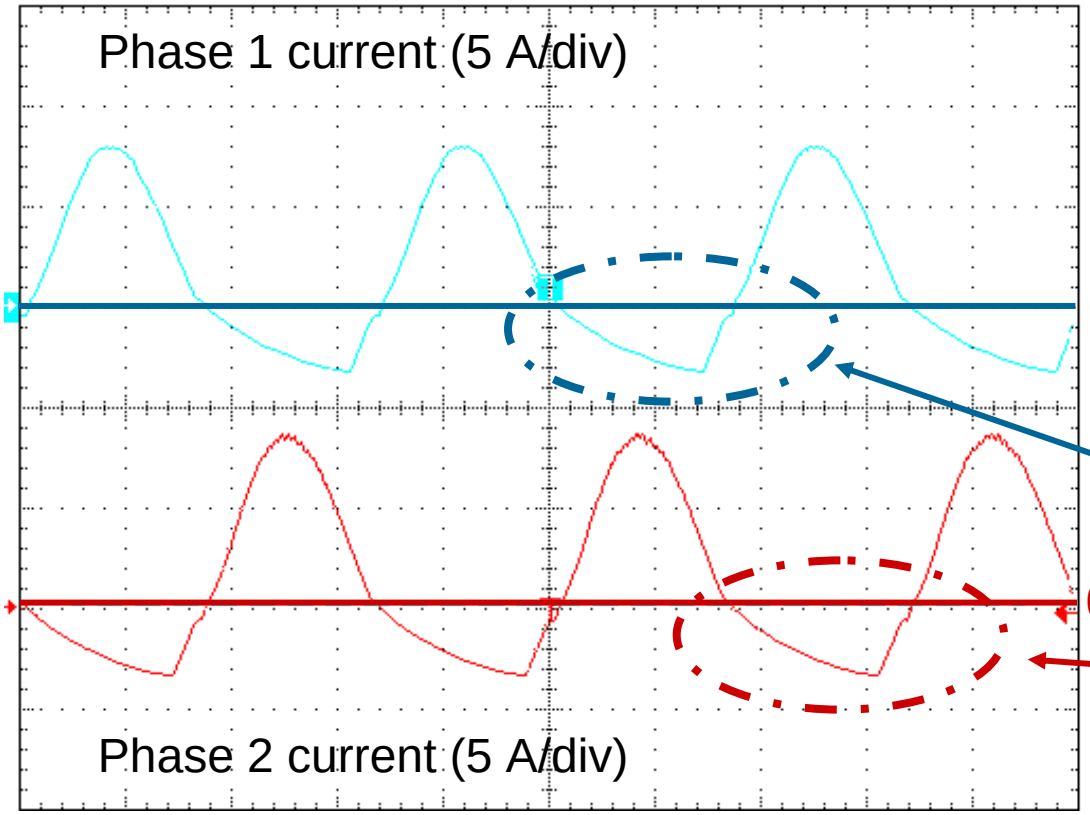
Ivo Barbi无桥升压 Ivo Barbi Bridgeless Boost



两个PFC段但是： Two PFC stages but:

- 一个驱动器，无需检测活动的半波 One driver with no need for detecting the active half-wave
- 热性能有所改善 Improved thermal performance
- 由于采用惯常的PFC段，负相总是接地，EMI问题迎刃而解 As with convential PFC stages, the negative phase is always attached to ground. EMI issue is solved.

电流分配 Current Sharing



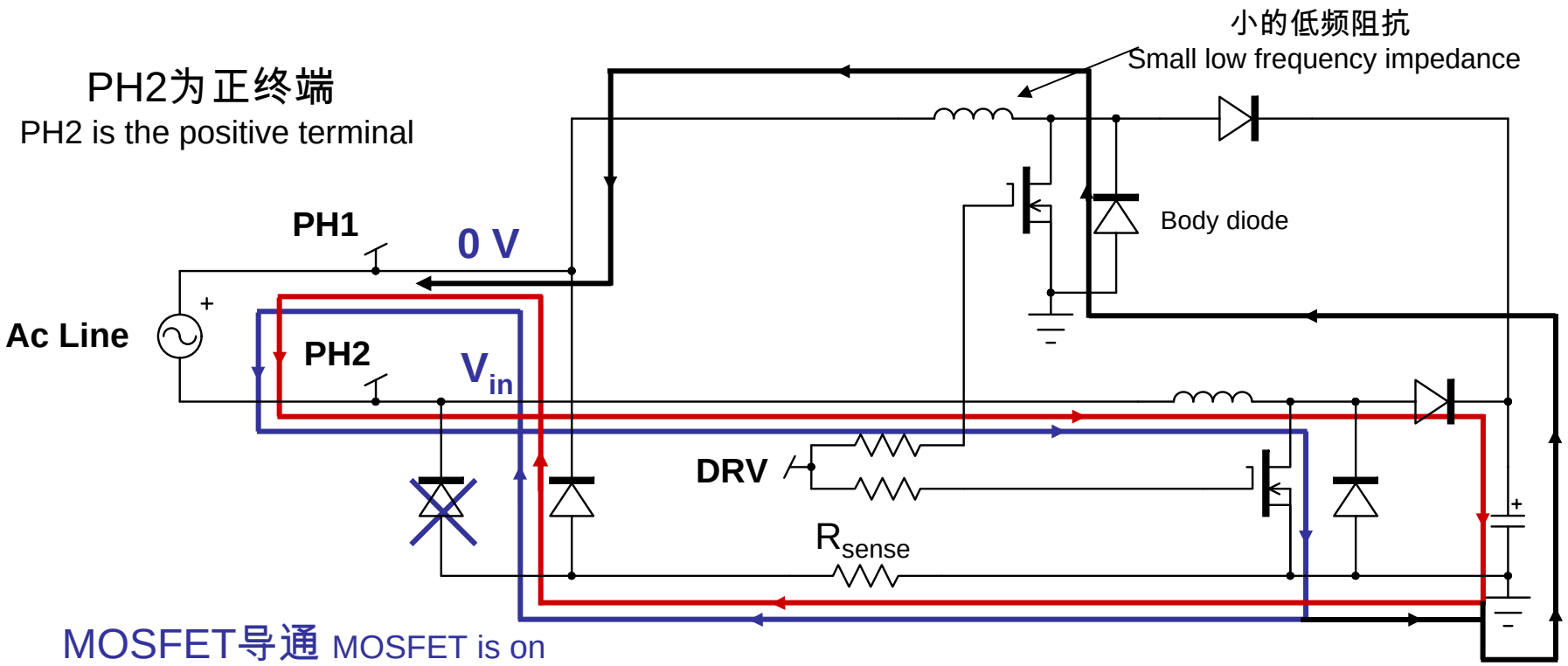
一部分工作相位的电流流经不工作的MOSFET和线圈Part of the active phase current flows throught the inactive MOSFET and coil!

一部分电流流经假定为不工作的MOSFET和线圈

Part of the current flows…

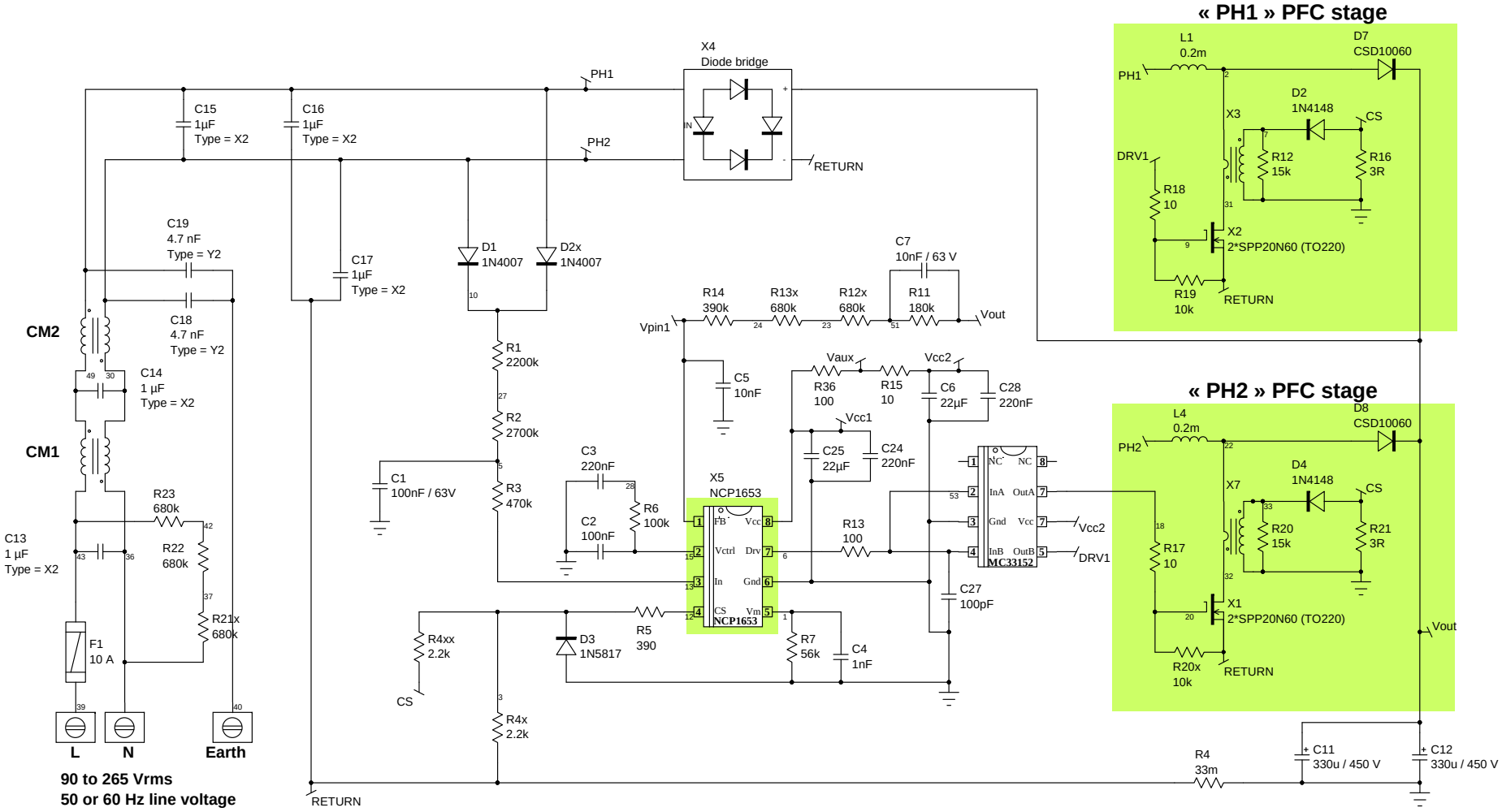
… through the supposedly inactive MOSFET and coil

两个返回路径 Two Rreturn Paths…

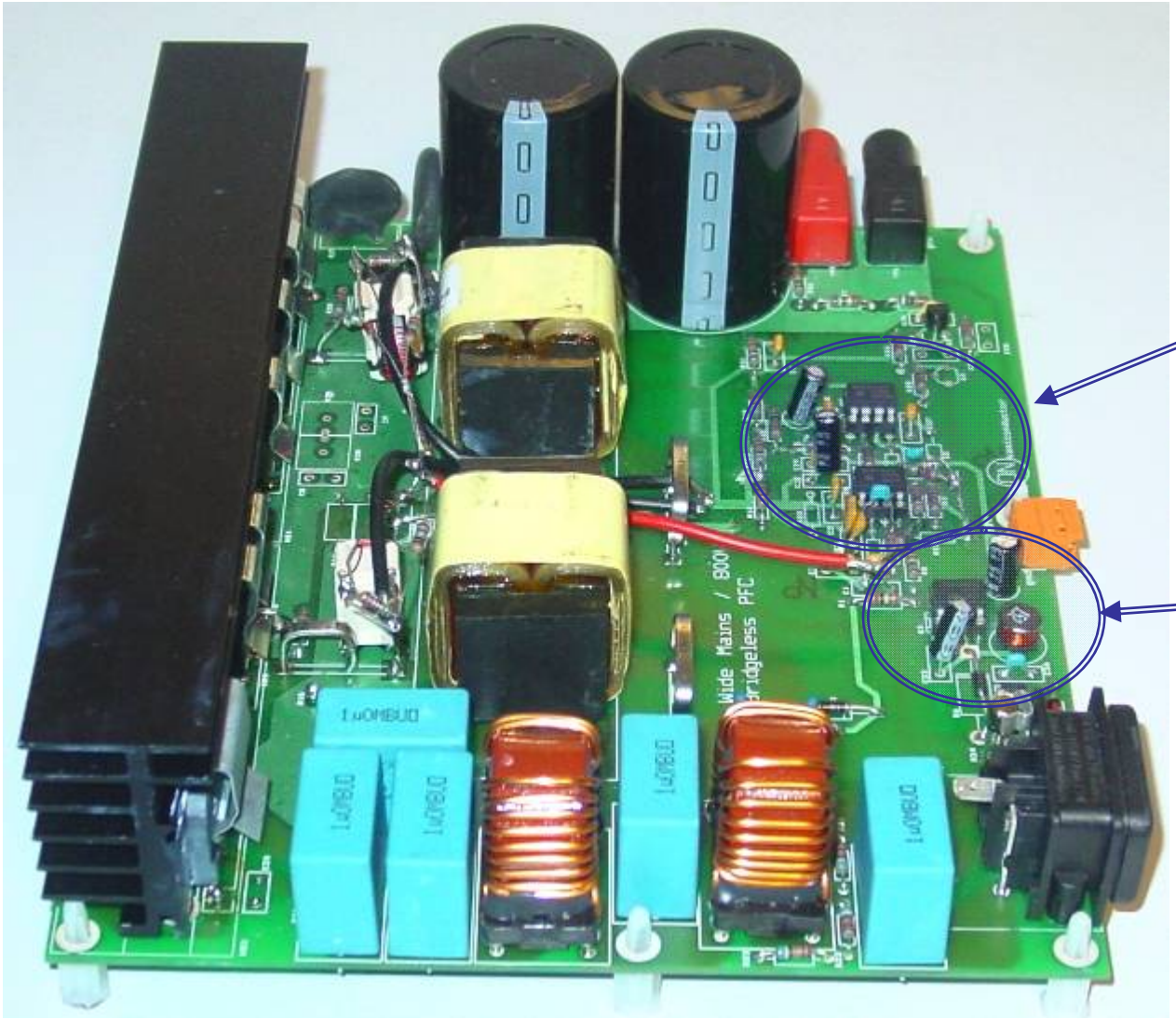


需要电流感应变压器 Need for current sense transformers

800 W原型原理图 Schematic for 800 W Prototype



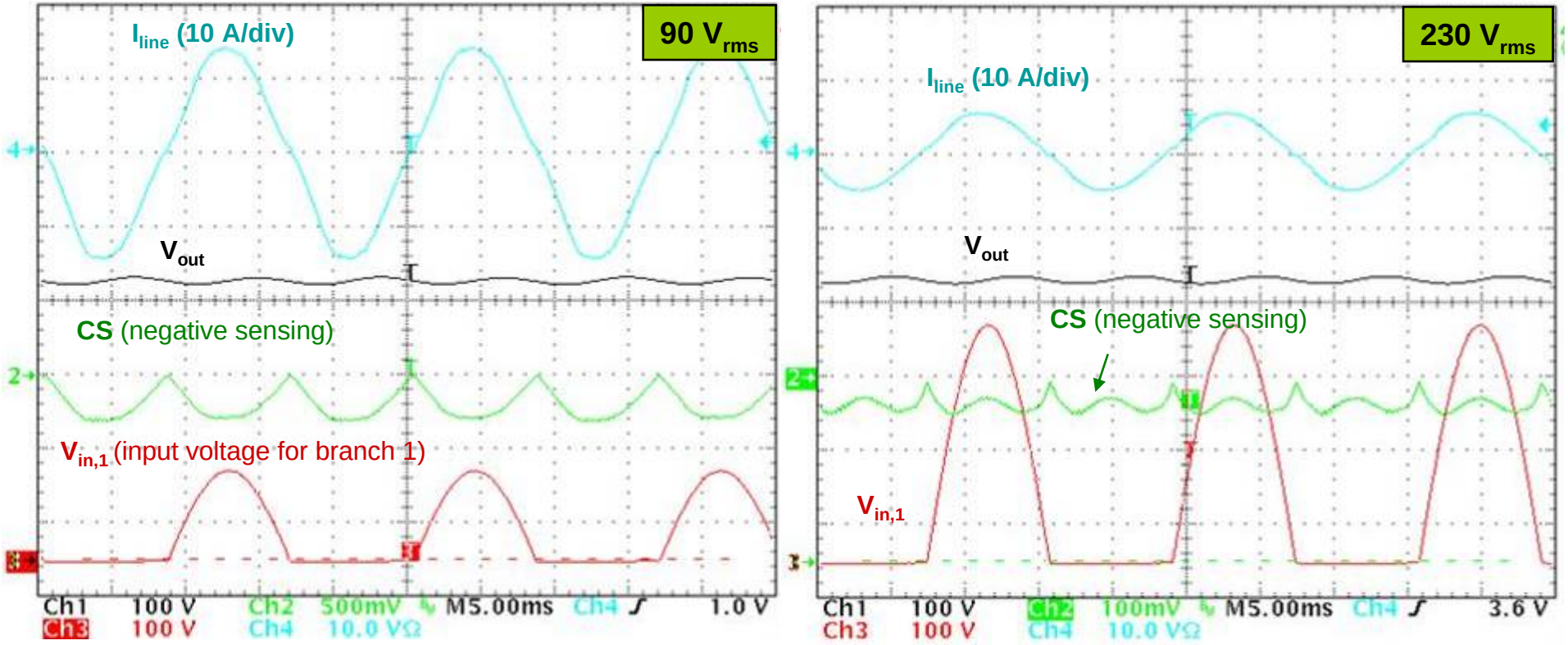
电路板照片 Board Photograph



NCP1653
和MC33152
MOSFET驱动器
NCP1653
And
MC33152
MOSFET driver

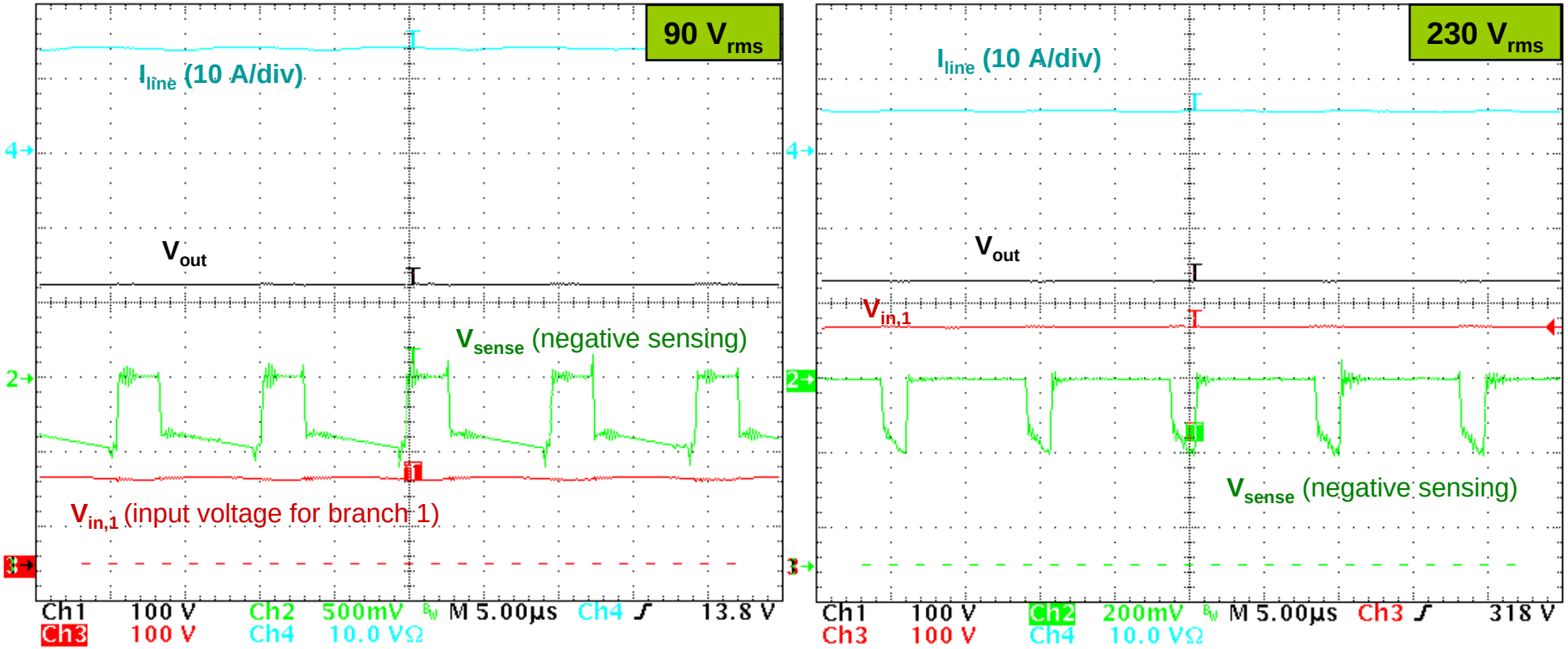
大容量转换器
产生V_{cc}电压
Bulk converter
to generate the
V_{cc} voltage
(NCP1012)

典型的波形 Typical Waveforms



- 这些迹线显示了全负载下的典型波形(I_{out} = 2.1 A) These plots portray typical waveforms at full load (I_{out} = 2.1 A)
- “CS”代表了流经两个分支的MOSFET的电流(电流变压器的公共输出) “CS” is representative of the current flowing into the MOSFETs of the two branches (common output of the current transformers)
- 输入电流是正弦曲线 The input current is sinusoidal

范例迹线窗(正弦曲线的顶部) Zoom of the Precedent Plots (top of the Sinusoid)



- 开关频率是100 kHz The switching frequency is 100 kHz
- 这些波形与传统CCM PFC的波形类似 The waveforms are similar to those of a traditional CCM PFC

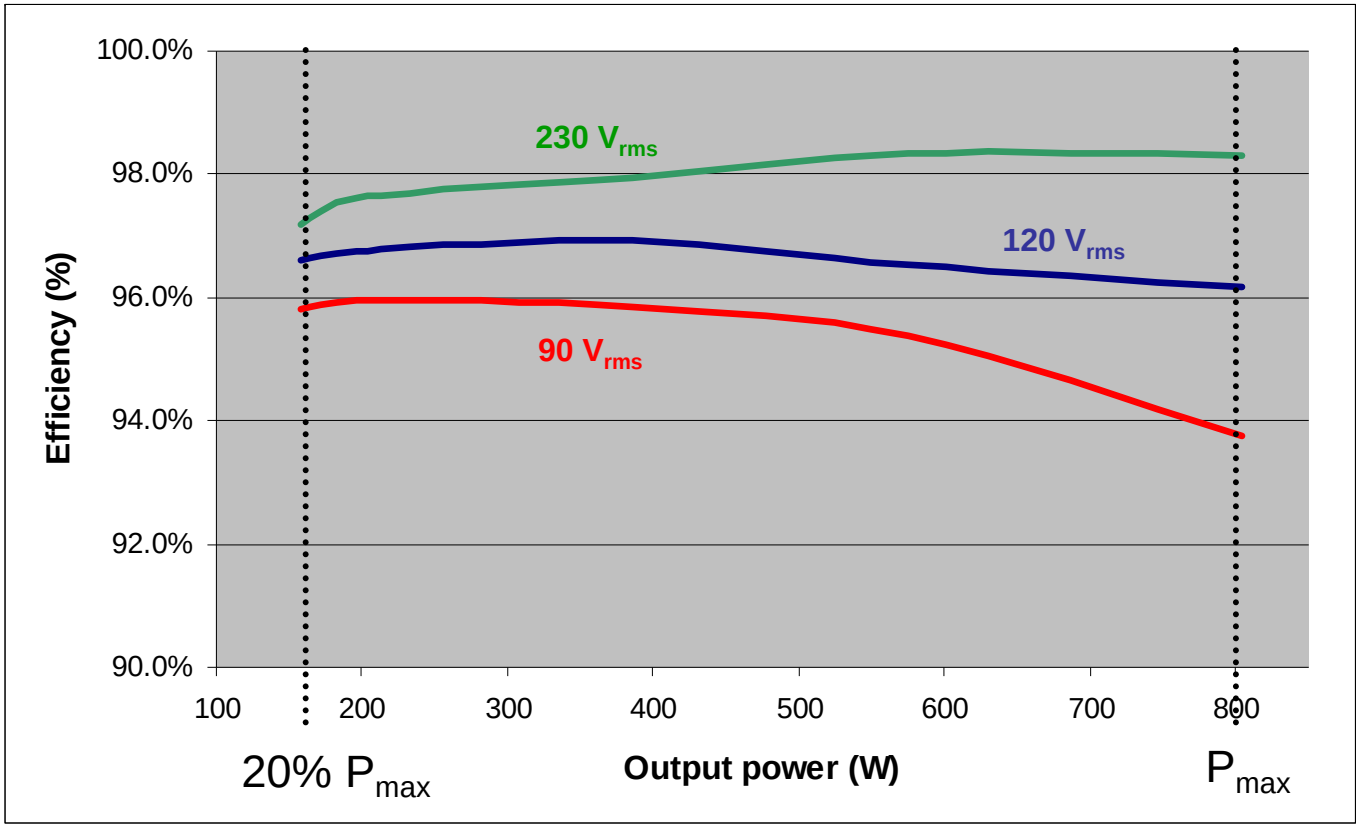
性能评测 Performance Measurements

- 测量条件如下： Conditions for the measurements:
  - 电路板在满负载、低电压线路下工作了30分钟后进行测量 The measurements were made after the board was 30 mn operated full load, low line
  - 所有测量是在没有中断的情况下连续进行的 All the measurements were made consecutively without interruption
  - 采用电能表PM1200对PF、THD、$I_{in(rms)}$进行测量 PF, THD, $I_{in(rms)}$ were measured by a power meter PM1200
  - 采用HP 34401A万用表在电路输出端直接测量$V_{in(rms)}$ $V_{in(rms)}$ was measured directly at the input of the board by a HP 34401A multimeter
  - 采用HP 34401A万用表测量V_{out} V_{out} was measured by a HP 34401A multimeter
  - 输入功率根据如下公式计算： The input power was computed according to:

$$P_{in(avg)} = V_{in(rms)} \cdot I_{in(rms)} \cdot PF$$

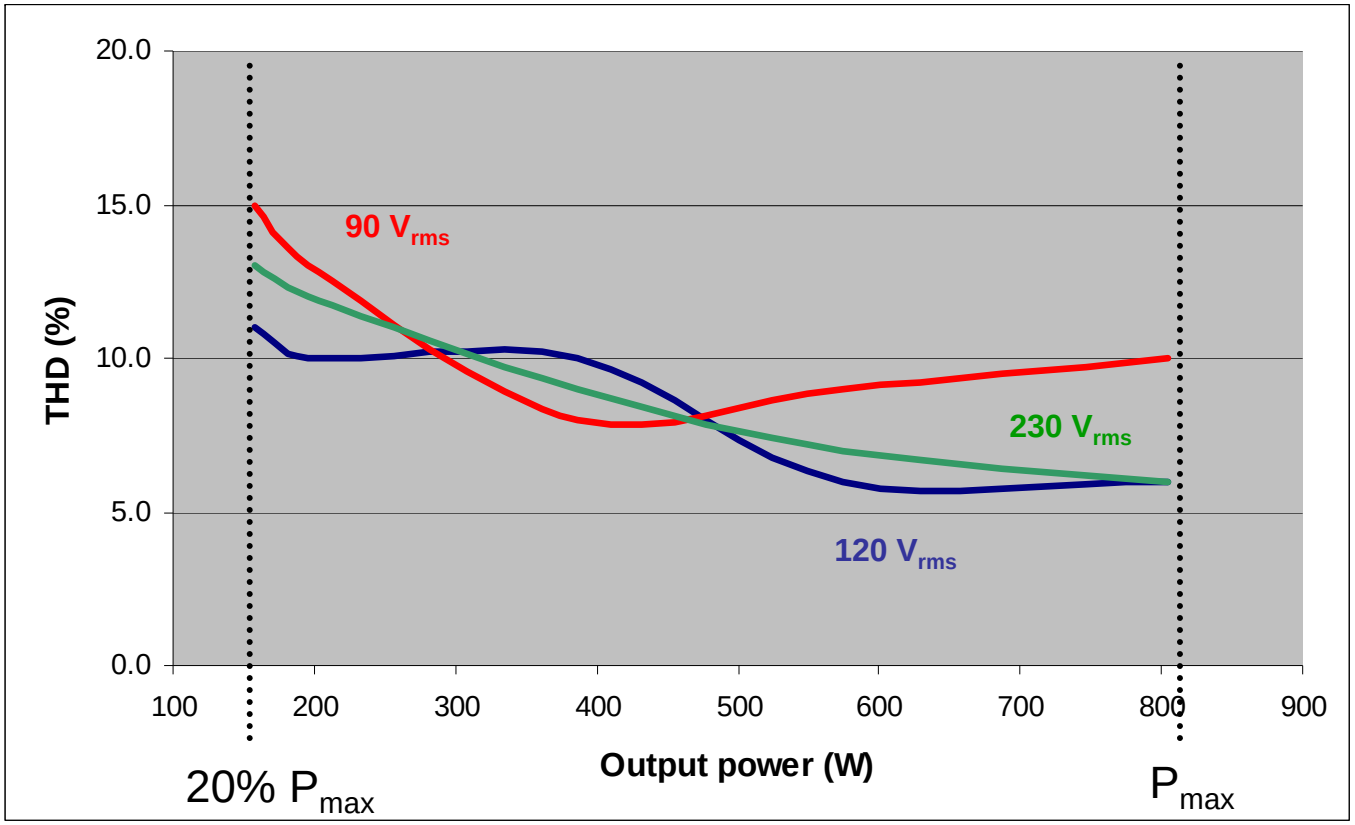
  - **机箱打开、室温、无风扇 Open frame, ambient temperature, no fan**

效率对比负载 Efficiency versus Load



- 该迹线显示了负载从20%到100%的效率 The plot portrays the efficiency from 20% to 100% of the load
- 在90 V_{rms}、满负载下，无风扇效率为94%（100 V_{rms}为95%) At 90 V_{rms}, full load, it is about 94% without fan (95% at 100 V_{rms})
- 满负载的20%处，效率接近或超过96% At 20% of full load, efficiency is in the range or higher than 96%

THD对比负载 THD versus Load



- 在整个范围内，总谐波失真（THD）保持非常低 THD remains very low on the whole range

小结 Conclusion

- 由NCP1653控制的无桥PFC已在开发中(100 kHz) A bridgeless PFC controlled by the NCP1653 has been developed (100 kHz)
- 原型已在全负载(800 W输出)、无风扇(机箱打开、室温)条件下进行了测试 The prototype was tested at full load (800 W output) without fan (open frame, ambient temperature)
- 在这些条件下，测量出的效率在90 V_{rms} 下为94%左右，100 V_{rms}下为95% In these conditions, the efficiency was measured in the range of 94% at 90 V_{rms} and 95% at 100 V_{rms}
- THD保持非常低 The THD remains very low
- 无桥对于大功率应用会是一个高效的解决方案 Bridgeless can be an efficient solution for high power applications.
- 应用笔记正在准备中，将在今年第四季度发布 An application note is being prepared and should be posted in Q4 this year.

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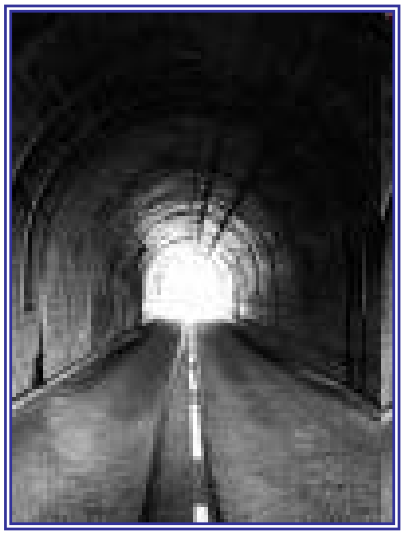

结论 Conclusions

- 新的需求： New requirements:
  - 紧凑的外形尺寸(LCD TV) Compactness and form factor (LCD TV)
  - 效率（ATX电源)（Efficiency (ATX power supplies)
- 新的解决方案可以满足这些需求 New solutions can address them
- 交错式的PFC带来了： Interleaved PFC brings:
  - 效率 Efficiency
  - 扁平设计 Flat design
  - 改进的散热 Improved heat distribution
  - 穿过PFC段的有效值电流减小 Reduced rms current through the PFC stage
  - 模块化方案 Modular approach
- 无桥PFC： Bridgeless PFC:
  - 输入整流的损耗降低了一半 halves the losses in the input rectification
  - 改进了散热 Improves the heat distribution
- 安森美半导体支持这些创新的方案 ON Semiconductor supports these innovative approaches

For More Information

- View the extensive portfolio of power management products from ON Semiconductor at www.onsemi.com
- View reference designs, design notes, and other material supporting the design of highly efficient power supplies at www.onsemi.com/powersupplies