

# MOSFET – Power, Single N-Channel, $\mu$ 8FL

30 V, 55 A, 5.9 m $\Omega$

## NVTFS4C08N

### Features

- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C08NWF – Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Symbol	Parameter	Value	Unit	
$V_{DSS}$	Drain-to-Source Voltage	30	V	
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V	
$I_D$	Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 4)	$T_A = 25^\circ\text{C}$	17	A
		$T_A = 100^\circ\text{C}$	12	
$P_D$	Power Dissipation $R_{\theta JA}$ (Note 1, 2, 4)	$T_A = 25^\circ\text{C}$	3.1	W
		$T_A = 100^\circ\text{C}$	1.6	
$I_D$	Continuous Drain Current $R_{\theta JC}$ (Note 1, 3, 4)	$T_A = 25^\circ\text{C}$	55	
		$T_A = 100^\circ\text{C}$	39	A
$P_D$	Power Dissipation $R_{\theta JC}$ (Note 1, 3, 4)	$T_A = 25^\circ\text{C}$	31	W
		$T_A = 100^\circ\text{C}$	15	
$I_{DM}$	Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	253	A
$T_J, T_{stg}$	Operating Junction and Storage Temperature	-55 to +175	$^\circ\text{C}$	
$I_S$	Source Current (Body Diode)	28	A	
$E_{AS}$	Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, I_L = 20 A_{pk}, L = 0.1 \text{ mH}$ )	20	mJ	
$T_L$	Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

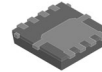
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Drain) (Notes 1 and 4)	4.9	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Notes 1 and 2)	48	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup> 2 oz. Cu pad.
3. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
30 V	5.9 m $\Omega$ @ 10 V	55 A
	9.0 m $\Omega$ @ 4.5 V	

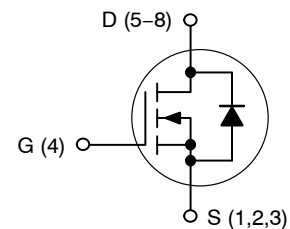


WDFN8  
CASE 511AB

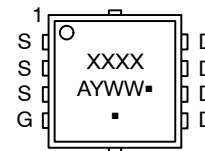


WDFNW8  
CASE 515AN

### N-Channel MOSFET



### MARKING DIAGRAM



4C08 = Specific Device Code for NVMTS4C08N

08WF = Specific Device Code of NVTFS4C08NWF

A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

# NVTFS4C08N

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>						
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient			13.8		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	$\mu\text{A}$
			$T_J = 125^\circ\text{C}$		10	
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA

### ON CHARACTERISTICS (Note 5)

$V_{GS(TH)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3		2.2	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient			5.0		$\text{mV}/^\circ\text{C}$
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		4.7	5.9	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 18\text{ A}$		7.2	9.0	
$g_{FS}$	Forward Transconductance	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		42		S
$R_G$	Gate Resistance	$T_A = 25^\circ\text{C}$		1.0		$\Omega$

### CHARGES AND CAPACITANCES

$C_{ISS}$	Input Capacitance	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		1113		$\text{pF}$
$C_{OSS}$	Output Capacitance			702		
$C_{RSS}$	Reverse Transfer Capacitance			39		
$C_{RSS}/C_{ISS}$	Capacitance Ratio	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		0.035		
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		8.4		$\text{nC}$
$Q_{G(TH)}$	Threshold Gate Charge			1.8		
$Q_{GS}$	Gate-to-Source Charge			3.5		
$Q_{GD}$	Gate-to-Drain Charge			3.3		
$V_{GP}$	Gate Plateau Voltage			3.4		V
$Q_{G(TOT)}$	Total Gate Charge	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		18.2		nC

### SWITCHING CHARACTERISTICS (Note 6)

$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		9.0		$\text{ns}$
$t_r$	Rise Time			33		
$t_{d(OFF)}$	Turn-Off Delay Time			15		
$t_f$	Fall Time			4.0		
$t_{d(ON)}$	Turn-On Delay Time	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		7.0		$\text{ns}$
$t_r$	Rise Time			26		
$t_{d(OFF)}$	Turn-Off Delay Time			19		
$t_f$	Fall Time			3.0		

### DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Forward Diode Voltage	$V_{GS} = 0\text{ V}, I_S = 10\text{ A}$	$T_J = 25^\circ\text{C}$		0.79	1.1	V
			$T_J = 125^\circ\text{C}$		0.66		
$t_{RR}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$		28.3		$\text{ns}$	
$t_a$	Charge Time			14.5			
$t_b$	Discharge Time			13.8			
$Q_{RR}$	Reverse Recovery Charge			15.3		nC	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

# NVTFS4C08N

## TYPICAL CHARACTERISTICS

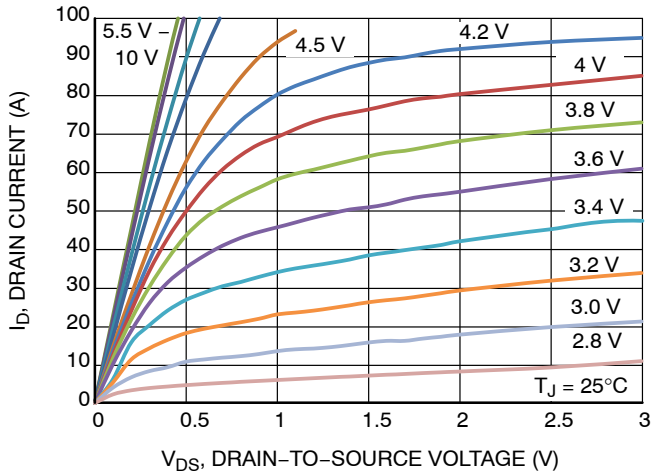


Figure 1. On-Region Characteristics

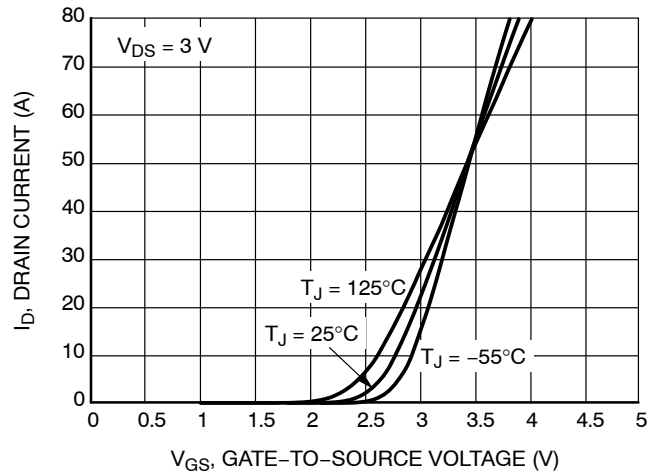


Figure 2. Transfer Characteristics

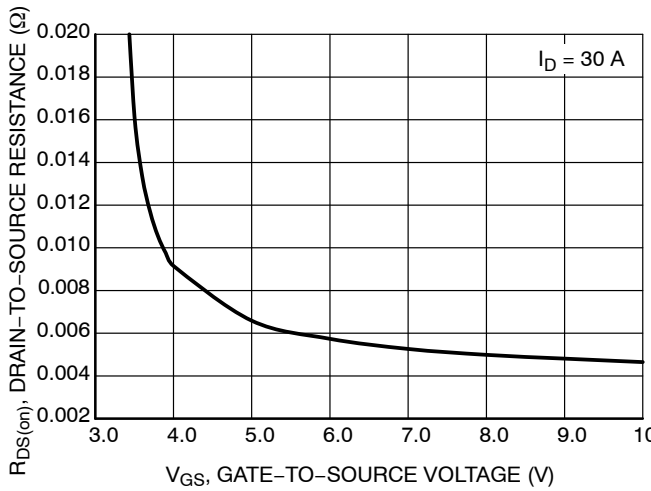


Figure 3. On-Resistance vs.  $V_{GS}$

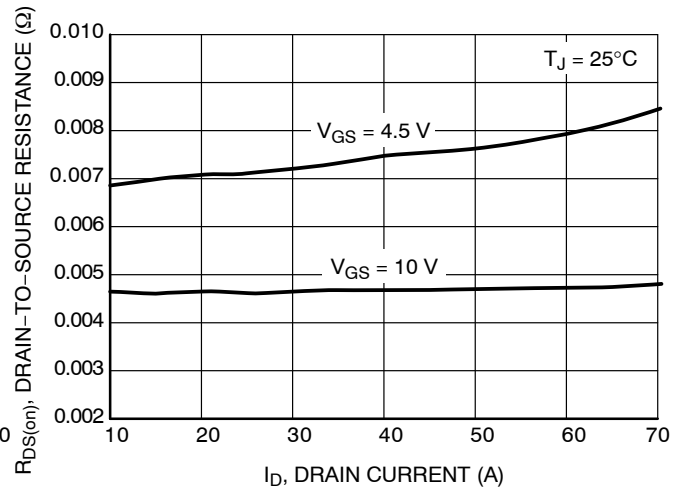


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

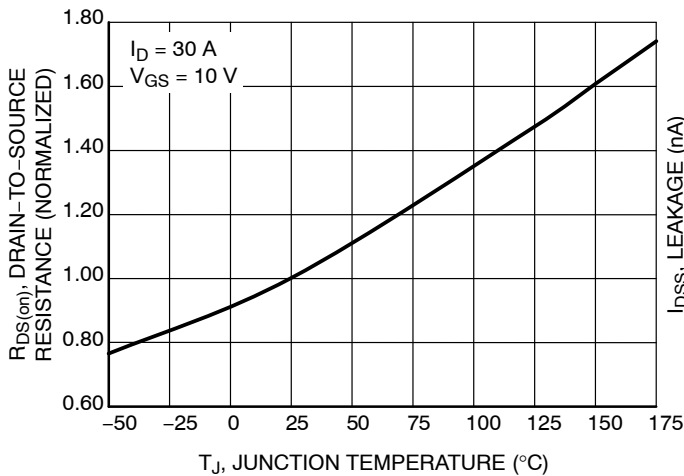


Figure 5. On-Resistance Variation with Temperature

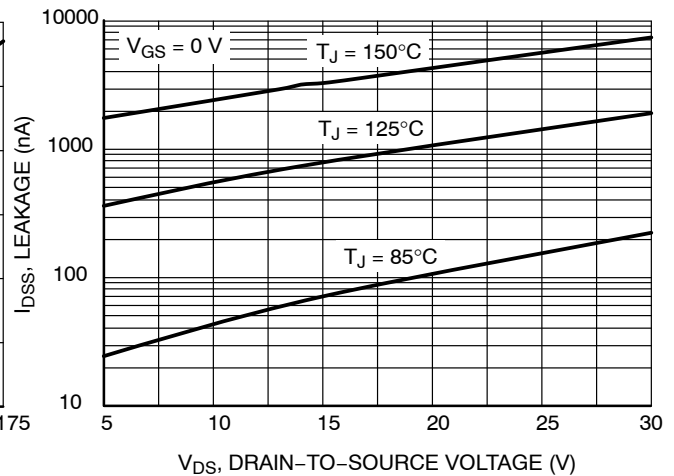


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVTFS4C08N

## TYPICAL CHARACTERISTICS (continued)

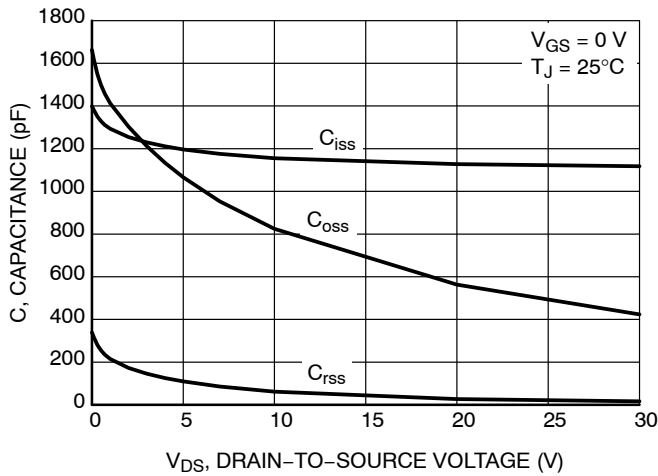


Figure 7. Capacitance Variation

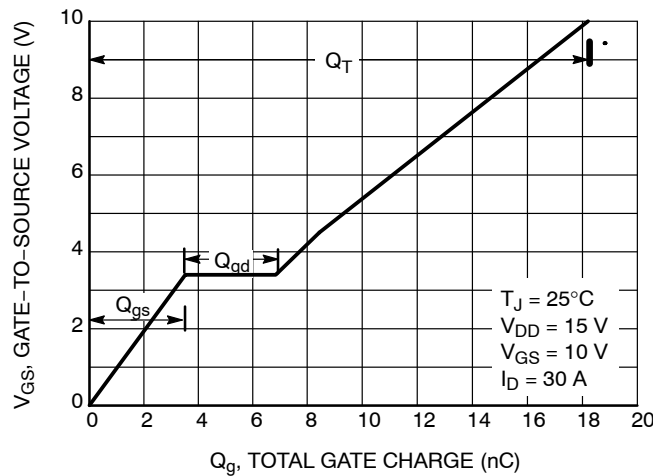


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

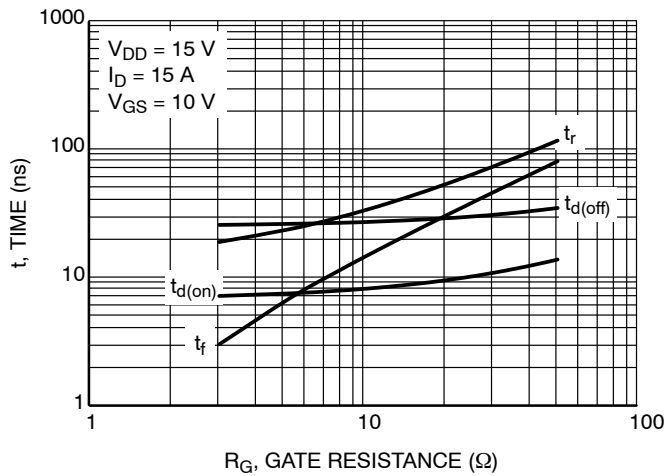


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

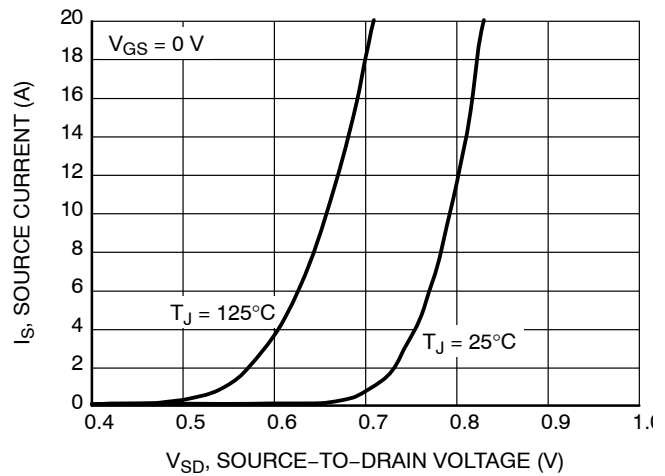


Figure 10. Diode Forward Voltage vs. Current

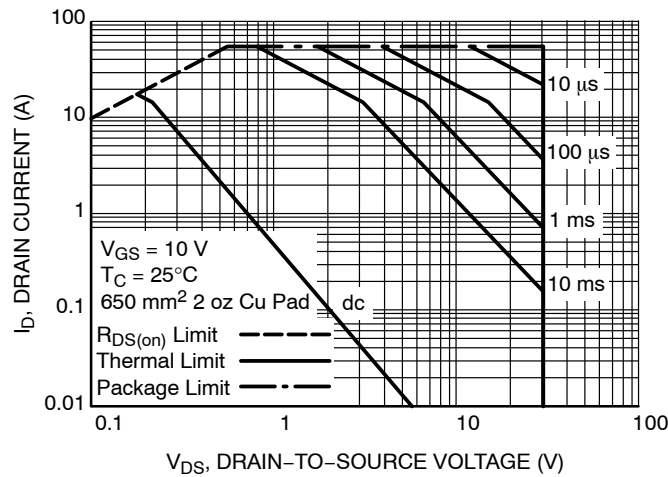


Figure 11. Maximum Rated Forward Biased Safe Operating Area

# NVTFS4C08N

## TYPICAL CHARACTERISTICS (continued)

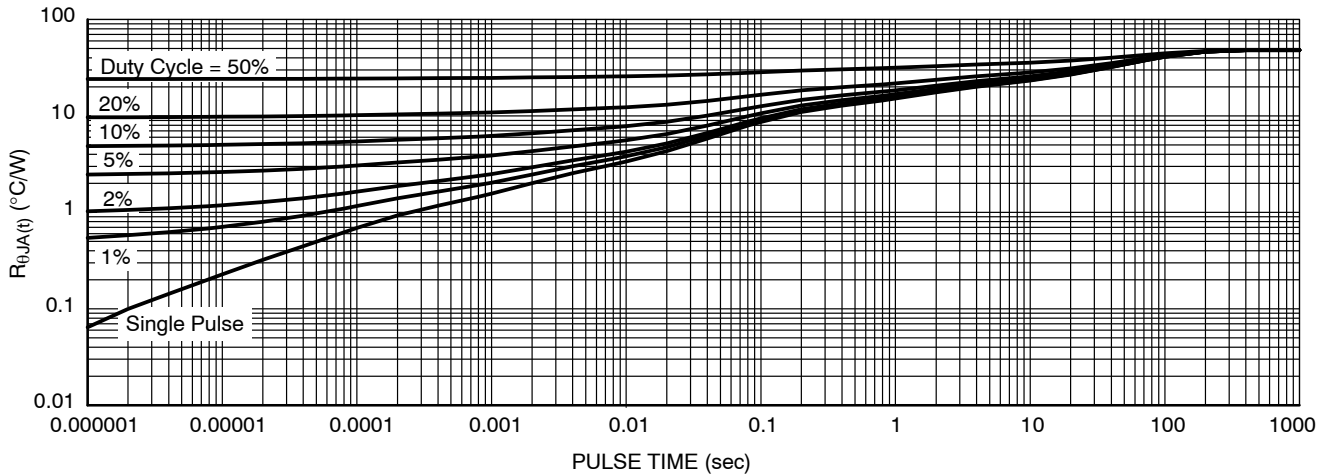


Figure 12. Thermal Response

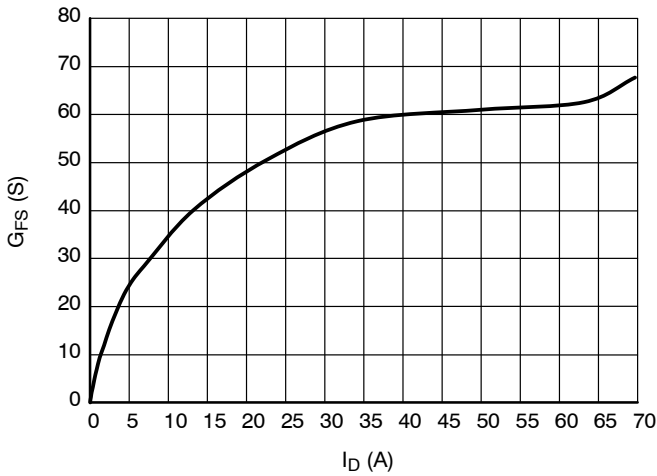


Figure 13.  $G_{FS}$  vs.  $I_D$

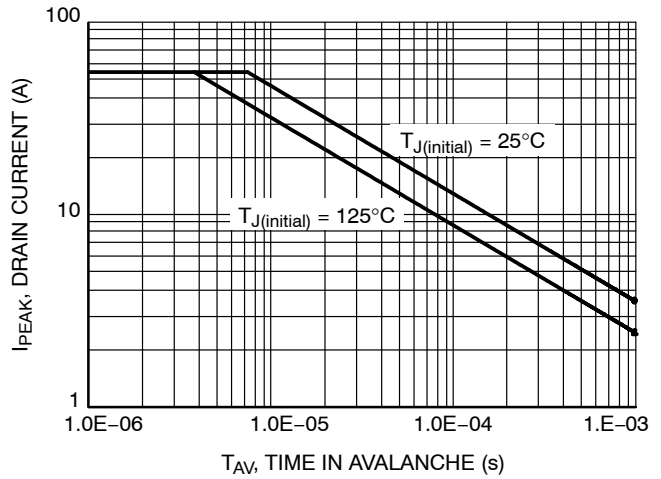


Figure 14. Avalanche Characteristics

### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
NVTFS4C08NTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFS4C08NTWG	WDFN8 (Pb-Free)	5000 / Tape & Reel

### DISCONTINUED (Note 7)

NVTFS4C08NWFTAG	WDFNW8 (Pb-Free)	1500 / Tape & Reel
NVTFS4C08NWFTWG	WDFNW8 (Pb-Free)	5000 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

7. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on [www.onsemi.com](http://www.onsemi.com).



SCALE 2:1

WDFN8 3.3x3.3, 0.65P  
CASE 511AB  
ISSUE D

DATE 23 APR 2012



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0 °	---	12 °	0 °	---	12 °



GENERIC MARKING DIAGRAM\*



- XXXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

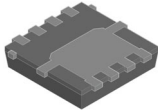
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

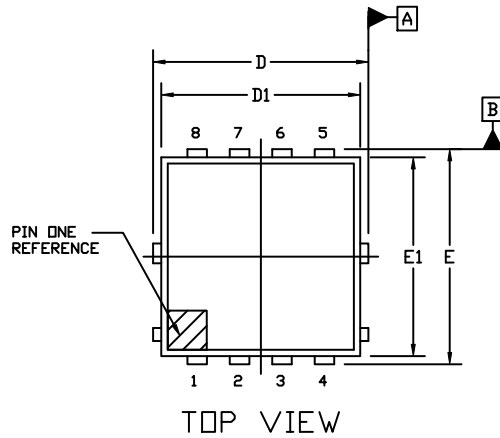
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DESCRIPTION:	WDFN8 3.3X3.3, 0.65P	PAGE 1 OF 1

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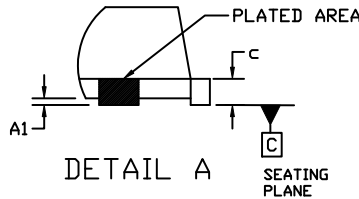


**WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF)**  
CASE 515AN  
ISSUE O

DATE 25 AUG 2020



TOP VIEW

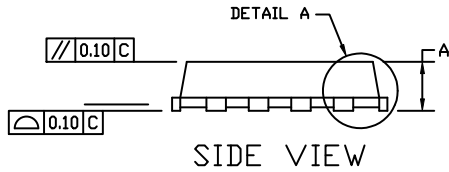


DETAIL A

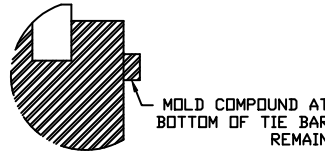
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

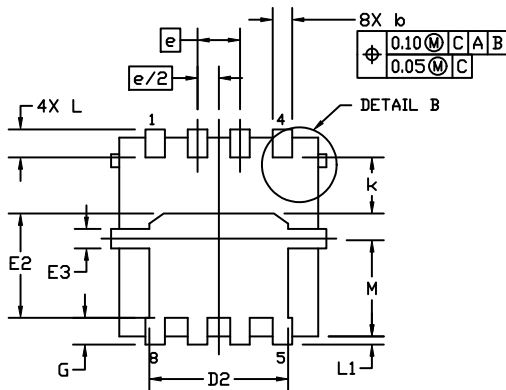
DIM	MILLIMETERS		
	MIN.	NDM.	MAX.
A	0.70	0.75	0.80
A1	0.00	----	0.05
b	0.23	0.30	0.40
c	0.15	0.20	0.25
D	3.05	3.30	3.55
D1	2.95	3.05	3.15
D2	1.98	2.11	2.24
E	3.05	3.30	3.55
E1	2.95	3.05	3.15
E2	1.47	1.60	1.73
E3	0.23	0.30	0.40
e	0.65 BSC		
G	0.30	0.41	0.51
K	0.65	0.80	0.95
L	0.30	0.43	0.59
L1	0.06	0.13	0.20
M	1.40	1.50	1.60



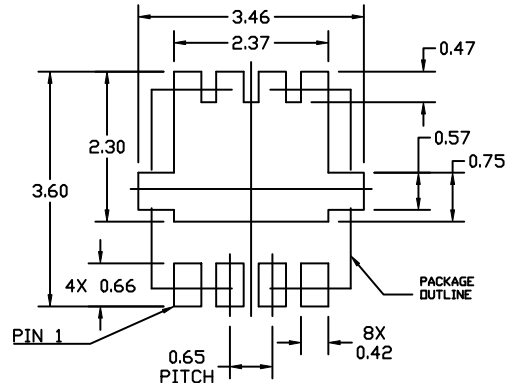
SIDE VIEW



DETAIL B



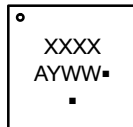
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

(Note: Microdot may be in either location)

<b>DOCUMENT NUMBER:</b>	<b>98AON24556H</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>WDFNW8 3.3x3.3, 0.65P (Full-Cut μ8FL WF)</b>	<b>PAGE 1 OF 1</b>

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