

MOSFET – Power, Single N-Channel, DFN5/DFNW5

60 V, 4.0 mΩ, 100 A

NVMFS5C645NL

Features

- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- NVMFS5C645NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|--|---|------------------------|-----------------------------------|-------------|------|
| Drain-to-Source Voltage | | | V _{DSS} | 60 | V |
| Gate-to-Source Voltage | | | V _{GS} | ±20 | V |
| Continuous Drain Current R _{θJC} (Notes 1, 3) | Steady State | T _C = 25°C | I _D | 100 | A |
| | | T _C = 100°C | | 71 | |
| Power Dissipation R _{θJC} (Note 1) | | T _C = 25°C | P _D | 79 | W |
| | | T _C = 100°C | | 40 | |
| Continuous Drain Current R _{θJA} (Notes 1, 2, 3) | Steady State | T _A = 25°C | I _D | 22 | A |
| | | T _A = 100°C | | 15 | |
| Power Dissipation R _{θJA} (Notes 1, 2) | | T _A = 25°C | P _D | 3.7 | W |
| | | T _A = 100°C | | 1.8 | |
| Pulsed Drain Current | T _A = 25°C, t _p = 10 μs | | I _{DM} | 820 | A |
| Operating Junction and Storage Temperature Range | | | T _J , T _{stg} | –55 to +175 | °C |
| Source Current (Body Diode) | | | I _S | 100 | A |
| Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 5 A) | | | E _{AS} | 185 | mJ |
| Lead Temperature for Soldering Purposes (1/8" from case for 10 s) | | | T _L | 260 | °C |

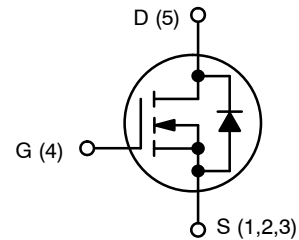
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

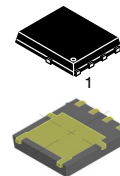
| Parameter | Symbol | Value | Unit |
|---|-----------------|-------|--------------------|
| Junction-to-Case – Steady State | $R_{\theta JC}$ | 1.9 | $^\circ\text{C/W}$ |
| Junction-to-Ambient – Steady State (Note 2) | $R_{\theta JA}$ | 41 | |

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

| $V_{(BR)DS}$ | $R_{DS(ON)}$ MAX | I_D MAX |
|--------------|------------------|-----------|
| 60 V | 4.0 mΩ @ 10 V | 100 A |
| | 5.7 mΩ @ 4.5 V | |



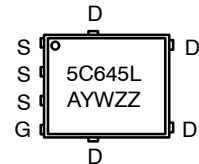
N-CHANNEL MOSFET



DFN5
CASE 488AA

DFNW5
CASE 507BA

MARKING DIAGRAM



5C645L = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NVMFS5C645NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------|--------|----------------|-----|-----|-----|------|
|-----------|--------|----------------|-----|-----|-----|------|

OFF CHARACTERISTICS

| | | | | | | |
|---|-------------------|---|----------------------------------|------|-----|----------------------|
| Drain-to-Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 60 | | | V |
| Drain-to-Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | 15.5 | | mV/ $^\circ\text{C}$ |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 48\text{ V}$ | $T_J = 25\text{ }^\circ\text{C}$ | | 10 | μA |
| | | | $T_J = 125^\circ\text{C}$ | | 250 | |
| Gate-to-Source Leakage Current | I_{GSS} | $V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$ | | | 100 | nA |

ON CHARACTERISTICS (Note 4)

| | | | | | | |
|-----------------------------------|------------------|--|-----|------|-----|----------------------|
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}, I_D = 80\text{ }\mu\text{A}$ | 1.2 | | 2.0 | V |
| Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | -4.9 | | mV/ $^\circ\text{C}$ |
| Drain-to-Source On Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 50\text{ A}$ | | 3.3 | 4.0 | $\text{m}\Omega$ |
| | | $V_{GS} = 4.5\text{ V}, I_D = 50\text{ A}$ | | 4.6 | 5.7 | |
| Forward Transconductance | g_{FS} | $V_{DS} = 15\text{ V}, I_D = 50\text{ A}$ | | 105 | | S |

CHARGES, CAPACITANCES & GATE RESISTANCE

| | | | | | | |
|------------------------------|--------------|--|--|------|--|----|
| Input Capacitance | C_{ISS} | $V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 50\text{ V}$ | | 2200 | | pF |
| Output Capacitance | C_{OSS} | | | 900 | | |
| Reverse Transfer Capacitance | C_{RSS} | | | 17 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$ | | 16 | | nC |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS} = 10\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$ | | 34 | | |
| Threshold Gate Charge | $Q_{G(TH)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}; I_D = 50\text{ A}$ | | 1.5 | | |
| Gate-to-Source Charge | Q_{GS} | | | 5.6 | | |
| Gate-to-Drain Charge | Q_{GD} | | | 5.1 | | |
| Plateau Voltage | V_{GP} | | | 2.8 | | V |

SWITCHING CHARACTERISTICS (Note 5)

| | | | | | | |
|---------------------|--------------|---|--|-----|--|----|
| Turn-On Delay Time | $t_{d(ON)}$ | $V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}, I_D = 50\text{ A}, R_G = 2.5\text{ }\Omega$ | | 10 | | ns |
| Rise Time | t_r | | | 15 | | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | 24 | | |
| Fall Time | t_f | | | 5.0 | | |

DRAIN-SOURCE DIODE CHARACTERISTICS

| | | | | | | | |
|-------------------------|----------|---|-----------------------------|--|------|-----|----|
| Forward Diode Voltage | V_{SD} | $V_{GS} = 0\text{ V},$ $I_S = 50\text{ A}$ | $T_J = 25^{\circ}\text{C}$ | | 0.88 | 1.2 | V |
| | | | $T_J = 125^{\circ}\text{C}$ | | 0.78 | | |
| Reverse Recovery Time | t_{RR} | $V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 50\text{ A}$ | | | 41 | | ns |
| Charge Time | t_a | | | | 21 | | |
| Discharge Time | t_b | | | | 20 | | |
| Reverse Recovery Charge | Q_{RR} | | | | | 32 | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

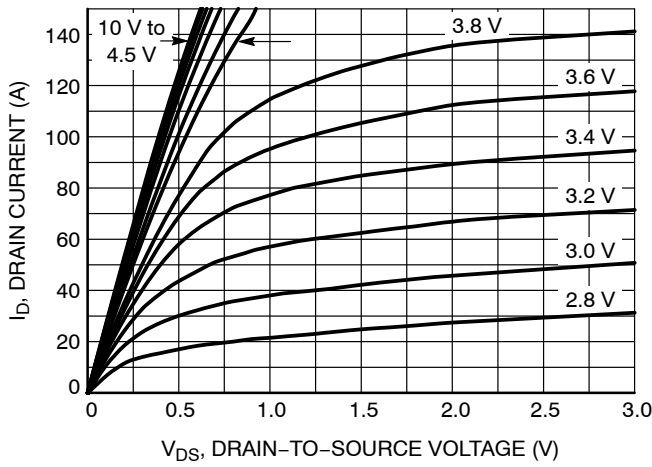


Figure 1. On-Region Characteristics

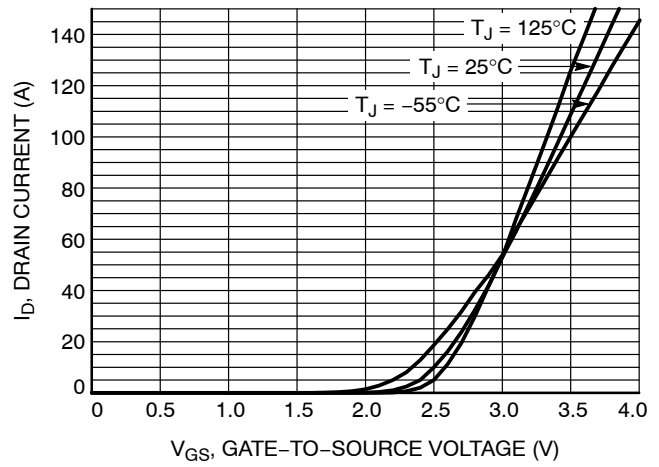


Figure 2. Transfer Characteristics

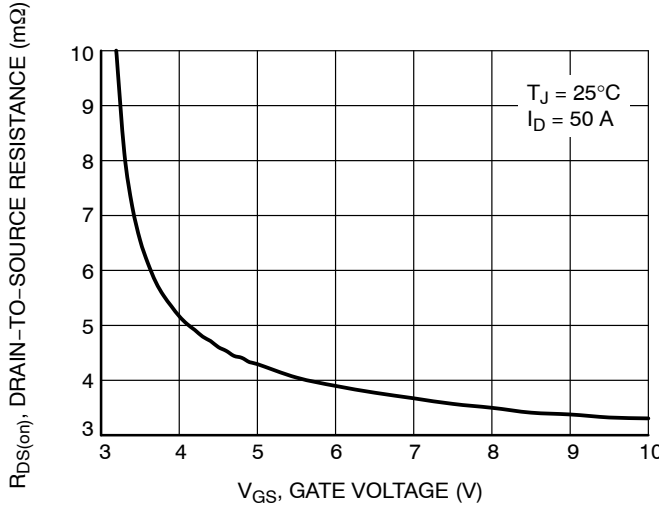


Figure 3. On-Resistance vs. Gate-to-Source Voltage

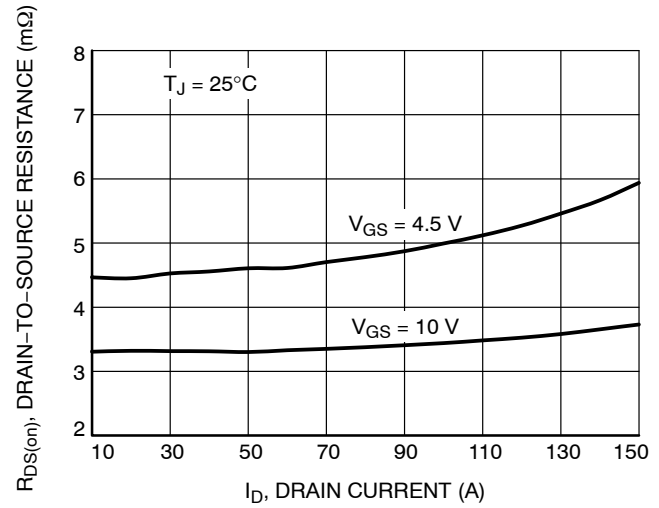


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

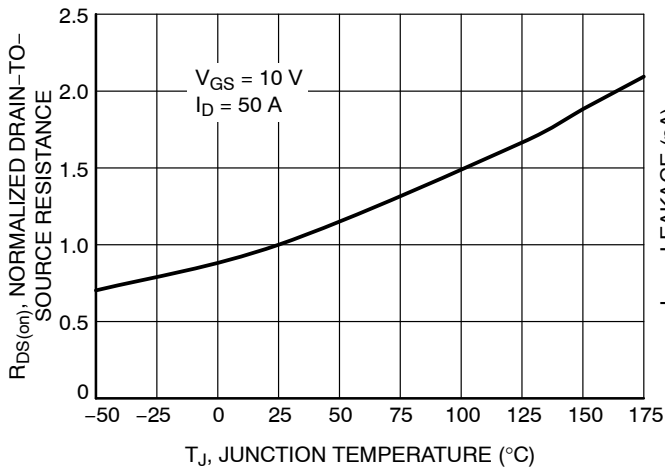


Figure 5. On-Resistance Variation with Temperature

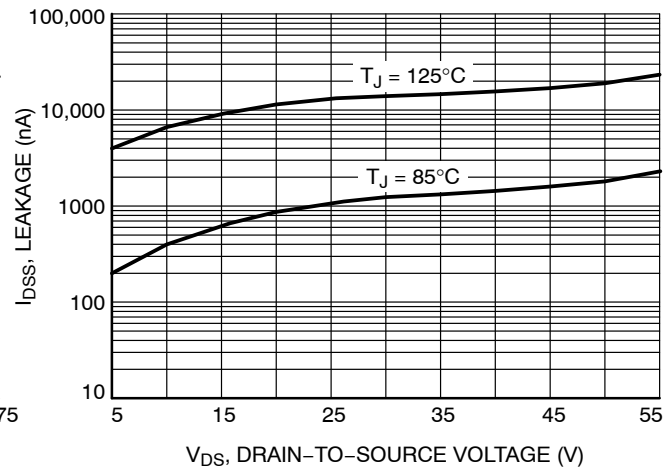


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

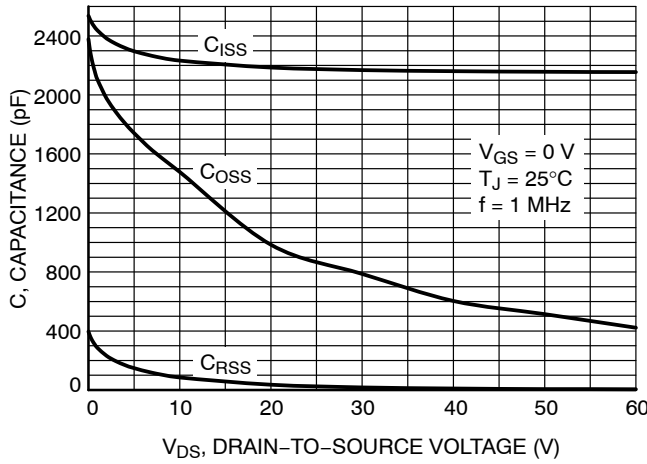


Figure 7. Capacitance Variation

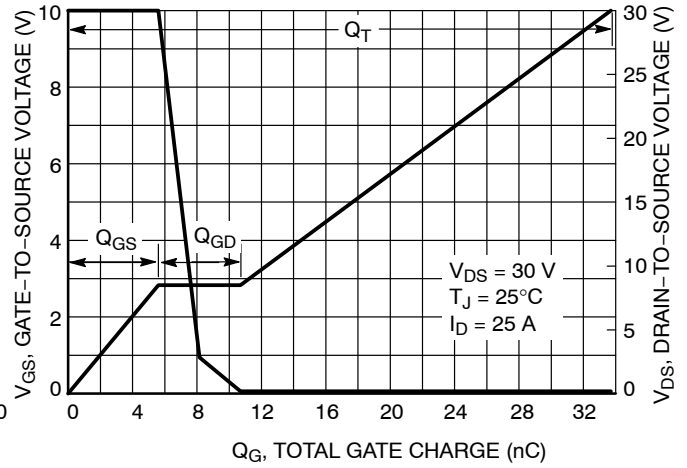


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

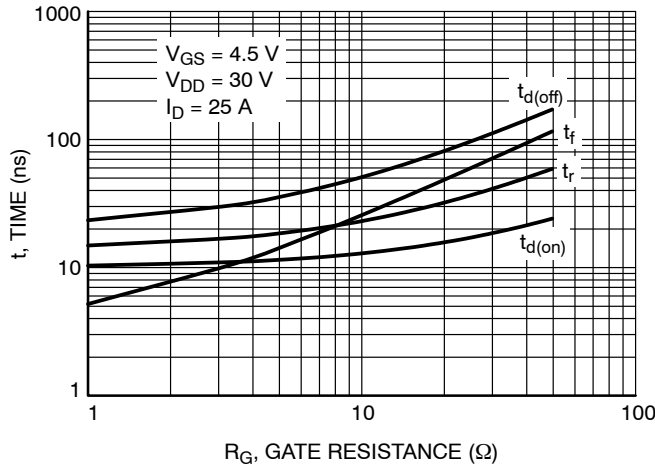


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

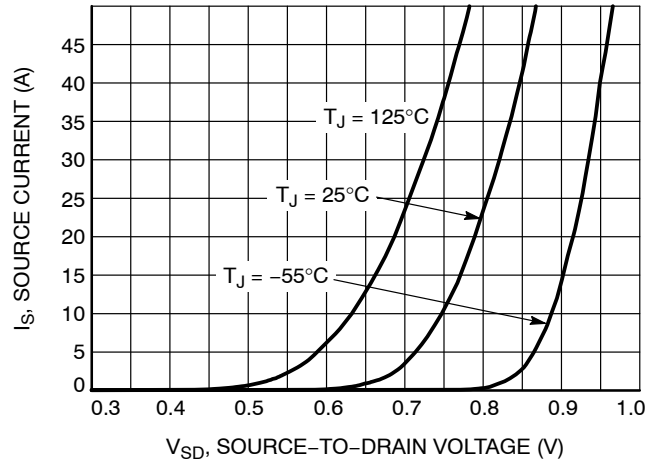


Figure 10. Diode Forward Voltage vs. Current

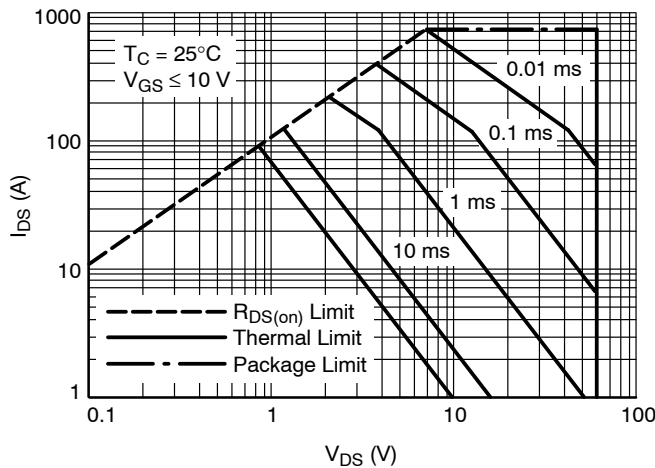


Figure 11. Safe Operating Area

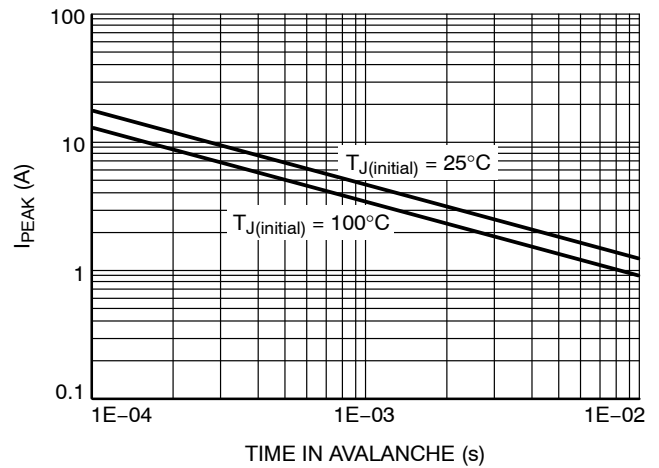


Figure 12. I_{PEAK} vs. Time in Avalanche

NVMFS5C645NL

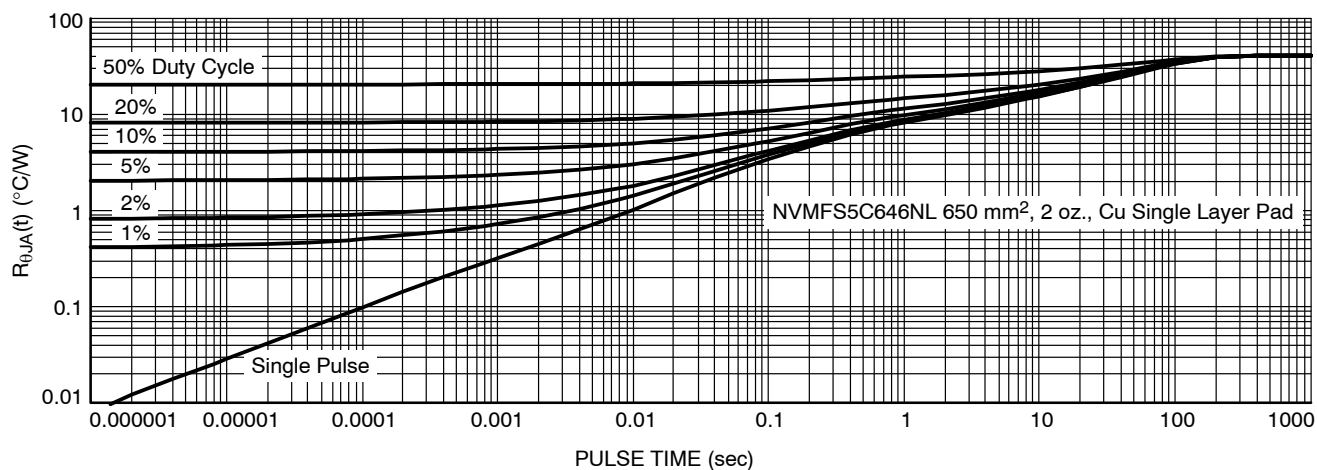


Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

| Device | Marking | Package | Shipping [†] |
|---------------------|---------|-------------------------------------|-----------------------|
| NVMFS5C645NLT1G | 5C645L | DFN5 (Pb-Free) | 1500 / Tape & Reel |
| NVMFS5C645NLWFT1G | 645LWF | DFNW5 (Pb-Free, Wettable Flanks) | 1500 / Tape & Reel |
| NVMFS5C645NLT3G | 5C645L | DFN5 (Pb-Free) | 5000 / Tape & Reel |
| NVMFS5C645NLWFT3G | 645LWF | DFNW5 (Pb-Free, Wettable Flanks) | 5000 / Tape & Reel |
| NVMFS5C645NLAFT1G | 5C645L | DFN5 (Pb-Free) | 1500 / Tape & Reel |
| NVMFS5C645NLWFAFT1G | 645LWF | DFNW5 (Pb-Free, Wettable Flanks) | 1500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 2:1

DFN5 5x6, 1.27P
(SO-8FL)
CASE 488AA
ISSUE N

DATE 25 JUN 2018

NOTES:

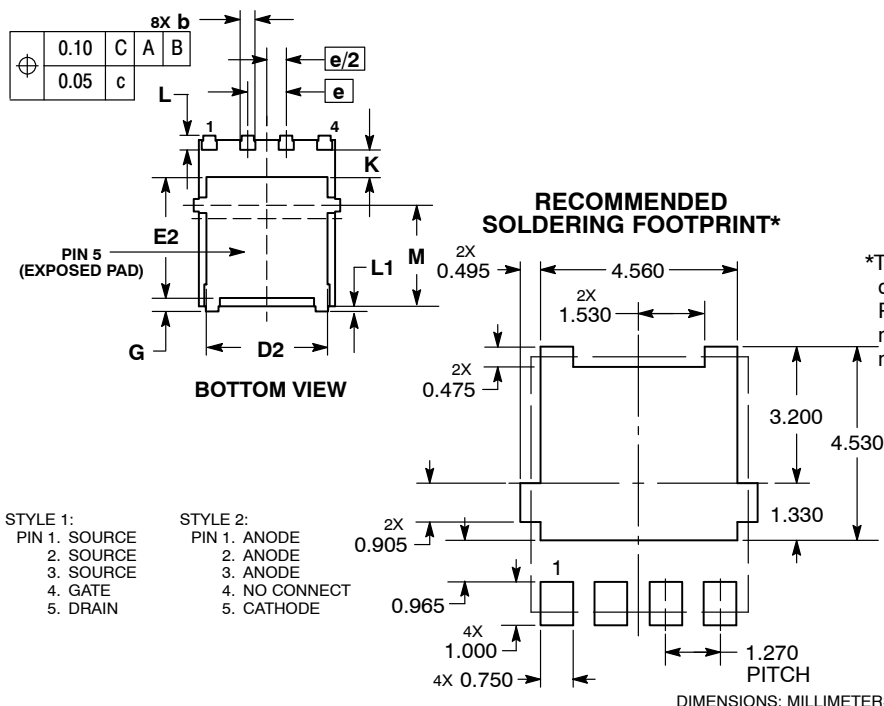
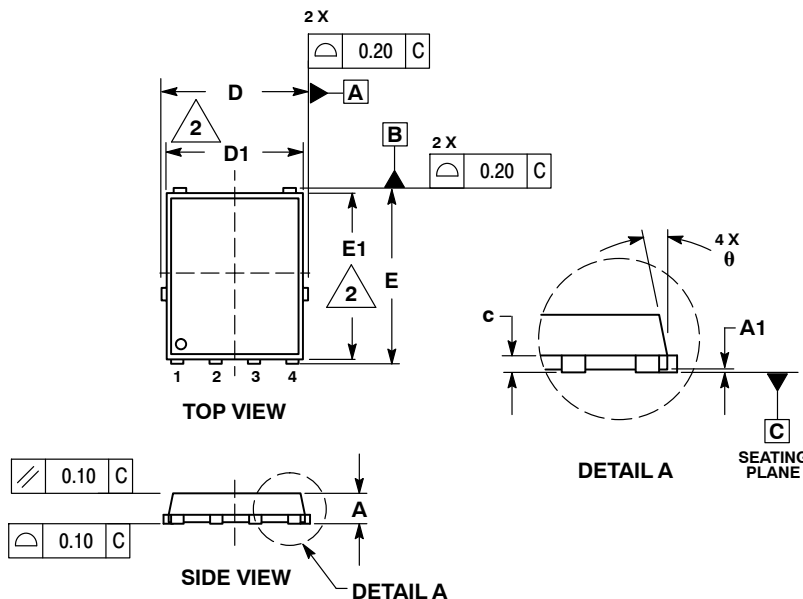
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| DIM | MILLIMETERS | | |
|-----|-------------|-------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | 5.00 | 5.15 | 5.30 |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 | 4.20 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.45 | 3.65 | 3.85 |
| e | 1.27 BSC | | |
| G | 0.51 | 0.575 | 0.71 |
| K | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.575 | 0.71 |
| L1 | 0.125 REF | | |
| M | 3.00 | 3.40 | 3.80 |
| θ | 0° | --- | 12° |

GENERIC
MARKING DIAGRAM*


XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

STYLE 2:
PIN 1. ANODE
2. ANODE
3. ANODE
4. NO CONNECT
5. CATHODE

DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DFNW5 4.90x5.90x1.00, 1.27P
CASE 507BA
ISSUE C

DATE 19 SEP 2024



TOP VIEW



SIDE VIEW



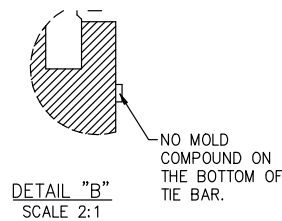
BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



DETAIL "A"
SCALE 2:1



DETAIL "B"
SCALE 2:1

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | --- | 0.05 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.23 | 0.28 | 0.33 |
| D | 5.00 | 5.15 | 5.30 |
| D1 | 4.70 | 4.90 | 5.10 |
| D2 | 3.80 | 4.00 | 4.20 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.70 | 5.90 | 6.10 |
| E2 | 3.45 | 3.65 | 3.85 |
| E3 | 3.00 | 3.40 | 3.80 |
| e | 1.27 BSC | | |
| k | 1.20 | 1.35 | 1.50 |
| L | 0.51 | 0.57 | 0.71 |
| L2 | 0.15 REF. | | |
| θ | 0° | 6° | 12° |



RECOMMENDED MOUNTING FOOTPRINT*
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

GENERIC
MARKING DIAGRAM*



XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
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