

# MOSFET – Power, Single N-Channel

40 V, 0.82 mΩ, 330 A

## NVMFS5C410NL

### Features

- Small Footprint (5x6 mm) for Compact Design
- Low  $R_{DS(on)}$  to Minimize Conduction Losses
- Low  $Q_G$  and Capacitance to Minimize Driver Losses
- NVMFS5C410NLWF – Wettable Flank Option for Enhanced Optical Inspection
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

| Symbol            | Parameter  | Value   | Unit             |
|-------------------|--|---|------------------|
| $V_{DS}$          | Drain-to-Source Voltage  | 40  | V                |
| $V_{GS}$          | Gate-to-Source Voltage   | $\pm 20$  | V                |
| $I_D$             | Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)                        | Steady State                                      | A                |
|                   |  | $T_C = 25^\circ\text{C}$                          |                  |
|                   |  | $T_C = 100^\circ\text{C}$                         |                  |
| $P_D$             | Power Dissipation $R_{\theta JC}$ (Note 1)                                   | Steady State                                      | W                |
|                   |  | $T_C = 25^\circ\text{C}$                          |                  |
|                   |  | $T_C = 100^\circ\text{C}$                         |                  |
| $I_D$             | Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)                     | Steady State                                      | A                |
|                   |  | $T_A = 25^\circ\text{C}$                          |                  |
|                   |  | $T_A = 100^\circ\text{C}$                         |                  |
| $P_D$             | Power Dissipation $R_{\theta JA}$ (Notes 1, 2)                               | Steady State                                      | W                |
|                   |  | $T_A = 25^\circ\text{C}$                          |                  |
|                   |  | $T_A = 100^\circ\text{C}$                         |                  |
| $I_{DM}$          | Pulsed Drain Current   | $T_A = 25^\circ\text{C}$ , $t_p = 10 \mu\text{s}$ | A                |
| $T_J$ , $T_{stg}$ | Operating Junction and Storage Temperature Range                             | $-55$ to $+175$                                   | $^\circ\text{C}$ |
| $I_S$             | Source Current (Body Diode)  | 169   | A                |
| $E_{AS}$          | Single Pulse Drain-to-Source Avalanche Energy ( $I_{L(pk)} = 29 \text{ A}$ ) | 706   | mJ               |
| $T_L$             | Lead Temperature for Soldering Purposes ( $1/8"$ from case for 10 s)         | 260   | $^\circ\text{C}$ |

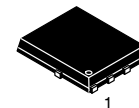
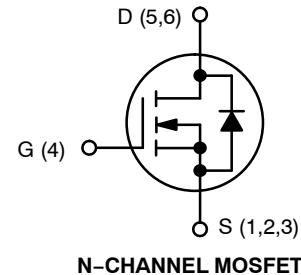
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL RESISTANCE MAXIMUM RATINGS

| Symbol          | Parameter                                   | Value | Unit                      |
|-----------------|---|-------|---------------------------|
| $R_{\theta JC}$ | Junction-to-Case – Steady State             | 0.9   | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Junction-to-Ambient – Steady State (Note 2) | 39    |                           |

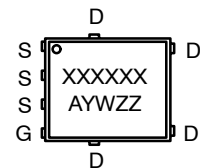
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm<sup>2</sup>, 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.

| $V_{(BR)DSS}$ | $R_{DS(ON)} \text{ MAX}$ | $I_D \text{ MAX}$ |
|---------------|--------------------------|-------------------|
| 40 V          | 0.82 mΩ @ 10 V           | 330 A             |
|               | 1.2 mΩ @ 4.5 V           |                   |



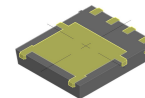
DFN5  
(SO-8FL)  
CASE 488AA  
STYLE 1

### MARKING DIAGRAMS



XXXXXX = 5C410L  
(NVMFS5C410NL) or  
410LWF  
(NVMFS5C410NLWF)

A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability



DFNW5  
(SO-8FL WF)  
CASE 507BE



XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

### ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 5.

# NVMFS5C410NL

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise specified)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|--------|-----------|----------------|-----|-----|-----|------|
|--------|-----------|----------------|-----|-----|-----|------|

### OFF CHARACTERISTICS

|                                      |   |  |   |      |           |       |
|--------------------------------------|---|--|---|------|-----------|-------|
| V <sub>(BR)DSS</sub>                 | Drain-to-Source Breakdown Voltage                         | V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA   | 40  |      |           | V     |
| V <sub>(BR)DSS</sub> /T <sub>J</sub> | Drain-to-Source Breakdown Voltage Temperature Coefficient |  |   | 21.2 |           | mV/°C |
| I <sub>DSS</sub>                     | Zero Gate Voltage Drain Current                           | V <sub>GS</sub> = 0 V,<br>V <sub>DS</sub> = 40 V | T <sub>J</sub> = 25°C<br>T <sub>J</sub> = 125°C |      | 10<br>250 | μA    |
| I <sub>GSS</sub>                     | Gate-to-Source Leakage Current                            | V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V    |   |      | 100       | nA    |

### ON CHARACTERISTICS (Note 4)

|                                     |                                   |   |  |              |             |       |
|-------------------------------------|-----------------------------------|---|--|--------------|-------------|-------|
| V <sub>GS(TH)</sub>                 | Gate Threshold Voltage            | V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA | 1.2  |              | 2.0         | V     |
| V <sub>GS(TH)</sub> /T <sub>J</sub> | Threshold Temperature Coefficient |   |  | -5.75        |             | mV/°C |
| R <sub>DS(on)</sub>                 | Drain-to-Source On Resistance     | V <sub>GS</sub> = 10 V<br>V <sub>GS</sub> = 4.5 V           | I <sub>D</sub> = 50 A<br>I <sub>D</sub> = 50 A | 0.65<br>0.95 | 0.82<br>1.2 | mΩ    |
| g <sub>FS</sub>                     | Forward Transconductance          | V <sub>DS</sub> = 15 V, I <sub>D</sub> = 50 A               |  | 190          |             | S     |

### CHARGES, CAPACITANCES & GATE RESISTANCE

|                     |                              |  |  |      |  |    |
|---------------------|------------------------------|--|--|------|--|----|
| C <sub>ISS</sub>    | Input Capacitance            | V <sub>GS</sub> = 0 V, f = 1 MHz, V <sub>DS</sub> = 25 V               |  | 8862 |  | pF |
| C <sub>OSS</sub>    | Output Capacitance           |  |  | 4156 |  |    |
| C <sub>RSS</sub>    | Reverse Transfer Capacitance |  |  | 116  |  |    |
| Q <sub>G(TOT)</sub> | Total Gate Charge            | V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 20 V; I <sub>D</sub> = 50 A |  | 66   |  | nC |
| Q <sub>G(TOT)</sub> | Total Gate Charge            | V <sub>GS</sub> = 10 V, V <sub>DS</sub> = 20 V; I <sub>D</sub> = 50 A  |  | 143  |  |    |
| Q <sub>G(TH)</sub>  | Threshold Gate Charge        | V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 20 V; I <sub>D</sub> = 50 A |  | 6.75 |  |    |
| Q <sub>GS</sub>     | Gate-to-Source Charge        |  |  | 21.4 |  |    |
| Q <sub>GD</sub>     | Gate-to-Drain Charge         |  |  | 22   |  |    |
| V <sub>GP</sub>     | Plateau Voltage              |  |  | 2.7  |  | V  |

### SWITCHING CHARACTERISTICS (Note 5)

|                     |                     |   |  |     |  |    |
|---------------------|---------------------|---|--|-----|--|----|
| t <sub>d(ON)</sub>  | Turn-On Delay Time  | V <sub>GS</sub> = 4.5 V, V <sub>DS</sub> = 20 V,<br>I <sub>D</sub> = 50 A, R <sub>G</sub> = 1.0 Ω |  | 20  |  | ns |
| t <sub>r</sub>      | Rise Time           |   |  | 130 |  |    |
| t <sub>d(OFF)</sub> | Turn-Off Delay Time |   |  | 66  |  |    |
| t <sub>f</sub>      | Fall Time           |   |  | 177 |  |    |

### DRAIN-SOURCE DIODE CHARACTERISTICS

|                 |                         |   |   |  |             |     |    |
|-----------------|-------------------------|---|---|--|-------------|-----|----|
| V <sub>SD</sub> | Forward Diode Voltage   | V <sub>GS</sub> = 0 V,<br>I <sub>S</sub> = 50 A                                 | T <sub>J</sub> = 25°C<br>T <sub>J</sub> = 125°C |  | 0.73<br>0.6 | 1.2 | V  |
| t <sub>RR</sub> | Reverse Recovery Time   | V <sub>GS</sub> = 0 V, dI <sub>S</sub> /dt = 100 A/μs,<br>I <sub>S</sub> = 50 A |   |  | 79.5        |     | ns |
| t <sub>a</sub>  | Charge Time             |   |   |  | 39          |     |    |
| t <sub>b</sub>  | Discharge Time          |   |   |  | 40.5        |     |    |
| Q <sub>RR</sub> | Reverse Recovery Charge |   |   |  | 126         |     | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

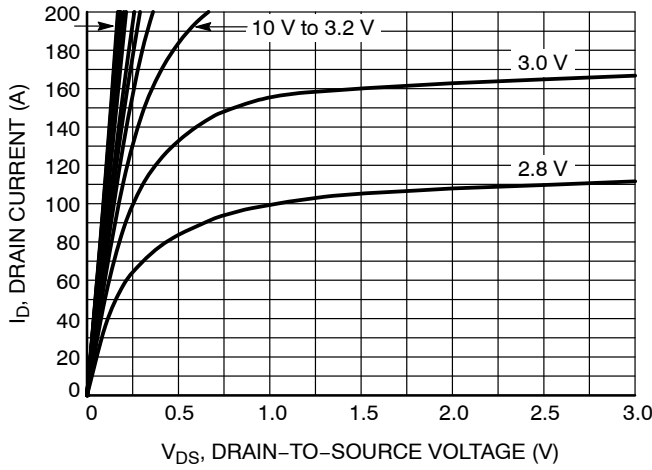


Figure 1. On-Region Characteristics

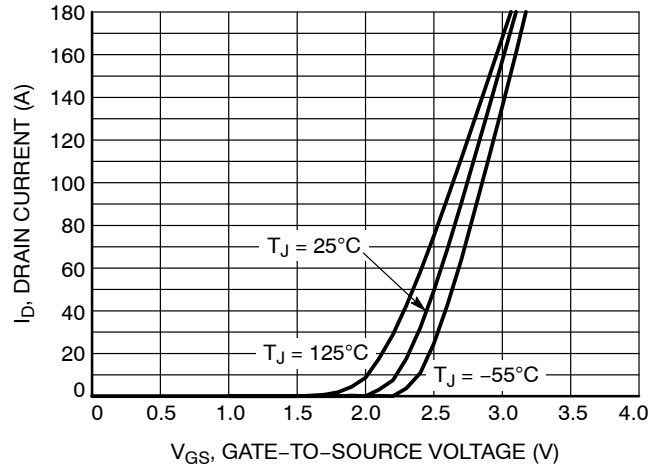


Figure 2. Transfer Characteristics

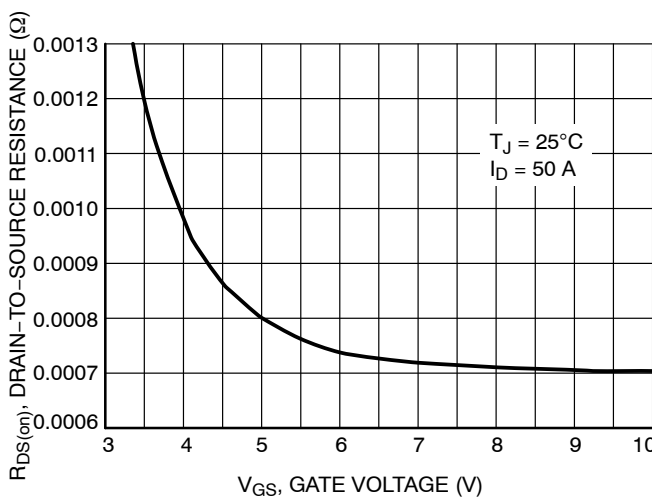


Figure 3. On-Resistance vs. Gate-to-Source Voltage

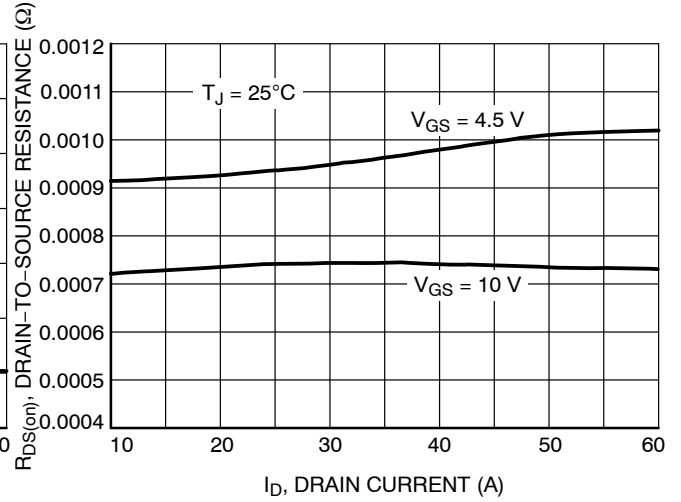


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

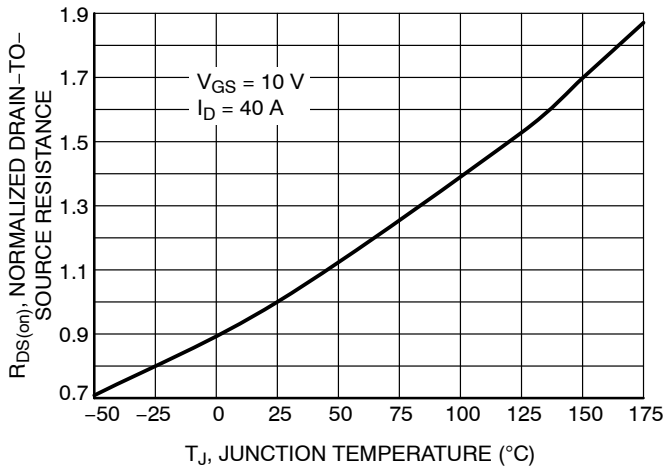


Figure 5. On-Resistance Variation with Temperature

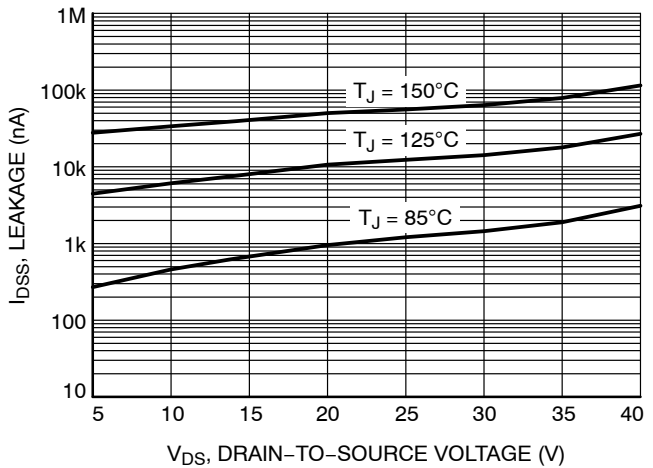


Figure 6. Drain-to-Source Leakage Current vs. Voltage

# NVMFS5C410NL

## TYPICAL CHARACTERISTICS (continued)

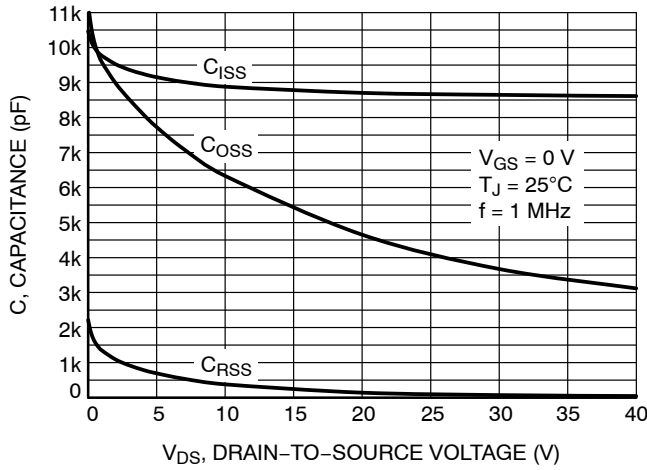


Figure 7. Capacitance Variation

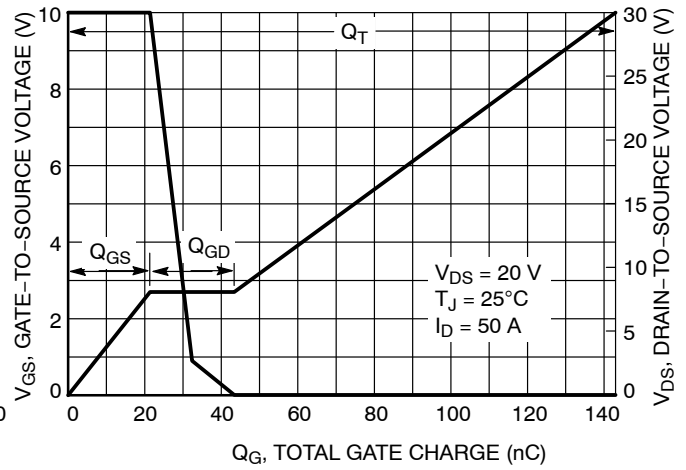


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

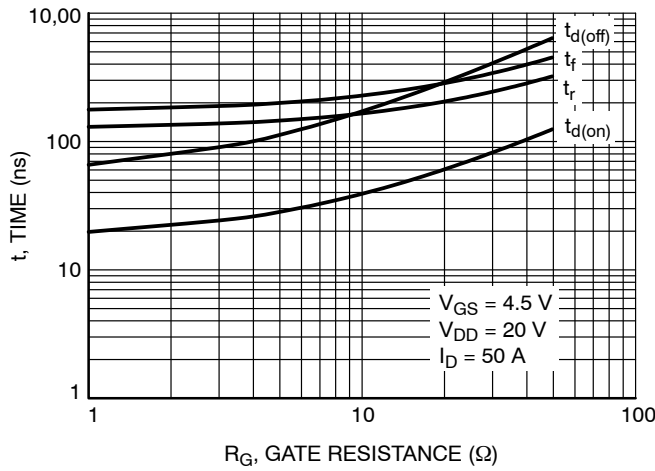


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

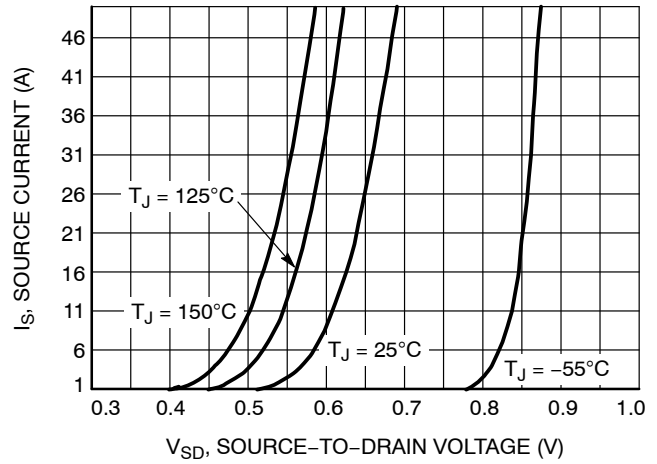


Figure 10. Diode Forward Voltage vs. Current

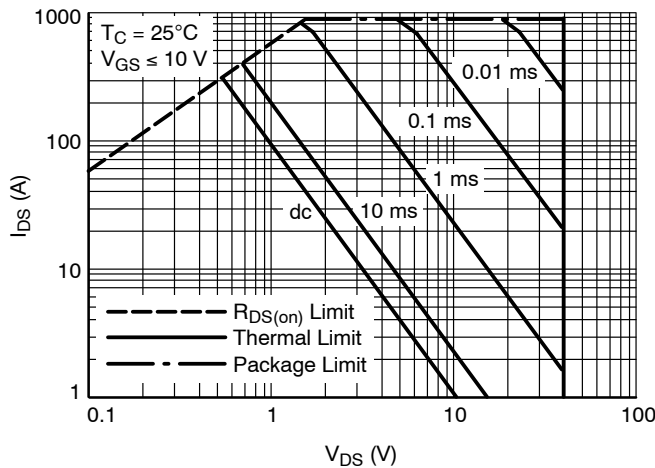


Figure 11. Safe Operating Area

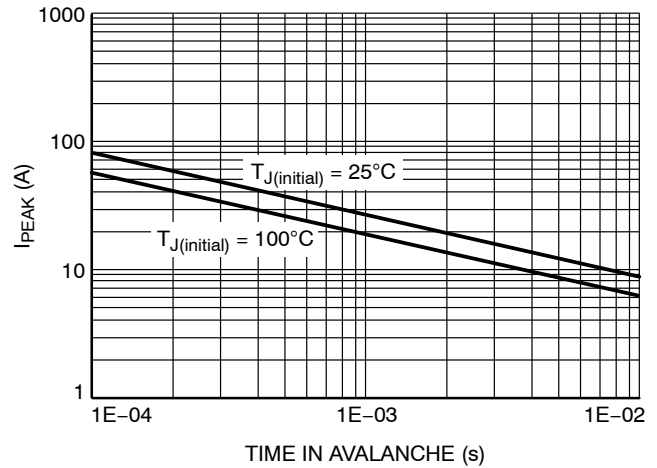


Figure 12.  $I_{PEAK}$  vs. Time in Avalanche

# NVMFS5C410NL

## TYPICAL CHARACTERISTICS (continued)

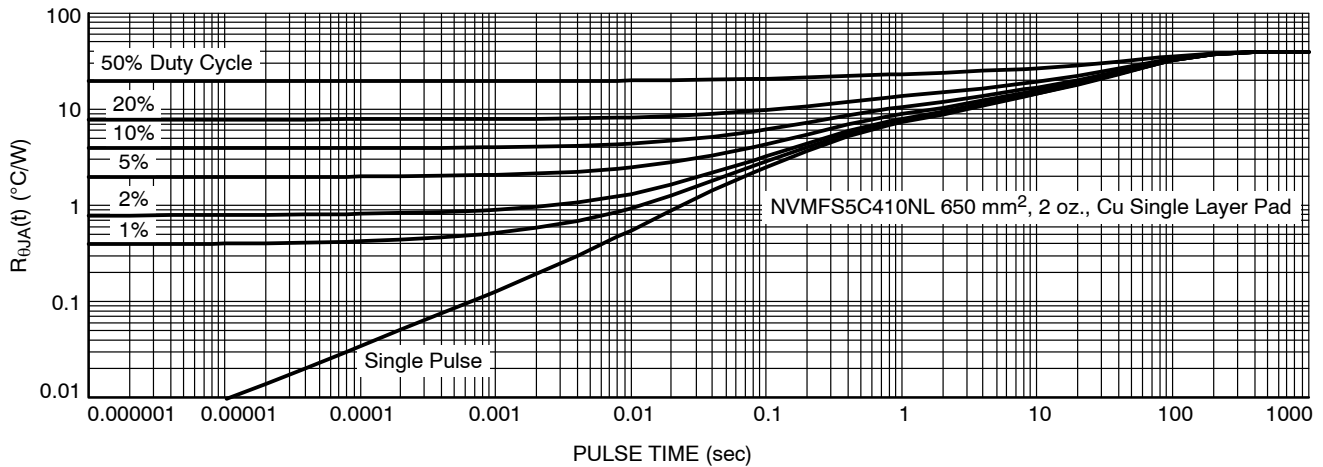


Figure 13. Thermal Characteristics

### DEVICE ORDERING INFORMATION

| Device              | Marking | Package  | Shipping†          |
|---------------------|---------|--|--------------------|
| NVMFS5C410NLT1G     | 5C410L  | DFN5<br>(Pb-Free)  | 1500 / Tape & Reel |
| NVMFS5C410NLWFT1G   | 410LWF  | DFNW5<br>(Pb-Free, Wettable Flanks,<br>Full-cut SO-8FL WF) | 1500 / Tape & Reel |
| NVMFS5C410NLWFT3G   | 410LWF  | DFNW5<br>(Pb-Free, Wettable Flanks,<br>Full-cut SO-8FL WF) | 5000 / Tape & Reel |
| NVMFS5C410NLAFT1G   | 5C410L  | DFN5<br>(Pb-Free)  | 1500 / Tape & Reel |
| NVMFS5C410NLWFAFT1G | 410LWF  | DFNW5<br>(Pb-Free, Wettable Flanks,<br>Full-cut SO-8FL WF) | 1500 / Tape & Reel |
| NVMFS5C410NLWFET1G  | 410LWF  | DFNW5<br>(Full-cut SO-8FL WF)                              | 1500 / Tape & Reel |
| NVMFS5C410NLWFET3G  | 410LWF  | DFNW5<br>(Full-cut SO-8FL WF)                              | 5000 / Tape & Reel |

### DISCONTINUED (Note 6)

|                 |        |                   |                    |
|-----------------|--------|-------------------|--------------------|
| NVMFS5C410NLT3G | 5C410L | DFN5<br>(Pb-Free) | 5000 / Tape & Reel |
|-----------------|--------|-------------------|--------------------|

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

6. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on [www.onsemi.com](http://www.onsemi.com).



SCALE 2:1

**DFN5 5x6, 1.27P**  
**(SO-8FL)**  
**CASE 488AA**  
**ISSUE N**

DATE 25 JUN 2018



## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

| DIM | MILLIMETERS |       |      |
|-----|-------------|-------|------|
|     | MIN         | NOM   | MAX  |
| A   | 0.90        | 1.00  | 1.10 |
| A1  | 0.00        | ---   | 0.05 |
| b   | 0.33        | 0.41  | 0.51 |
| c   | 0.23        | 0.28  | 0.33 |
| D   | 5.00        | 5.15  | 5.30 |
| D1  | 4.70        | 4.90  | 5.10 |
| D2  | 3.80        | 4.00  | 4.20 |
| E   | 6.00        | 6.15  | 6.30 |
| E1  | 5.70        | 5.90  | 6.10 |
| E2  | 3.45        | 3.65  | 3.85 |
| e   | 1.27 BSC    |       |      |
| G   | 0.51        | 0.575 | 0.71 |
| K   | 1.20        | 1.35  | 1.50 |
| L   | 0.51        | 0.575 | 0.71 |
| L1  | 0.125 REF   |       |      |
| M   | 3.00        | 3.40  | 3.80 |
| θ   | 0°          | ---   | 12°  |

**GENERIC**  
**MARKING DIAGRAM\***


XXXXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
W = Work Week  
ZZ = Lot Traceability

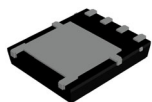
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

|                         |                                 |  |
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| <b>DESCRIPTION:</b>     | <b>DFN5 5x6, 1.27P (SO-8FL)</b> | <b>PAGE 1 OF 1</b>   |

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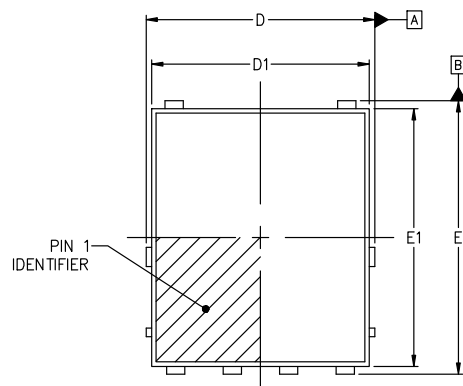


DFNW5 4.90x5.90x1.00, 1.27P

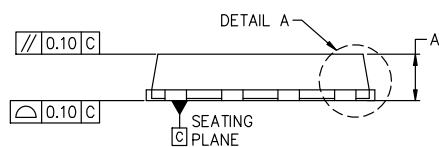
CASE 507BE

ISSUE B

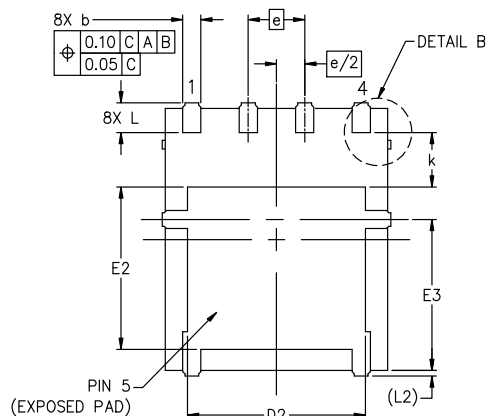
DATE 19 SEP 2024



TOP VIEW

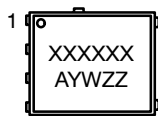


SIDE VIEW



BOTTOM VIEW

GENERIC  
MARKING DIAGRAM\*

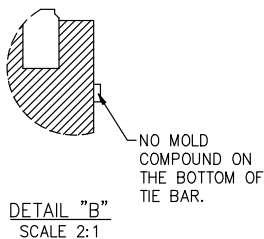
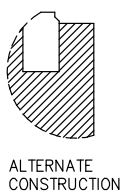
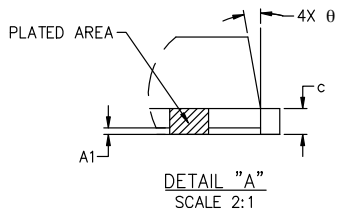


XXXXXX = Specific Device Code  
A = Assembly Location  
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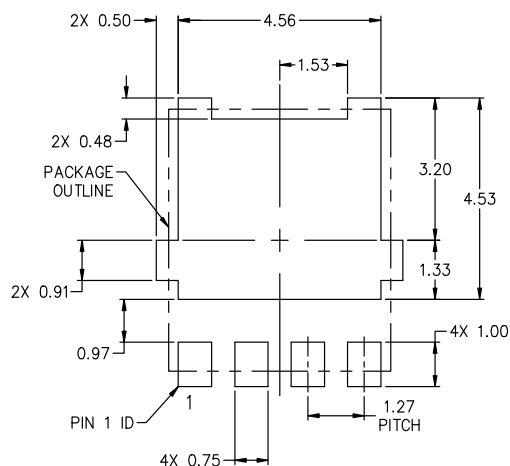
\*This information is generic. Please refer to device data sheet for actual part marking.  
Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-2018.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
4. THIS PACKAGE CONTAINS WETTABLE FLANK DESIGN FEATURES TO AID IN FILLET FORMATION ON THE LEADS DURING MOUNTING.



| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN         | NOM  | MAX  |
| A   | 0.90        | 1.00 | 1.10 |
| A1  | 0.00        | ---  | 0.05 |
| b   | 0.33        | 0.41 | 0.51 |
| c   | 0.23        | 0.28 | 0.33 |
| D   | 5.00        | 5.15 | 5.30 |
| D1  | 4.70        | 4.90 | 5.10 |
| D2  | 3.80        | 4.00 | 4.20 |
| E   | 6.00        | 6.15 | 6.30 |
| E1  | 5.70        | 5.90 | 6.10 |
| E2  | 3.45        | 3.65 | 3.85 |
| E3  | 3.00        | 3.40 | 3.80 |
| e   | 1.27 BSC    |      |      |
| k   | 1.20        | 1.35 | 1.50 |
| L   | 0.51        | 0.57 | 0.71 |
| L2  | 0.15 REF.   |      |      |
| θ   | 0°          | 6°   | 12°  |



RECOMMENDED MOUNTING FOOTPRINT\*  
\*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

|                  |                             |   |
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| DESCRIPTION:     | DFNW5 4.90x5.90x1.00, 1.27P | PAGE 1 OF 1   |

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