

# NUP4016P5T5G, SZNUP4016P5T5G

## Ultra-Low Capacitance Diode-TVS Array for High Speed Data Line Protection

The NUP4016P5 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra-low capacitance and high level of ESD protection makes this device well suited for use in USB 2.0 applications.

### Features

- Ultra-Low Capacitance (0.5 pF Typical Between I/O Lines and Ground)
- ESD Rating of Class 3B (Exceeding 8 kV) per Human Body model and Class C (Exceeding 400 V) per Machine Model
- Protection for the Following IEC Standards:  
IEC 61000-4-2 15 kV (contact)
- UL Flammability Rating of 94 V-0
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This is a Pb-Free Device\*

### Typical Applications

- High Speed Communication Line Protection
- USB 2.0 High Speed Data Line and Power Line Protection
- Monitors and Flat Panel Displays
- MP3
- Gigabit Ethernet

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T <sub>J</sub>	-40 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
Human Body Model (HBM) Machine Model (MM) IEC 61000-4-2 Contact (ESD)	ESD	16000 400 15000	V

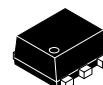
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

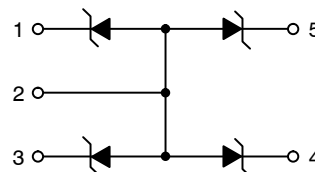


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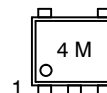
<http://onsemi.com>



SOT-953  
CASE 527AE



MARKING DIAGRAM



4 = Specific Device Code  
M = Date Code

### ORDERING INFORMATION

Device	Package	Shipping†
NUP4016P5T5G	SOT-953 (Pb-Free)	4,000 / Tape & Reel
SZNUP4016P5T5G	SOT-953 (Pb-Free)	4,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	$V_{RWM}$	(Note 1)			5.0	V
Breakdown Voltage	$V_{BR}$	$I_T = 1\text{ mA}$ , (Note 2)	5.5			V
Reverse Leakage Current	$I_R$	$V_{RWM} = 5\text{ V}$			1.0	$\mu\text{A}$
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ between I/O Pins and GND		0.5	0.8	pF
Junction Capacitance	$C_J$	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ between I/O Pins		0.3	0.5	pF

1. TVS devices are normally selected according to the working peak reverse voltage ( $V_{RWM}$ ), which should be equal or greater than the DC or continuous peak operating voltage level.
2.  $V_{BR}$  is measured at pulse test current  $I_T$ .
3. Include SZ-prefix devices where applicable.

## TYPICAL PERFORMANCE CURVES

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

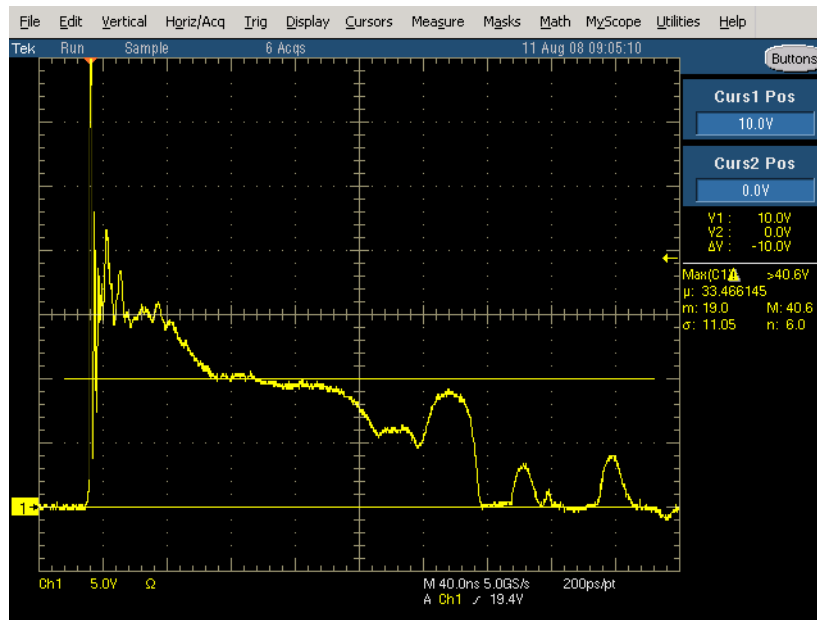
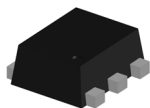


Figure 1. ESD Clamping Voltage Screenshot  
(8 kV Contact per IEC61000-4-2)

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

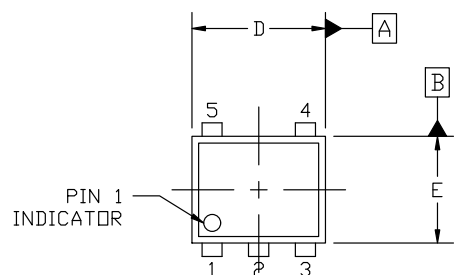


**SOT-953 1.00x0.80x0.37, 0.35P**  
CASE 527AE  
ISSUE F

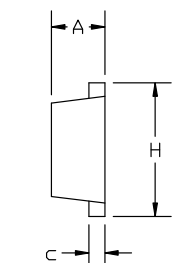
DATE 17 JAN 2024

## NOTES:

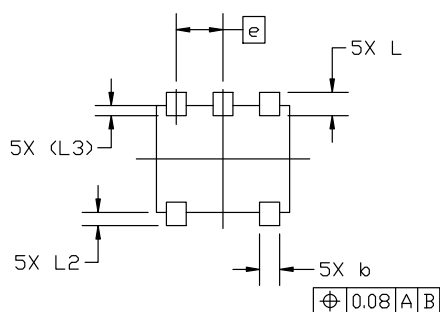
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



TOP VIEW

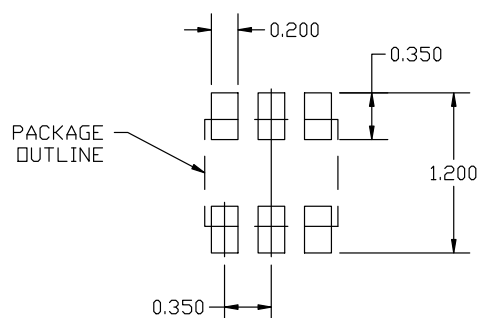


SIDE VIEW



BOTTOM VIEW

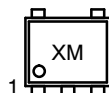
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H	0.95	1.00	1.05
L	0.125	0.175	0.225
L2	0.05	0.10	0.15
L3	0.075 (REF)		



RECOMMENDED MOUNTING  
FOOTPRINT

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM\*



X = Specific Device Code  
M = Month Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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