NTMS5838NL

Power MOSFET
40 V, 7.5 A, 20 mΩ

Features

- Low $R_{DS(on)}$
- Low Capacitance
- Optimized Gate Charge
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	40	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	5.8	A
		T_A = 70°C		4.6	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	1.5	W
		T_A = 70°C		1.0	
Continuous Drain Current $R_{\theta JA}$ (Note 1)	t ≤10 s	T_A = 25°C	I_D	7.5	A
		T_A = 70°C		6.0	
Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	P_D	2.6	W
		T_A = 70°C		1.6	
Pulsed Drain Current	t_p = 10 μs		I_{DM}	30	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to +150	°C
Source Current (Body Diode)			I_S	7.5	A
Single Pulse Drain−to−Source Avalanche Energy (V_{DD} = 40 V, V_{GS} = 10 V, L = 0.1 mH)			EAS	20	mJ
			IAS	20	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

THERMAL RESISTANCE MAXIMUM RATINGS

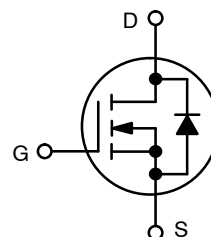| Parameter	Symbol	Value	Unit
Junction−to−Ambient Steady State (Note 1)	$R_{\theta JA}$	83	
Junction−to−Ambient − t ≤10 s (Note 1)	$R_{\theta JA}$	49	°C/W
Junction−to−Foot (Drain) (Note 1)	$R_{\theta JF}$	22	
Junction−to−Ambient Steady State (Note 2)	$R_{\theta JA}$	123	

1. Surface−mounted on FR4 board using 1 sq−in pad
   (Cu area = 1.127 in sq [2 oz] including traces).
2. Surface−mounted on FR4 board using 0.155 in sq (100mm²) pad size.

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
40 V	20 mΩ @ 10 V	7.5 A
	36.5 mΩ @ 4.5 V	

N−CHANNEL MOSFET

MARKING DIAGRAM/ PIN ASSIGNMENT

SO−8
CASE 751
STYLE 12

```
1        8
Source ⊏⊐ Drain
Source ⊏⊐ Drain
Source ⊏⊐ Drain
Gate   ⊏⊐ Drain
    Top View
```
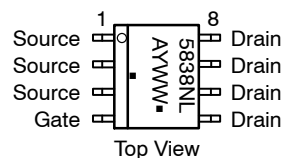
5838NL
AYWW▪

A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package*

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTMS5838NLR2G	SO−8 (Pb−Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMS5838NL

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA		40			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				32		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 40 V	T_J = 25°C			1	µA
			T_J = 125°C			100	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 µA		1.0	1.8	3.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				6.0		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 7 A			16.2	20	mΩ
		V_{GS} = 4.5 V, I_D = 7 A			25.0	36.5	
Forward Transconductance	g_{FS}	V_{DS} = 15 V, I_D = 7 A			4.0		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1 MHz, V_{DS} = 20 V			785		pF
Output Capacitance	C_{OSS}				123		
Reverse Transfer Capacitance	C_{RSS}				90		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 20 V; I_D = 7 A			17		nC
		V_{GS} = 4.5 V, V_{DS} = 20 V; I_D = 7 A			8.6	11	
Threshold Gate Charge	$Q_{G(TH)}$				0.8		
Gate−to−Source Charge	Q_{GS}				2.8		
Gate−to−Drain Charge	Q_{GD}				4.0		
Plateau Voltage	V_{GP}				3.2		V
Gate Resistance	R_G				1.8		Ω
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 20 V, I_D = 7 A, R_G = 2.5 Ω			11		ns
Rise Time	t_r				23		
Turn−Off Delay Time	$t_{d(OFF)}$				17		
Fall Time	t_f				4.0		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 7 A	T_J = 25°C		0.84	1.2	V
			T_J = 125°C		0.7		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dIS/dt = 100 A/µs, I_S = 7 A			17		ns
Charge Time	t_a				11		
Discharge Time	t_b				6.0		
Reverse Recovery Charge	Q_{RR}				10		nC

3. Pulse Test: pulse width ≤ 300 µs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.
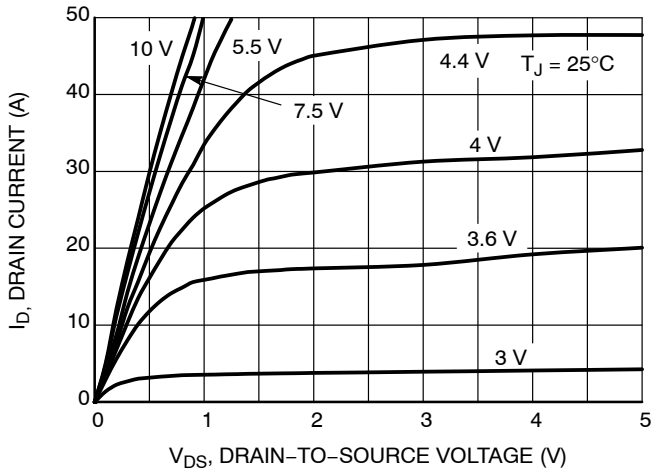
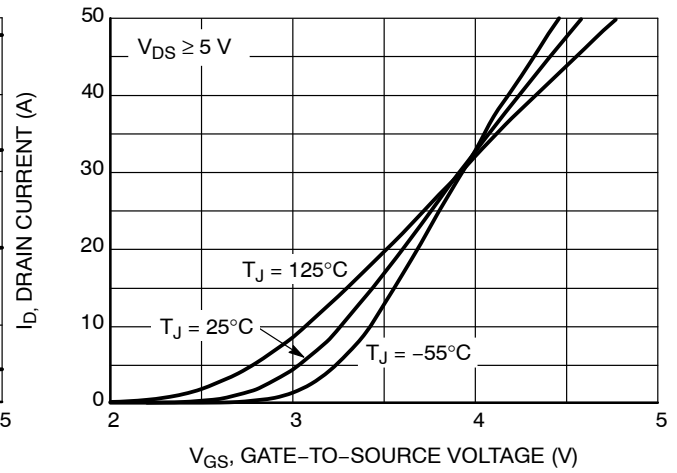## TYPICAL PERFORMANCE CURVES

Figure 1. On−Region Characteristics
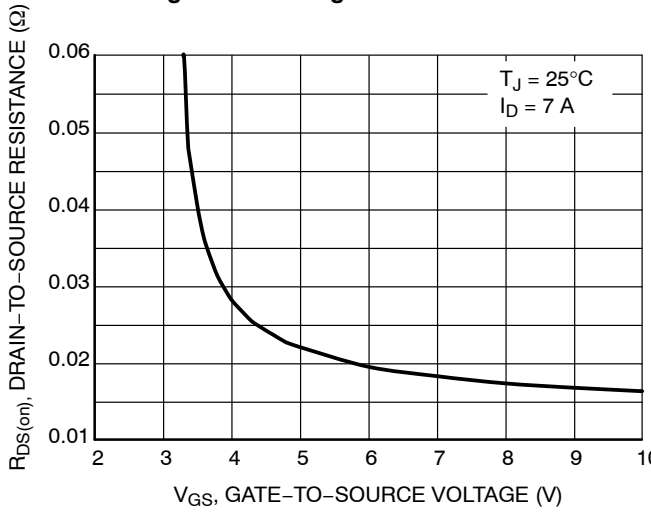
Figure 2. Transfer Characteristics

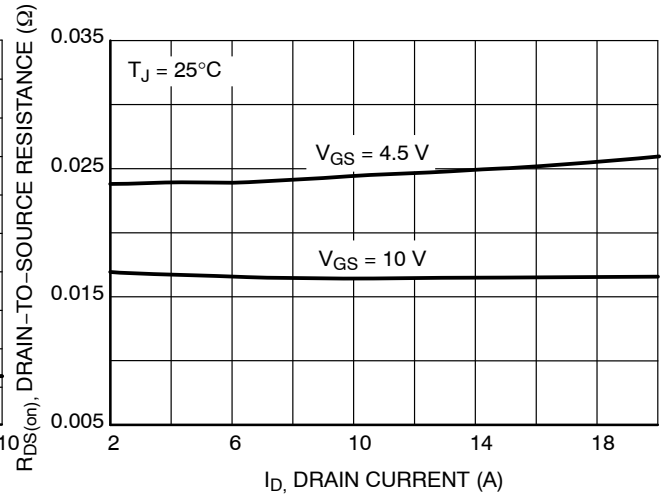**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

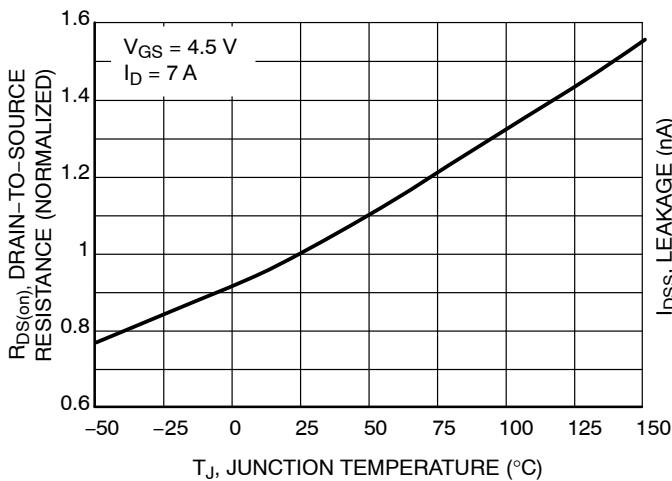**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

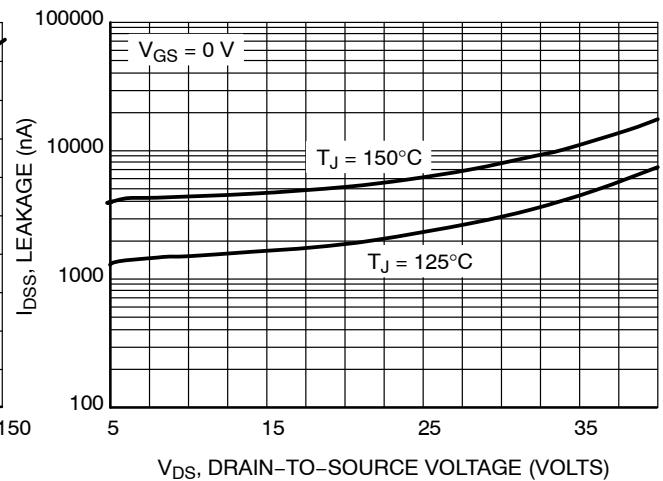**Figure 5. On−Resistance Variation with Temperature**

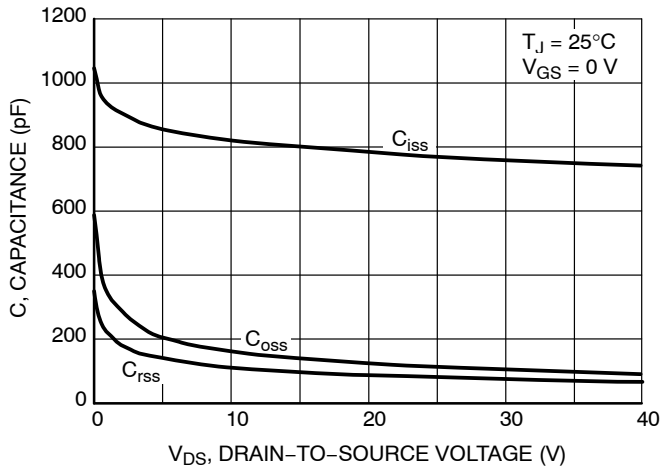**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

NTMS5838NL

TYPICAL PERFORMANCE CURVES

Figure 7. Capacitance Variation
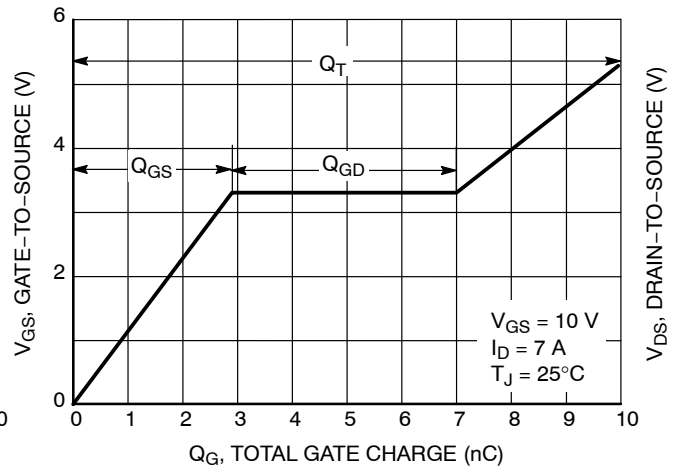
Figure 8. Gate–To–Source and Drain–To–Source Voltage vs. Total Charge
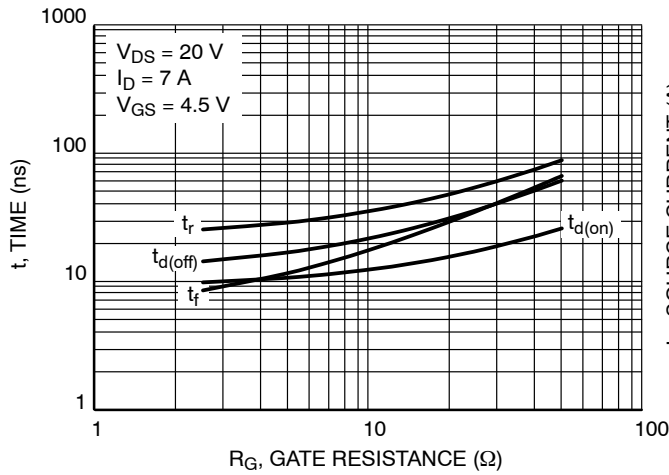
Figure 9. Resistive Switching Time Variation vs. Gate Resistance
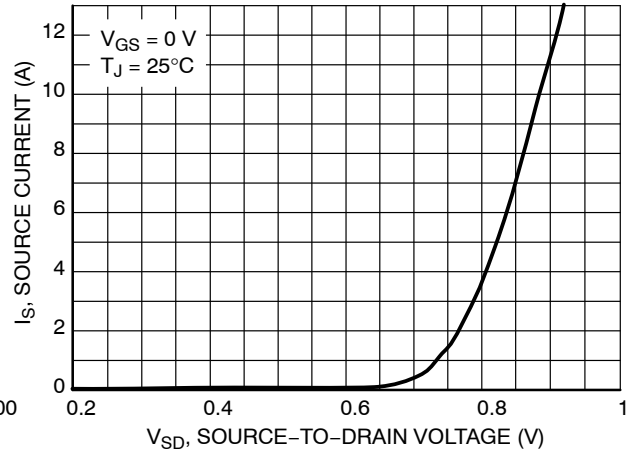
Figure 10. Diode Forward Voltage vs. Current
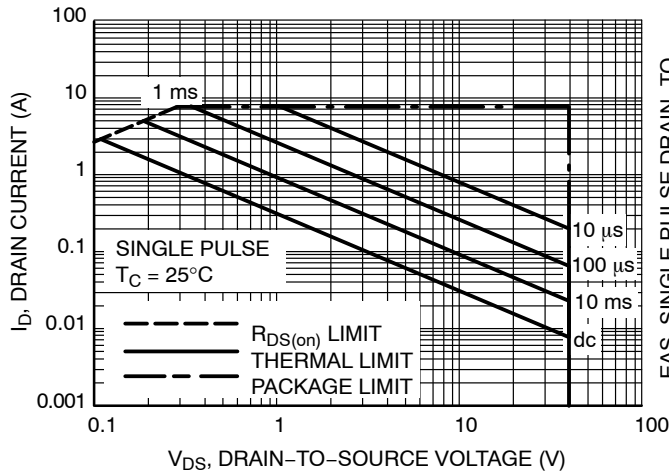
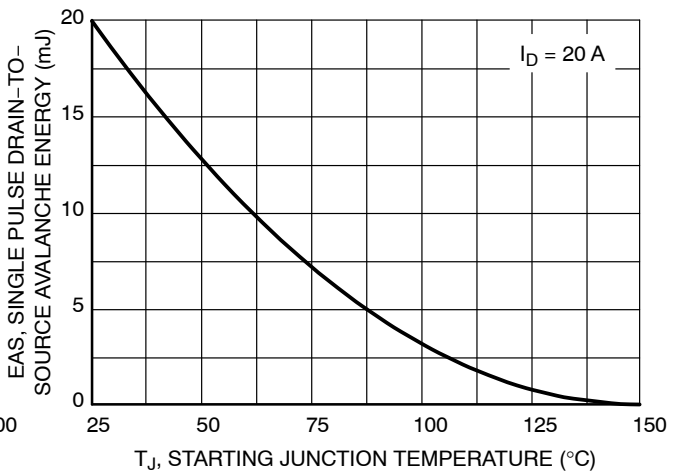**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature
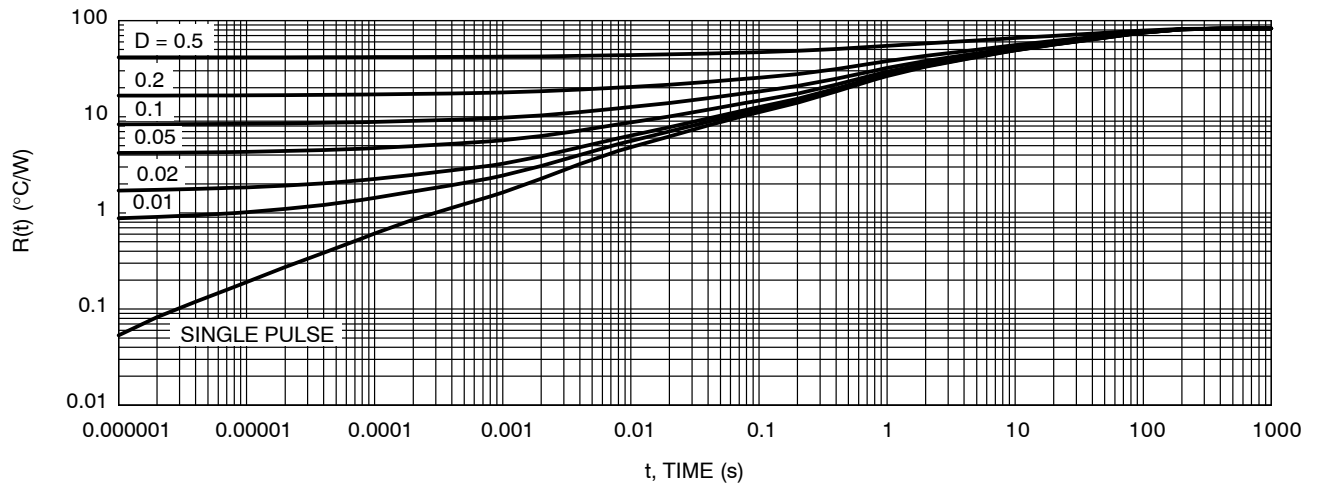
TYPICAL PERFORMANCE CURVES

Figure 13. Thermal Response

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

8

1

SCALE 1:1

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

−X−

A

8   5

B   S | $\oplus$ | 0.25 (0.010) Ⓜ | Y | Ⓜ |

1   4

−Y−

G

| | 0.25 (0.010) Ⓜ | Z | Y Ⓢ | X Ⓢ |

C

SEATING PLANE

−Z−

| $\triangle$ | 0.10 (0.004) |

H   D

N X 45°

K

M   J

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

GENERIC MARKING DIAGRAM*

SOLDERING FOOTPRINT*

1.52 / 0.060

7.0 / 0.275

4.0 / 0.155

0.6 / 0.024

1.270 / 0.050

SCALE 6:1 $\left(\dfrac{mm}{inches}\right)$

8
XXXXX
ALYWX
1

IC

8
XXXXX
ALYWX ■
1

IC (Pb−Free)

8
XXXXXX
AYWW
1

Discrete

8
XXXXXX
AYWW ■
1

Discrete (Pb−Free)

XXXXX = Specific Device Code
A   = Assembly Location
L   = Wafer Lot
Y   = Year
W   = Work Week
■   = Pb−Free Package

XXXXXX = Specific Device Code
A   = Assembly Location
Y   = Year
WW   = Work Week
■   = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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DESCRIPTION:	SOIC−8 NB		**PAGE 1 OF 2**

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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