# NTMS4N01R2

# Power MOSFET
# 4.2 Amps, 20 Volts
## N−Channel Enhancement−Mode
## Single SO−8 Package

**Features**

- High Density Power MOSFET with Ultra Low $R_{DS(on)}$ Providing Higher Efficiency
- Miniature SO−8 Surface Mount Package Saving Board Space; Mounting Information for the SO−8 Package is Provided
- $I_{DSS}$ Specified at Elevated Temperature
- Drain−to−Source Avalanche Energy Specified
- Diode Exhibits High Speed, Soft Recovery
- Pb−Free Package is Available

**Applications**

- Power Management in Portable and Battery−Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain−to−Source Voltage | $V_{DSS}$ | 20 | V |
| Drain−to−Gate Voltage ($R_{GS}$ = 1.0 mΩ) | $V_{DGR}$ | 20 | V |
| Gate−to−Source Voltage − Continuous | $V_{GS}$ | ±10 | V |
| Thermal Resistance, Junction−to−Ambient (Note 1)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Pulsed Drain Current (Note 4) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 50<br>2.5<br>5.9<br>4.7<br>25 | °C/W<br>W<br>A<br>A<br>A |
| Thermal Resistance, Junction−to−Ambient (Note 2)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Pulsed Drain Current (Note 4) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 100<br>1.25<br>4.2<br>3.3<br>20 | °C/W<br>W<br>A<br>A<br>A |
| Thermal Resistance, Junction−to−Ambient (Note 3)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Pulsed Drain Current (Note 4) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 162<br>0.77<br>3.3<br>2.6<br>15 | °C/W<br>W<br>A<br>A<br>A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |
| Single Pulse Drain−to−Source Avalanche Energy − Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 7.5 Apk, L = 6 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 169 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Mounted onto a 2″ square FR−4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
2. Mounted onto a 2″ square FR−4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t = steady state.
3. Minimum FR−4 or G−10 PCB, t = Steady State.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

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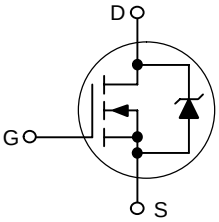
**4.2 AMPERES, 20 VOLTS**
**0.045 Ω @ $V_{GS}$ = 4.5 V**

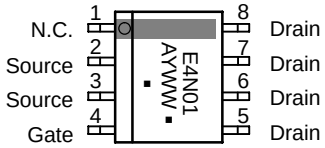
**Single N−Channel**





**SO−8**
**CASE 751**
**STYLE 13**

**MARKING DIAGRAM AND PIN ASSIGNMENT**




Top View

E4N01 = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTMS4N01R2 | SO−8 | 2500 / Tape & Reel |
| NTMS4N01R2G | SO−8 (Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 5)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 20 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | | – | 0.2 | – | |
| Gate−Body Leakage Current ($V_{GS}$ = +10 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| Gate−Body Leakage Current ($V_{GS}$ = −10 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | −100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 0.6 | 0.95 | 1.2 | Vdc |
| Temperature Coefficient (Negative) | | | – | −3.0 | – | mV/°C |
| Static Drain−to−Source On−State Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 4.2 Adc) | | $R_{DS(on)}$ | – | 0.030 | 0.04 | Ω |
| ($V_{GS}$ = 2.7 Vdc, $I_D$ = 2.1 Adc) | | | – | 0.035 | 0.05 | |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 2.0 Adc) | | | – | 0.037 | – | |
| Forward Transconductance ($V_{DS}$ = 2.5 Vdc, $I_D$ = 2.0 Adc) | | $g_{FS}$ | – | 10 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 870 | 1200 | pF |
| Output Capacitance | | $C_{oss}$ | – | 260 | 400 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 60 | 100 | |
| **SWITCHING CHARACTERISTICS** (Notes 6 & 7) | | | | | | |
| Turn−On Delay Time | ($V_{DD}$ = 12 Vdc, $I_D$ = 4.2 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 2.3 Ω) | $t_{d(on)}$ | – | 13 | 25 | ns |
| Rise Time | | $t_r$ | – | 35 | 65 | |
| Turn−Off Delay Time | | $t_{d(off)}$ | – | 45 | 75 | |
| Fall Time | | $t_f$ | – | 50 | 90 | |
| Total Gate Charge | ($V_{DS}$ = 12 Vdc, $V_{GS}$ = 4.5 Vdc, $I_D$ = 4.2 Adc) | $Q_{tot}$ | – | 11 | 16 | nC |
| Gate−Source Charge | | $Q_{gs}$ | – | 2.0 | – | |
| Gate−Drain Charge | | $Q_{gd}$ | – | 3.0 | – | |
| **BODY−DRAIN DIODE RATINGS** (Note 6) | | | | | | |
| Diode Forward On−Voltage | ($I_S$ = 4.2 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.85 | 1.1 | Vdc |
| | ($I_S$ = 4.2 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.70 | – | |
| Reverse Recovery Time | ($I_S$ = 4.2 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 20 | – | ns |
| | | $t_a$ | – | 12 | – | |
| | | $t_b$ | – | 8.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.01 | – | μC |

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

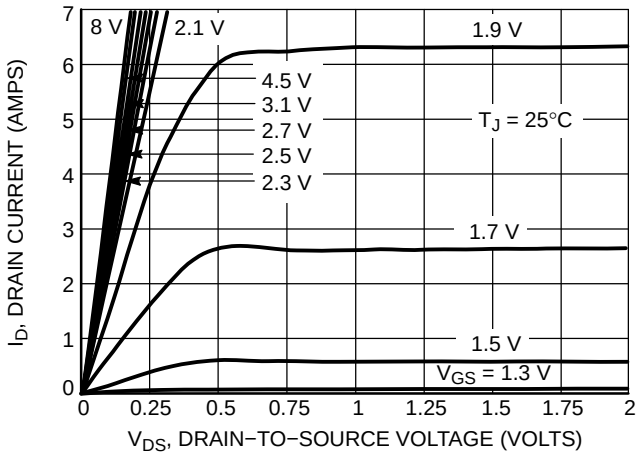



**Figure 1. On−Region Characteristics**

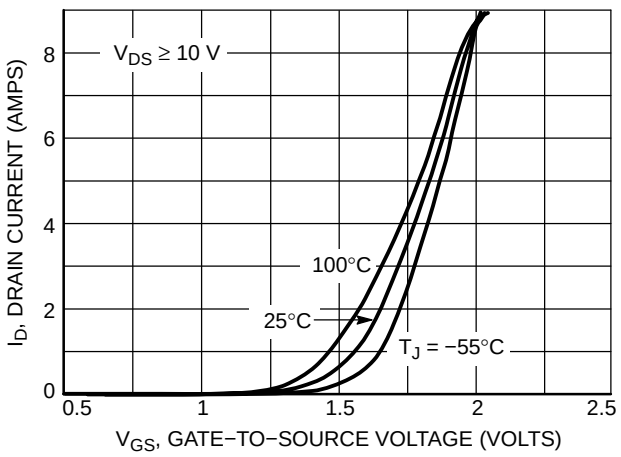



**Figure 2. Transfer Characteristics**

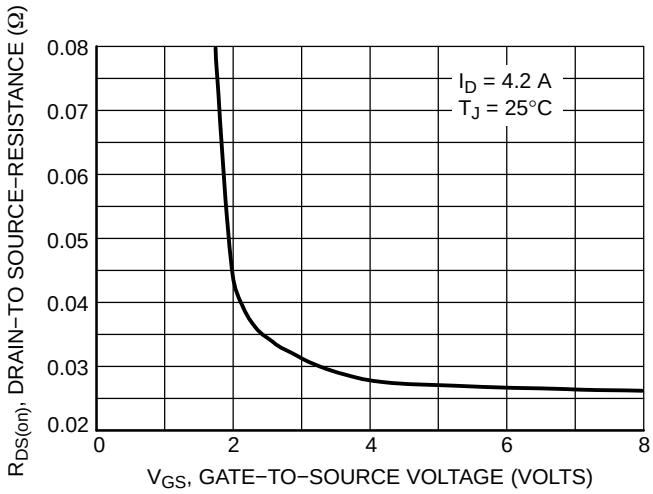



**Figure 3. On−Resistance versus Gate−To−Source Voltage**

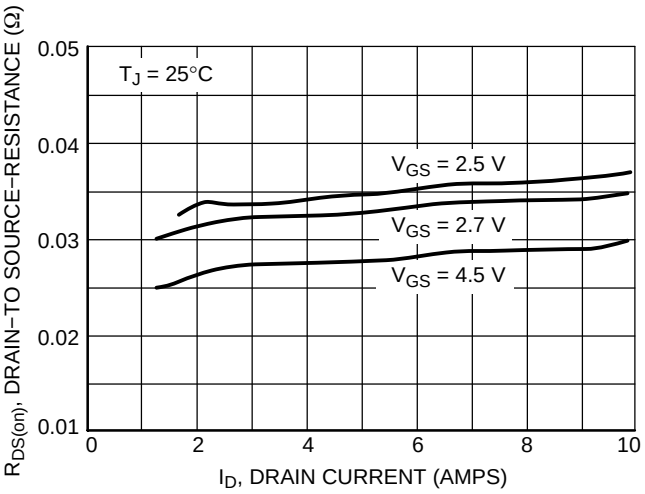



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

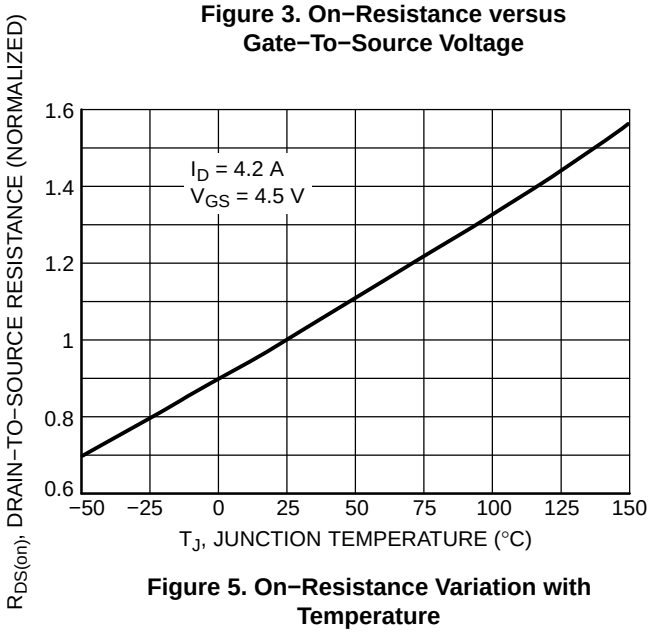



**Figure 5. On−Resistance Variation with Temperature**

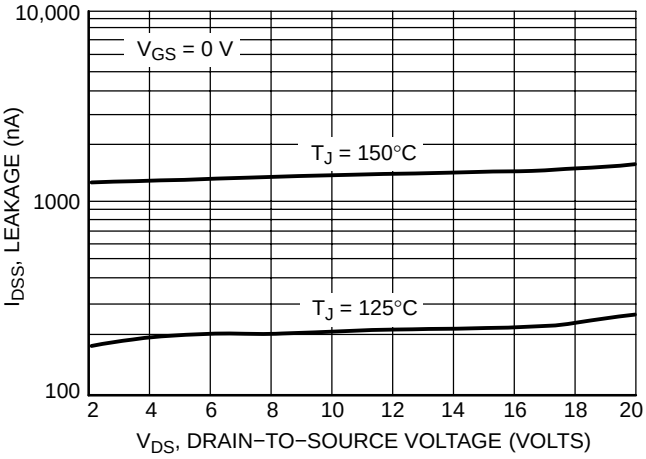



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

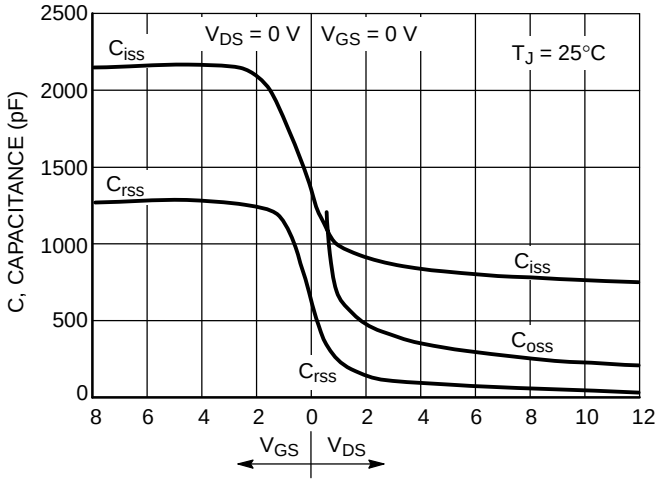



**Figure 7. Capacitance Variation**

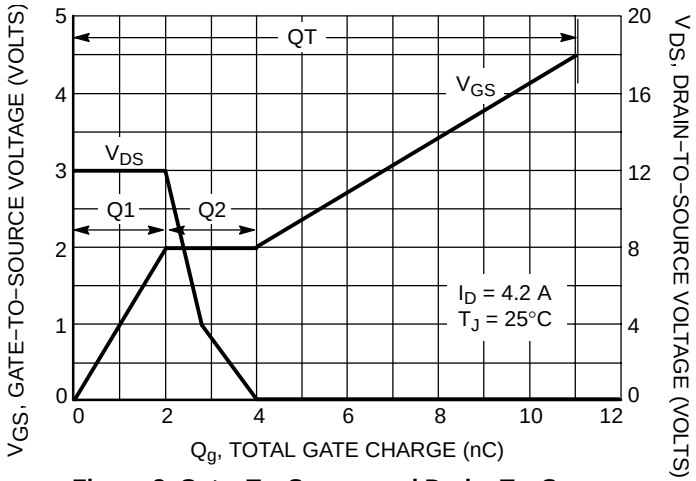



**Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge**

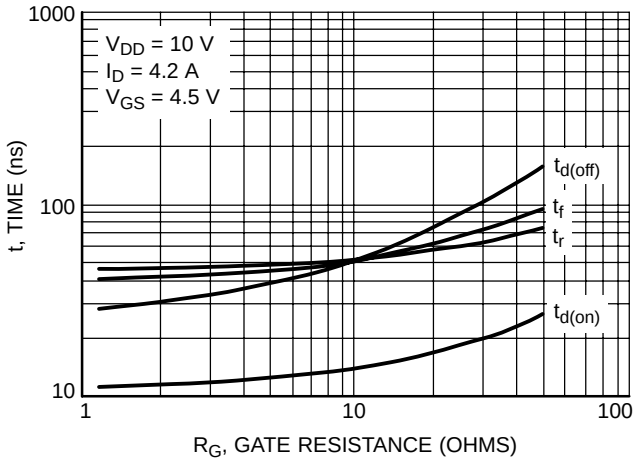



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

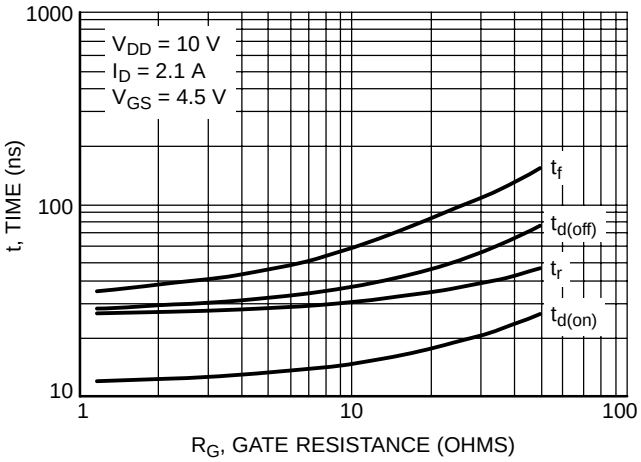



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN−TO−SOURCE DIODE CHARACTERISTICS

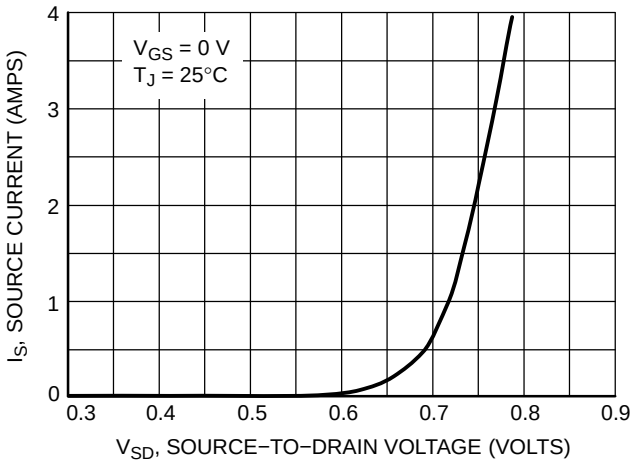



**Figure 11. Diode Forward Voltage versus Current**

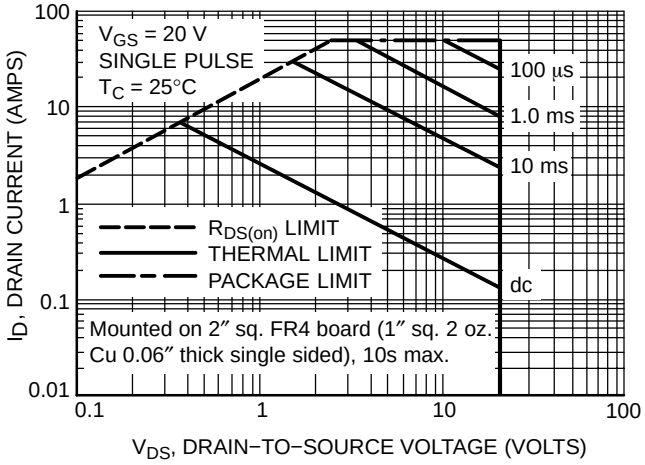



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

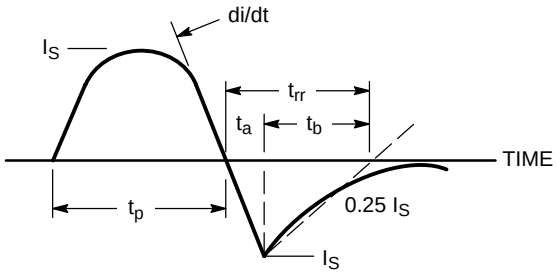



**Figure 13. Diode Reverse Recovery Waveform**

## TYPICAL ELECTRICAL CHARACTERISTICS

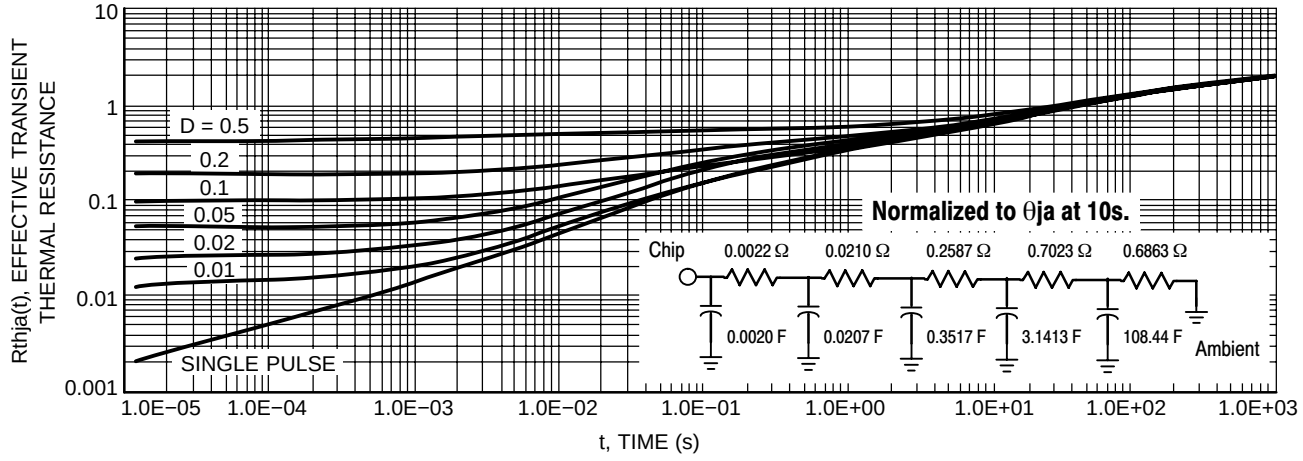
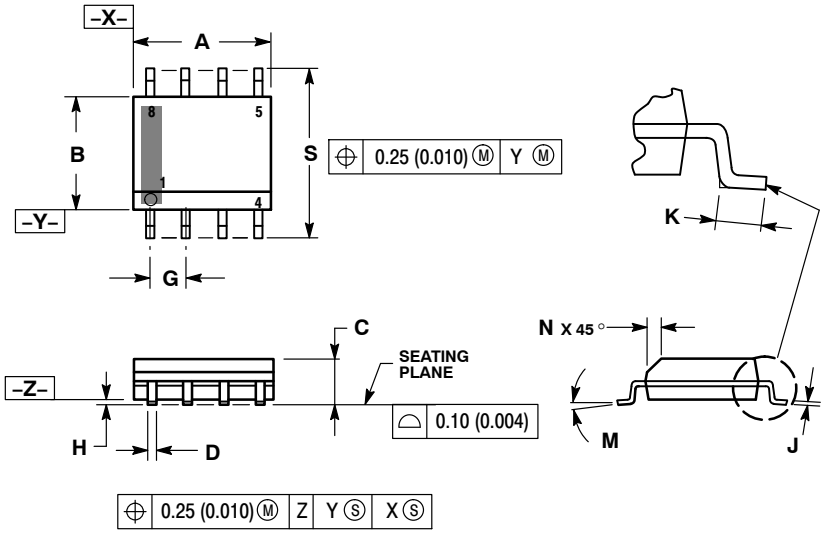



**Figure 14. Thermal Response**

**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

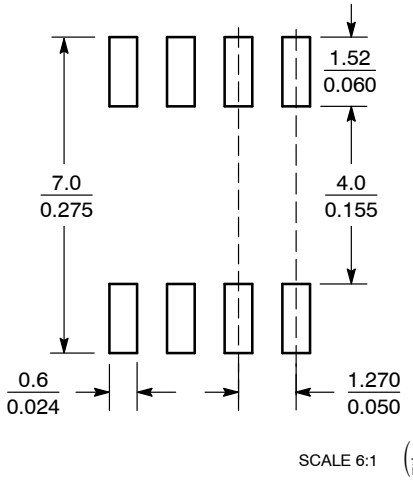
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

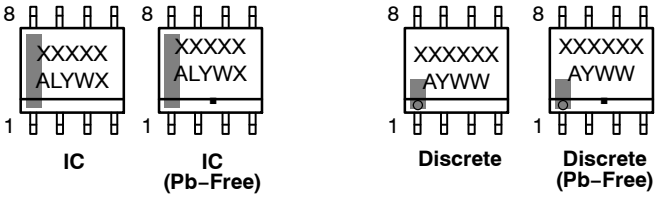
## SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*




XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | | |
|---|---|---|---|
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CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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