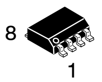
DATA SHEET
www.onsemi.com

MOSFET – Power, P-Channel, SOIC-8

-30 V, -11.4 A

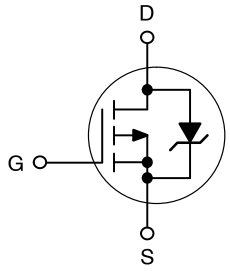
NTMS4177P

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
−30 V	12 mΩ @ −10 V	−11.4 A
	19 mΩ @ −4.5 V	



SOIC−8
CASE 751
STYLE 12

P−Channel



Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- SOIC−8 Surface Mount Package Saves Board Space
- This is a Pb−Free Device

Applications

- Load Switches
- Notebook PC’s
- Desktop PC’s

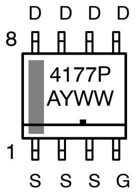
MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Symbol	Rating			Value	Unit
V_{DSS}	Drain−to−Source Voltage			−30	V
V_{GS}	Gate−to−Source Voltage			±20	V
I_D	Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	−8.9	A
			T_A = 70°C	−7.1	
P_D	Power Dissipation $R_{\theta JA}$ (Note 1)		T_A = 25°C	1.52	W
I_D	Continuous Drain Current $R_{\theta JA}$ (Note 2)		T_A = 25°C	−6.6	A
			T_A = 70°C	−5.3	
P_D	Power Dissipation $R_{\theta JA}$ (Note 2)		T_A = 25°C	0.84	W
I_D	Continuous Drain Current $R_{\theta JA}$ t < 10 s (Note 1)		T_A = 25°C	−11.4	A
			T_A = 70°C	−9.3	
P_D	Power Dissipation $R_{\theta JA}$ t < 10 s (Note 1)		T_A = 25°C	2.5	W
I_{DM}	Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		−46	A
T_J, T_{STG}	Operating Junction and Storage Temperature			−55 to +150	°C
I_S	Source Current (Body Diode)			−2.1	A
EAS	Single Pulse Drain−to−Source Avalanche Energy T_J = 25°C, V_{DD} = 30 V, V_{GS} = 10 V, I_L = 20 A_{pk}, L = 1.0 mH, R_G = 25 Ω			200	mJ
T_L	Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Surface−mounted on FR4 board using 1 inch sq pad size, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

MARKING DIAGRAM & PIN ASSIGNMENT



4177P = Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTMS4177PR2G	SOIC−8 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2008

THERMAL RESISTANCE RATINGS

Symbol	Rating	Max	Unit
$R_{\theta JA}$	Junction−to−Ambient – Steady State (Note 3)	82	°C/W
$R_{\theta JA}$	Junction−to−Ambient – t≤10 s (Note 3)	50	
$R_{\theta JF}$	Junction−to−FOOT (Drain)	20	
$R_{\theta JA}$	Junction−to−Ambient – Steady State (Note 4)	148	

3. Surface−mounted on FR4 board using 1 inch sq pad size, 1 oz Cu.
4. Surface−mounted on FR4 board using the minimum recommended pad size.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)jk

Symbol	Characteristic	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
$V_{(BR)DSS}$	Drain−to−Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA		−30			V
$V_{(BR)DSS}/T_J$	Drain−to−Source Breakdown Voltage Temperature Coefficient				29		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{GS} = 0 V, V_{DS} = −24 V	T_J = 25°C			−1.0	μA
			T_J = 85°C			−5.0	
I_{GSS}	Gate−to−Source Leakage Current	V_{DS} = 0 V, V_{GS} = ±20 V				±100	nA
ON CHARACTERISTICS (Note 5)							
$V_{GS(TH)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA		−1.5		−2.5	V
$V_{GS(TH)}/T_J$	Negative Threshold Temperature Coefficient				6.0		mV/°C
$R_{DS(on)}$	Drain−to−Source On Resistance	V_{GS} = −10 V	I_D = −11.4 A		10	12	mΩ
		V_{GS} = −4.5 V	I_D = −9.1 A		15	19	
g_{FS}	Forward Transconductance	V_{DS} = −1.5 V	I_D = −11.4 A		30		S
CHARGES, CAPACITANCES AND GATE RESISTANCE							
C_{ISS}	Input Capacitance	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −24 V			3100		pF
C_{OSS}	Output Capacitance				550		
C_{RSS}	Reverse Transfer Capacitance				370		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −11.4 A			29		nC
$Q_{G(TH)}$	Threshold Gate Charge				3.3		
Q_{GS}	Gate−to−Source Charge				10		
Q_{GD}	Gate−to−Drain Charge				13		
$Q_{G(TOT)}$	Total Gate Charge	V_{GS} = −10 V, V_{DS} = −15 V, I_D = −11.4 A,			55		nC
R_G	Gate Resistance				2.0	4.0	Ω
SWITCHING CHARACTERISTICS (Note 6)							
$t_{d(ON)}$	Turn−On Delay Time	V_{GS} = −10 V, V_{DD} = −15 V, I_D = −1.0 A, R_G = 6.0 Ω			18		ns
t_r	Rise Time				13		
$t_{d(OFF)}$	Turn−Off Delay Time				64		
t_f	Fall Time				36		
DRAIN−TO−SOURCE CHARACTERISTICS							
V_{SD}	Forward Diode Voltage	V_{GS} = 0 V I_D = −2.1 A	T_J = 25°C		−0.73	−1.0	V
			T_J = 125°C		0.54		
t_{RR}	Reverse Recovery Time	V_{GS} = 0 V, d_{IS}/d_t = 100 A/μs, I_S = −2.1 A			34		ns
T_a	Charge Time				18		
T_b	Discharge Time				16		
Q_{RR}	Reverse Recovery Time				30		nC

5. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES

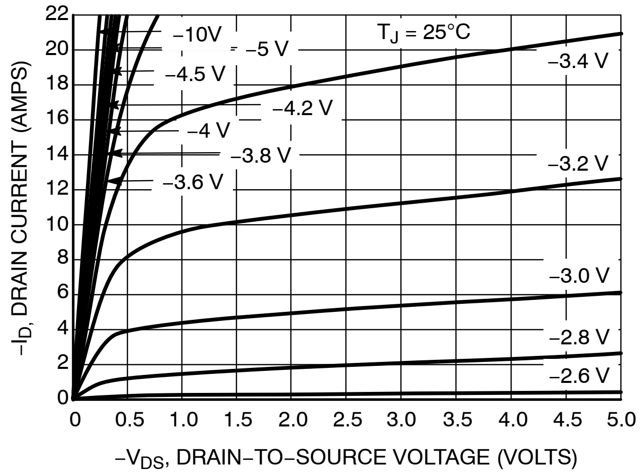


Figure 1. On−Region Characteristics

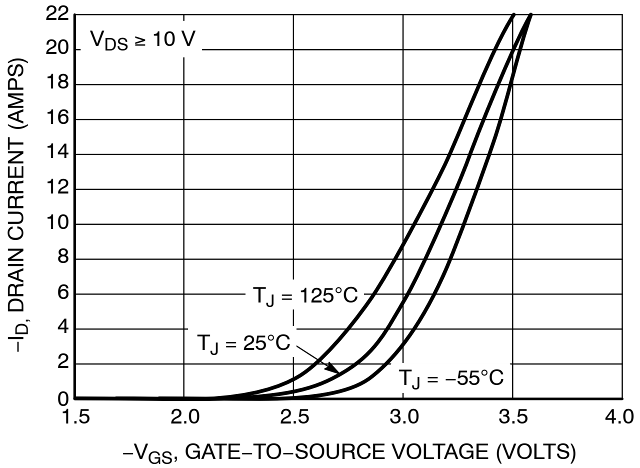


Figure 2. Transfer Characteristics

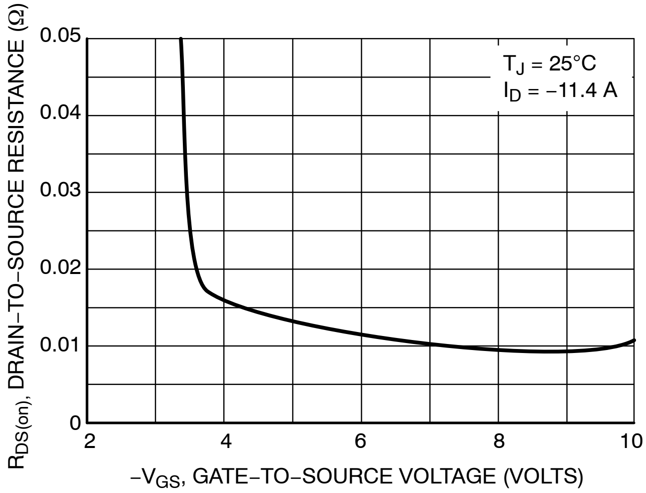


Figure 3. On−Resistance vs. Gate−to−Source Voltage

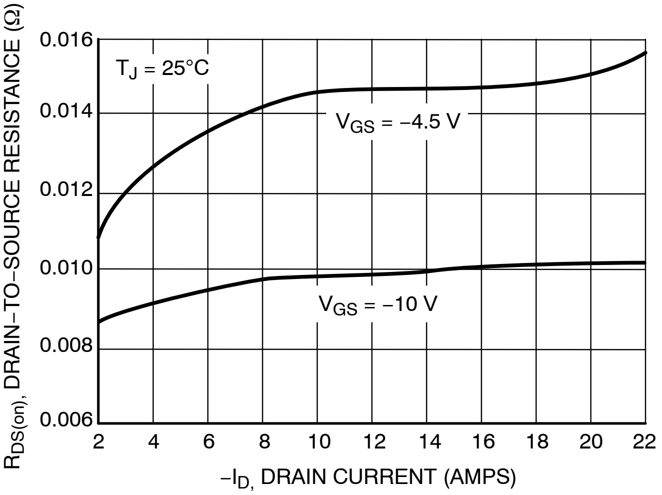


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

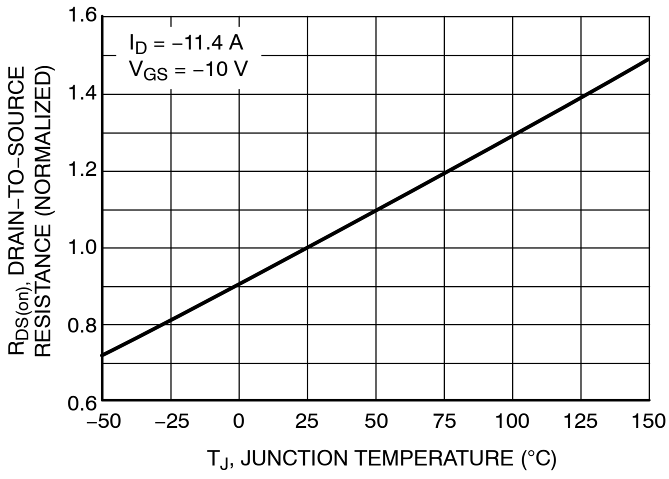


Figure 5. On−Resistance Variation with Temperature

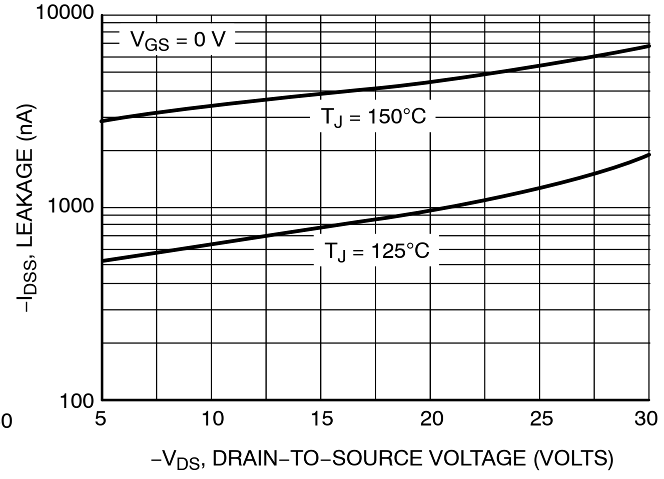


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (continued)

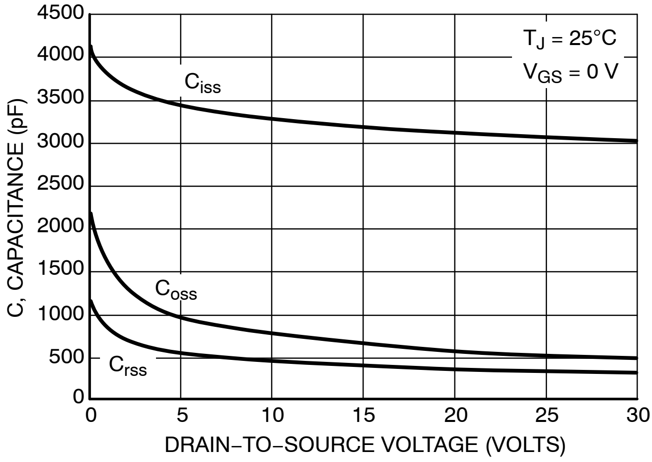


Figure 7. Capacitance Variation

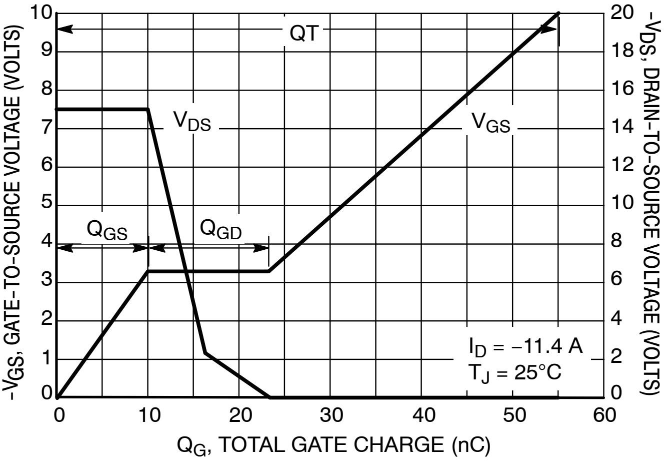


Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge

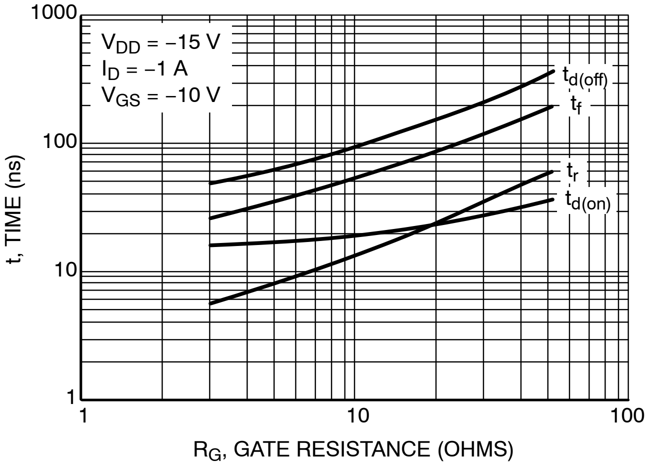


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

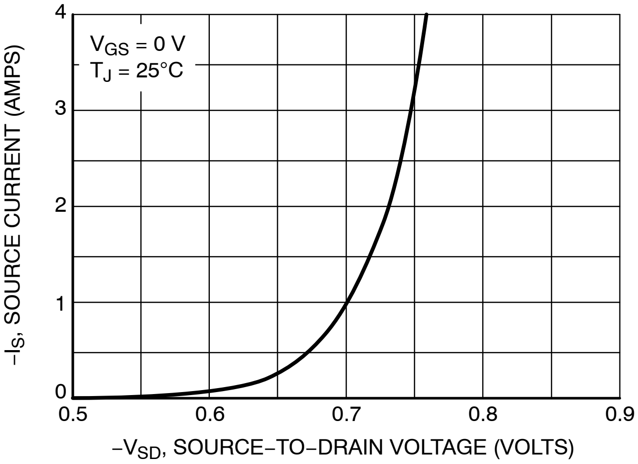


Figure 10. Diode Forward Voltage vs. Current

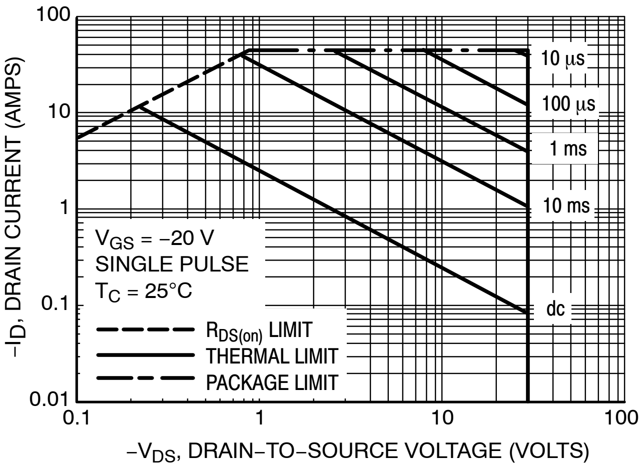


Figure 11. Maximum Rated Forward Biased Safe Operating Area

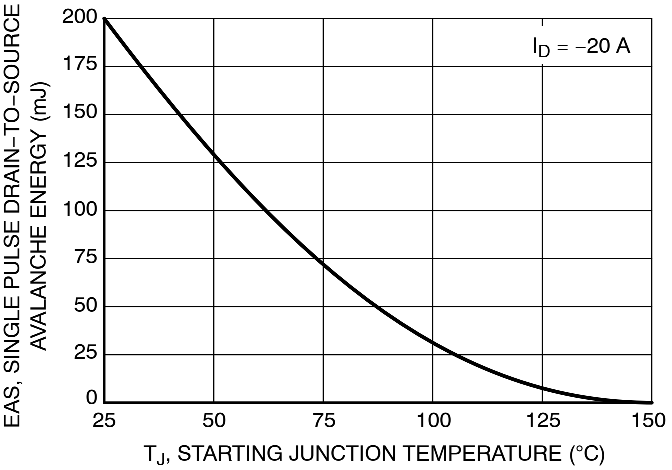
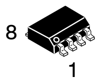


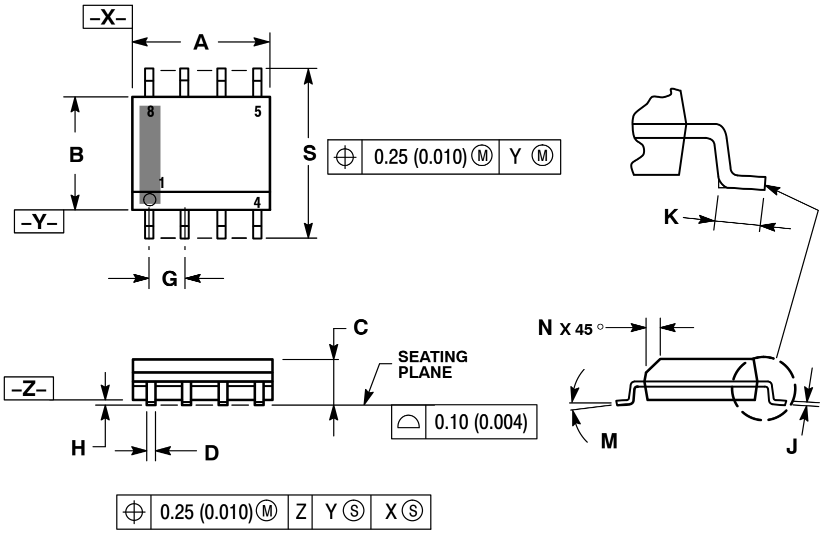
Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

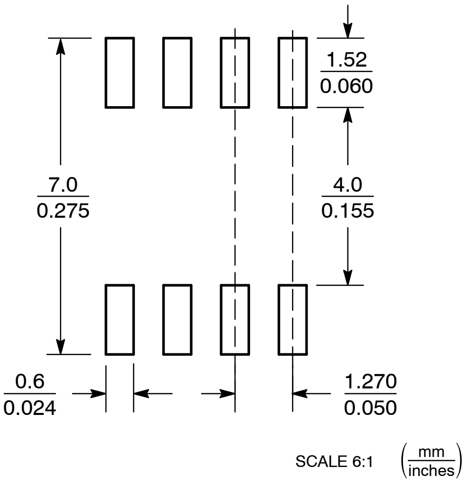
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

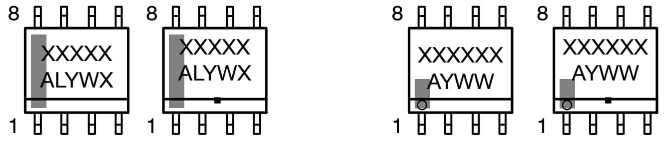
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC **IC (Pb−Free)** **Discrete** **Discrete (Pb−Free)**

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

onsemi and onsemi. are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales