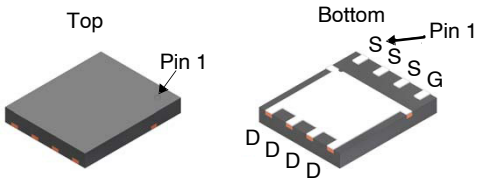
MOSFET – N-Channel, Shielded Gate, POWERTRENCH®

80 V, 147 A, 3.1 mΩ

NTMFS08N003C



PQFN8 5X6, 1.27P
Power 56
CASE 483AF

General Description

This N-Channel MV MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

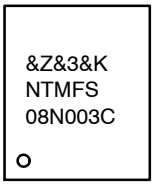
Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 3.1 mΩ at V_{GS} = 10 V, I_D = 56 A
- Max $R_{DS(on)}$ = 8.1 mΩ at V_{GS} = 6 V, I_D = 28 A
- 50% Lower Qrr Than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- This Device is Pb-Free, Halide Free and is RoHS Compliant

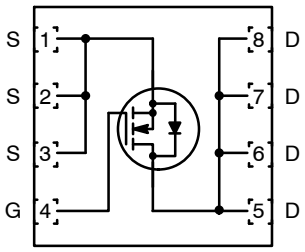
Applications

- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= 3-Digits Date Code
&K	= 2-Digits Lot Traceability Code
NTMFS08N003C	= Specific Device Code



N−CHANNEL MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25 °C unless otherwise noted)

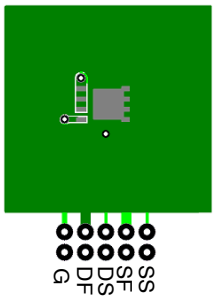
Symbol	Parameter				Ratings	Unit
V_{DS}	Drain to Source Voltage				80	V
V_{GS}	Gate to Source Voltage				±20	V
I_D	Drain Current	−Continuous	T_C = 25 °C	(Note 4)	147	A
		−Continuous	T_C = 100 °C	(Note 4)	92	
		−Continuous	T_A = 25 °C	(Note 1a)	22	
		−Pulsed		(Note 3)	658	
E_{AS}	Single Pulse Avalanche Energy			(Note 2)	486	mJ
P_D	Power Dissipation		T_C = 25 °C		125	W
	Power Dissipation		T_A = 25 °C	(Note 1a)	2.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range				−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

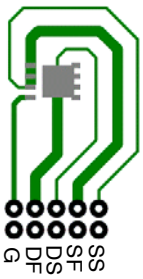
THERMAL CHARACTERISTICS

Symbol	Parameter		Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case		1	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	45	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 45 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b) 115 °C/W when mounted on a minimum pad of 2 oz copper.

2. E_{AS} of 486 mJ is based on starting T_J = 25 °C; N-ch: L = 3 mH, I_{AS} = 18 A, V_{DD} = 80 V, V_{GS} = 10 V, 100% test at L = 0.1 mH, I_{AS} = 57 A.
3. Pulsed Id please refer to Figure 11 SOA graph for more details.
4. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

ELECTRICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25 °C	–	60	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 310 μA	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 310 μA, referenced to 25 °C	–	–8.2	–	mV/°C
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 56 A	–	2.6	3.1	mΩ
		V_{GS} = 6 V, I_D = 28 A	–	3.8	8.1	
		V_{GS} = 10 V, I_D = 56 A, T_J = 125 °C	–	4.3	5.2	
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 56 A	–	123	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1 MHz	–	3820	5350	pF
C_{oss}	Output Capacitance		–	1335	1870	pF
C_{rss}	Reverse Transfer Capacitance		–	44	80	pF
R_g	Gate Resistance		0.1	0.6	1.3	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-on Delay Time	V_{DD} = 40 V, I_D = 56 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	20	36	ns
t_r	Rise Time		–	8	16	ns
$t_{d(off)}$	Turn-off Delay Time		–	40	64	ns
t_f	Fall Time		–	12	23	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to 10 V, V_{DD} = 40 V, I_D = 56 A	–	52	73	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to 6 V, V_{DD} = 40 V, I_D = 56 A	–	33	46	nC
Q_{gs}	Gate to Source Charge	V_{DD} = 40 V, I_D = 56 A	–	17	–	nC
Q_{gd}	Gate to Drain ”Miller” Charge	V_{DD} = 40 V, I_D = 56 A	–	10	–	nC
Q_{oss}	Output Charge	V_{DD} = 40 V, V_{GS} = 0 V	–	77	–	nC
Q_{sync}	Total Gate Charge Sync	V_{DS} = 0 V, I_D = 56 A	–	44	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.2 A (Note 5)	–	0.7	1.2	V
		V_{GS} = 0 V, I_S = 56 A (Note 5)	–	0.8	1.3	
t_{rr}	Reverse Recovery Time	I_F = 28 A, di/dt = 300 A/μs	–	28	45	ns
Q_{rr}	Reverse Recovery Charge		–	53	84	nC
t_{rr}	Reverse Recovery Time	I_F = 28 A, di/dt = 1000 A/μs	–	23	36	ns
Q_{rr}	Reverse Recovery Charge		–	121	194	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Pulse Test: Pulse Width <300 μs, Duty cycle <2.0%.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

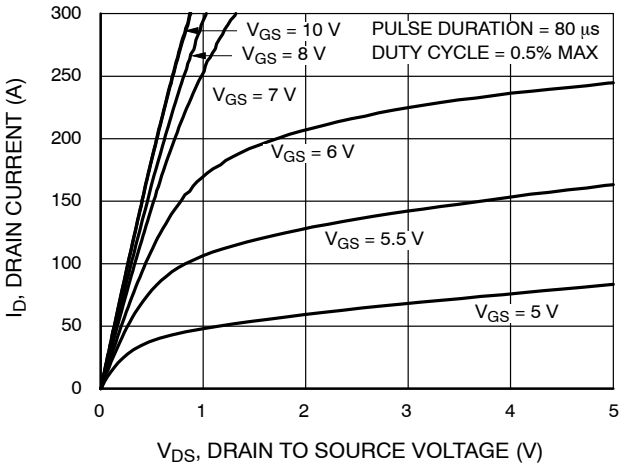


Figure 1. On Region Characteristics

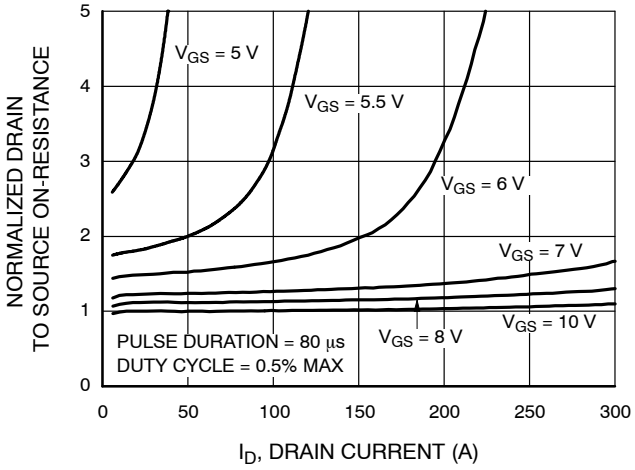


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

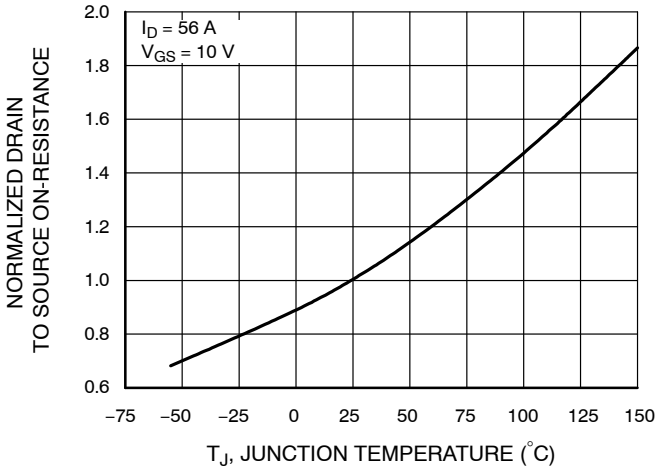


Figure 3. Normalized On Resistance vs. Junction Temperature

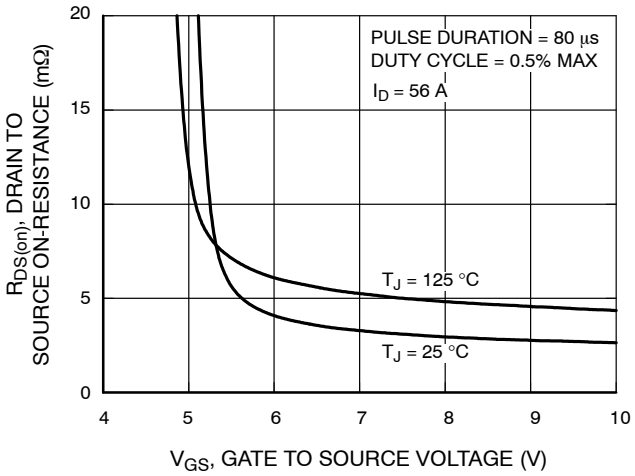


Figure 4. On-Resistance vs. Gate to Source Voltage

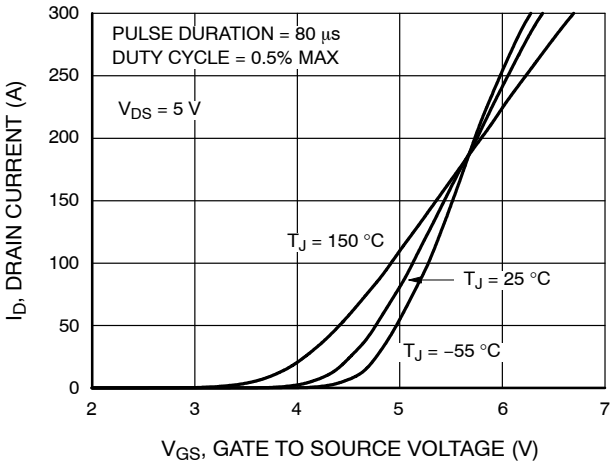


Figure 5. Transfer Characteristics

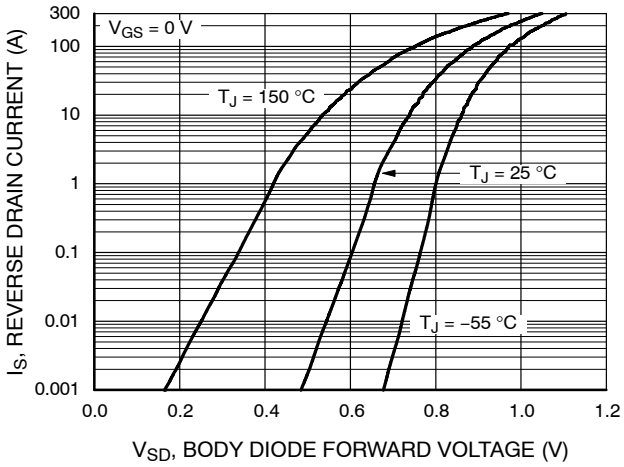


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted) (continued)

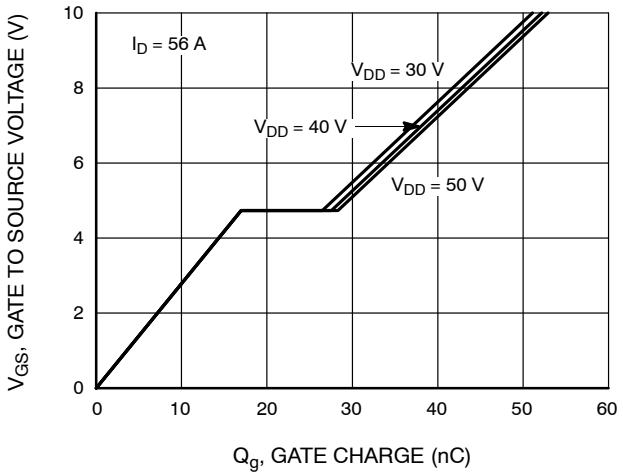


Figure 7. Gate Charge Characteristics

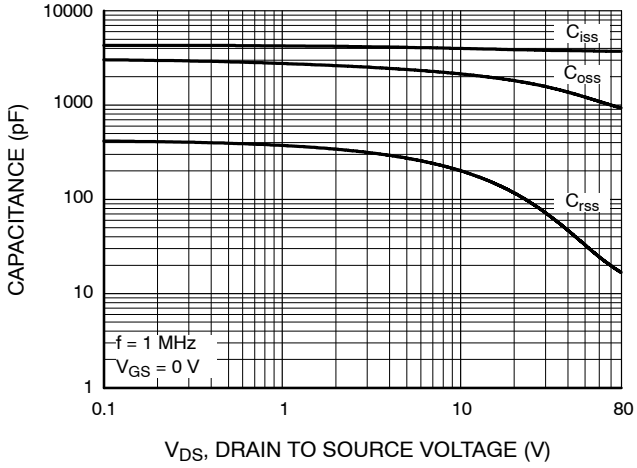


Figure 8. Capacitance vs. Drain to Source Voltage

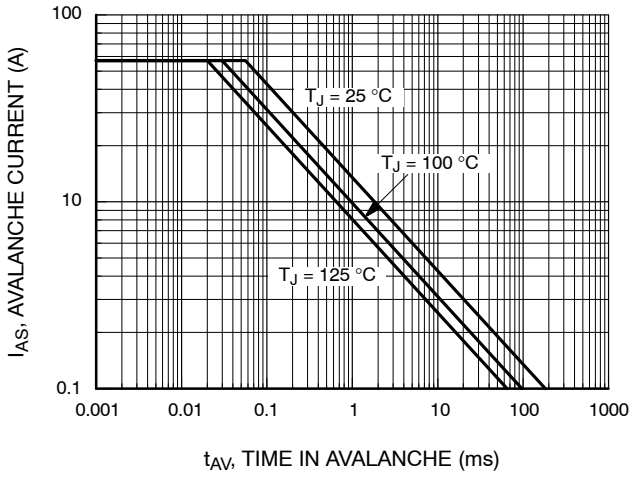


Figure 9. Unclamped Inductive Switching Capability

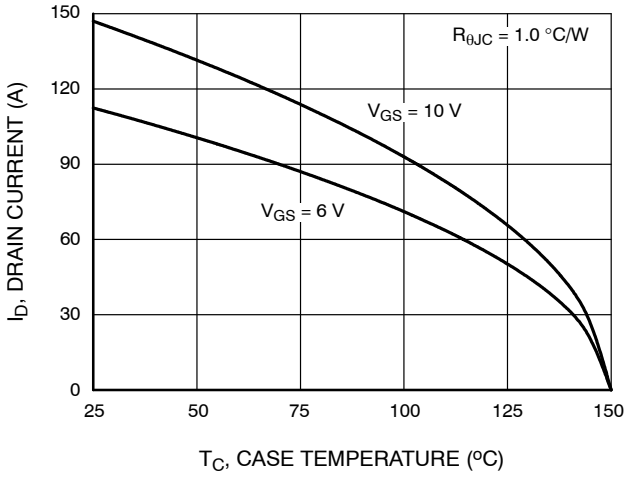


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

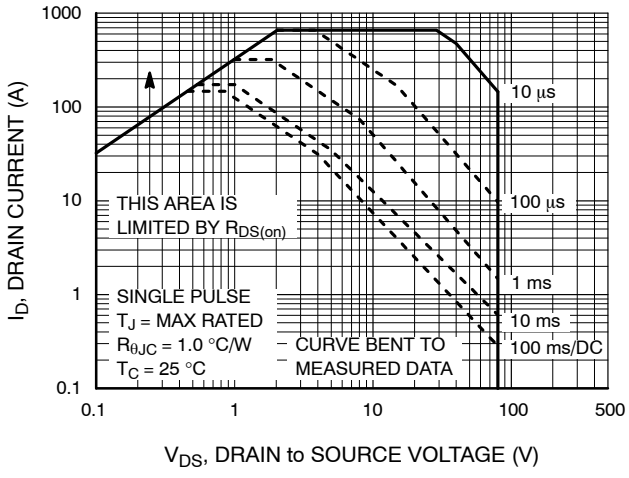


Figure 11. Forward Bias Safe Operating Area

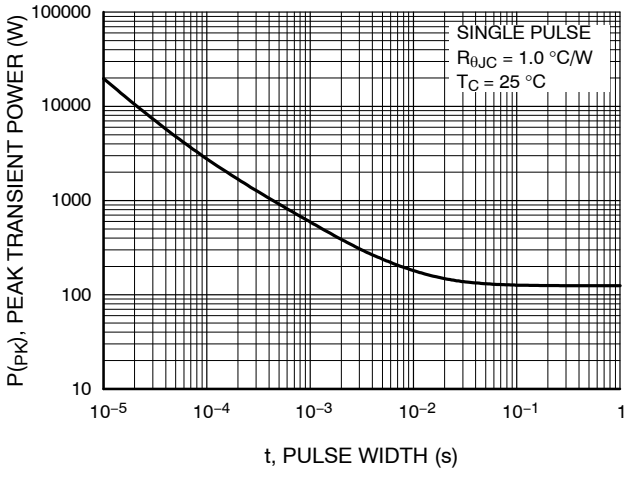


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (T_J = 25 °C unless otherwise noted) (continued)

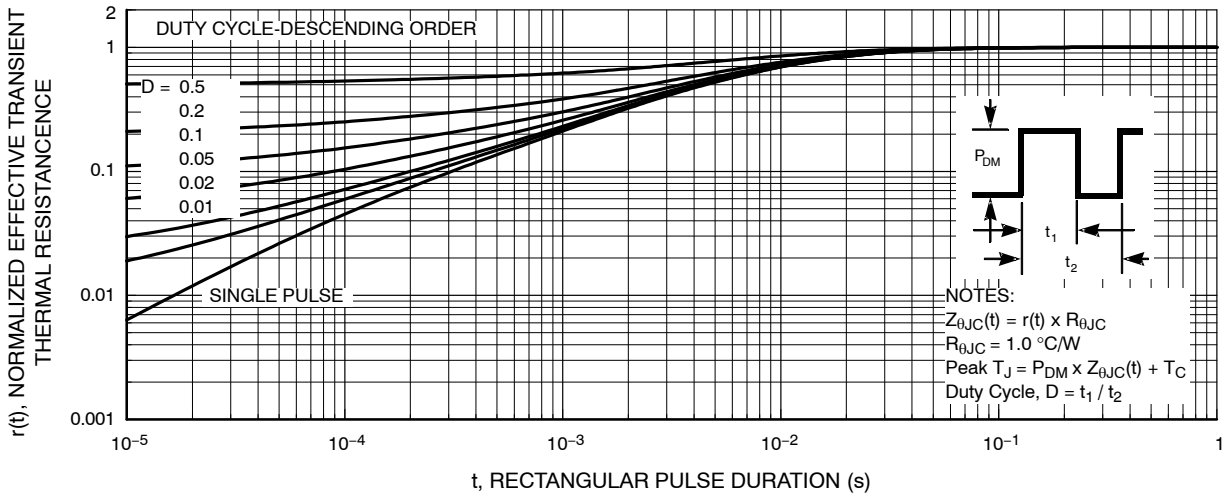
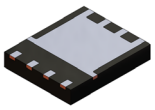


Figure 13. Junction-to-Case Transient Thermal Response Curve

ORDERING INFORMATION

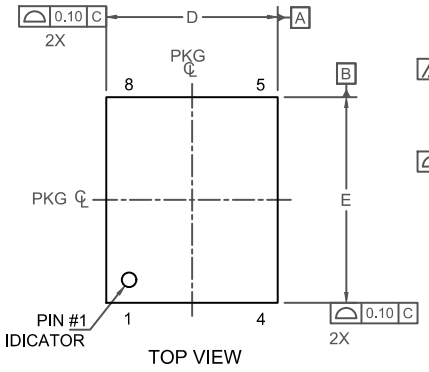
Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
NTMFS08N003C	NTMFS08N003C	PQFN8 5X6, 1.27P Power 56 (Pb-Free)	13”	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

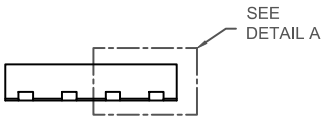


PQFN8 5X6, 1.27P
CASE 483AF
ISSUE A

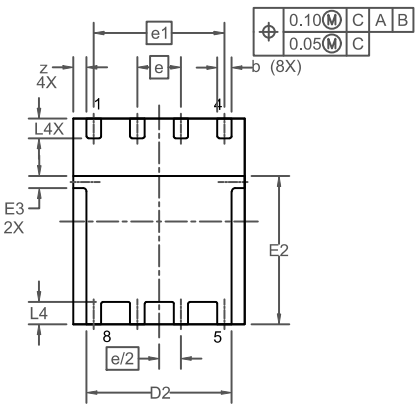
DATE 06 JUL 2021



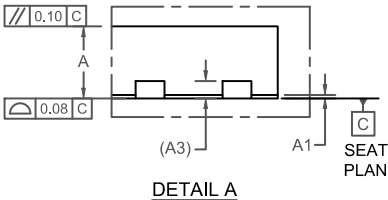
TOP VIEW



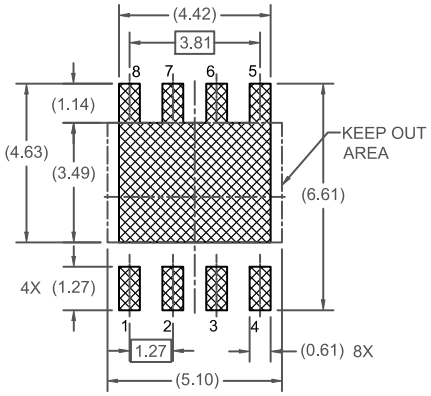
SIDE VIEW



BOTTOM VIEW



DETAIL A
SCALE: 2:1



LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

A) PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF.		
b	0.37	0.42	0.47
D	4.90	5.00	5.10
D2	4.13	4.23	4.33
E	5.90	6.00	6.10
E2	4.23	4.33	4.43
E3	0.35 REF.		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
L	0.52	0.57	0.62
L4	0.55	0.65	0.75
z	0.38 REF		

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DESCRIPTION:	**PQFN8 5X6, 1.27P**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
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