NTHD2102P

Power MOSFET

−8.0 V, −4.6 A Dual P−Channel ChipFET™

Features

- Offers an Ultra Low $R_{DS(on)}$ Solution in the ChipFET Package
- Miniature ChipFET Package 40% Smaller Footprint than TSOP−6 making it an Ideal Device for Applications where Board Space is at a Premium
- Low Profile (<1.1 mm) Allows it to Fit Easily into Extremely Thin Environments such as Portable Electronics
- Designed to Provide Low $R_{DS(on)}$ at Gate Voltage as Low as 1.8 V, the Operating Voltage used in many Logic ICs in Portable Electronics
- Simplifies Circuit Design since Additional Boost Circuits for Gate Voltages are not Required
- Operated at Standard Logic Level Gate Drive, Facilitating Future Migration to Lower Levels using the same Basic Topology
- Pb−Free Package is Available

Applications

- Optimized for Battery and Load Management Applications in Portable Equipment such as MP3 Players, Cell Phones, Digital Cameras, Personal Digital Assistant and other Portable Applications
- Charge Control in Battery Chargers
- Buck and Boost Converters

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	−8.0	V
Gate−to−Source Voltage − Continuous	V_{GS}	±8.0	V
Drain Current − Continuous − 5 seconds	I_D I_D	−3.4 −4.6	A
Total Power Dissipation Continuous @ T_A = 25°C (5 sec) @ T_A = 25°C Continuous @ 85°C (5 sec) @ 85°C	P_D	 1.1 2.1 0.6 1.1	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C
Continuous Source Current (Diode Conduction)	Is	−1.1	A
Thermal Resistance (Note 1) Junction−to−Ambient, 5 sec Junction−to−Ambient, Continuous	 $R_{\theta JA}$ $R_{\theta JA}$	 60 113	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Surface Mounted on FR4 Board using 1 in sq pad size (Cu area = 1.27 in sq [1 oz] including traces).

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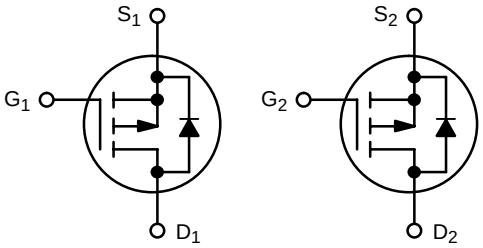
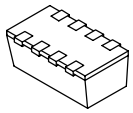
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
−8.0 V	50 mΩ @ −4.5 V	−4.6 A
	68 mΩ @ −2.5 V	
	100 mΩ @ −1.8 V	

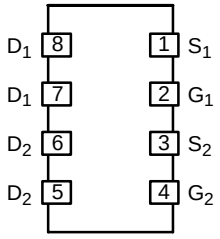


P−Channel MOSFET **P−Channel MOSFET**

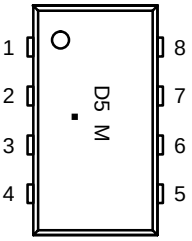


ChipFET
CASE 1206A
STYLE 2

PIN CONNECTIONS



MARKING DIAGRAM



D5 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTHD2102PT1	ChipFET	3000/Tape & Reel
NTHD2102PT1G	ChipFET (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 2) Temperature Coefficient (Positive)	$V_{(Br)DSS}$	V_{GS} = 0 V, I_D = −250 μA	−8.0	−	−	V
Gate−Body Leakage Current Zero	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±8.0 V		−	±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = −6.4 V, V_{GS} = 0 V V_{DS} = −6.4 V, V_{GS} = 0 V, T_J = 85°C		− −	−1.0 −5.0	μA
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = −250 μA	−0.45	−	−1.5	V
Static Drain−to−Source On−Resistance	$R_{DS(on)}$	V_{GS} = −4.5 V, I_D = −3.4 A V_{GS} = −2.5 V, I_D = −2.7 A V_{GS} = −1.8 V, I_D = −1.0 A	− − −	50 68 100	58 85 160	mΩ
Forward Transconductance	g_{FS}	V_{DS} = −5.0 V, I_D = −3.4 A	−	8.0	−	S
Diode Forward Voltage	V_{SD}	I_S = −1.1 A, V_{GS} = 0 V	−	−0.8	−1.2	V
DYNAMIC CHARACTERISTICS						
Input Capacitance	C_{iss}	V_{DS} = −6.4 V	−	715	−	pF
Output Capacitance	C_{oss}	V_{GS} = 0 V	−	160	−	
Transfer Capacitance	C_{rss}	f = 1.0 MHz	−	120	−	
SWITCHING CHARACTERISTICS (Note 3						
Turn−On Delay Time	$t_{d(on)}$	V_{DD} = −6.4 V		8.0	−	ns
Rise Time	t_r	V_{GS} = −4.5 V		20	−	
Turn−Off Delay Time	$t_{d(off)}$	I_D = −3.2 A		20	−	
Fall Time	t_f	R_G = 2.0 Ω		15	−	
Gate Charge	Q_g	V_{GS} = −2.5 V		8.0	16	nC
	Q_{gs}	I_D = −3.2 A		2.2	−	
	Q_{gd}	V_{DS} = −6.4 V		4.0	−	
Source−Drain Reverse Recovery Time	t_{rr}	I_F = −0.9 A, di/dt = 100		15	30	nA

2. Pulse Test: Pulse Width = 250 μs, Duty Cycle = 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

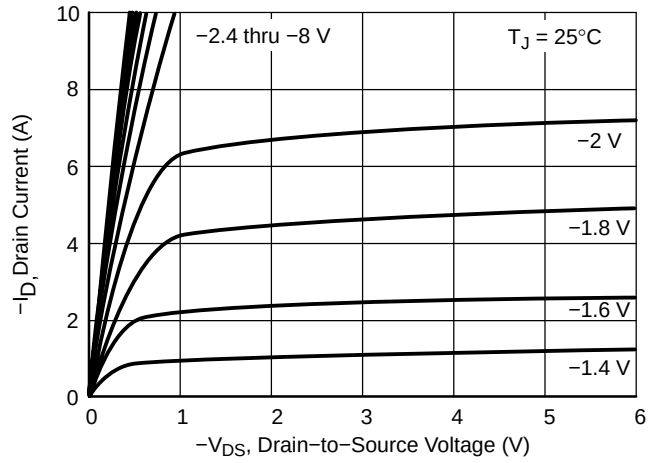


Figure 1. On−Region Characteristics

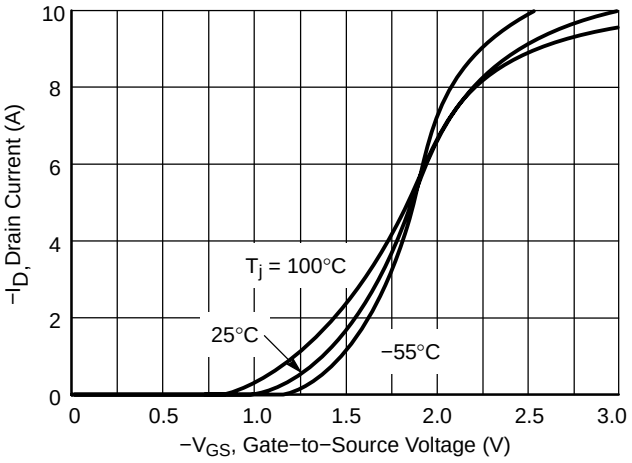


Figure 2. Transfer Characteristics

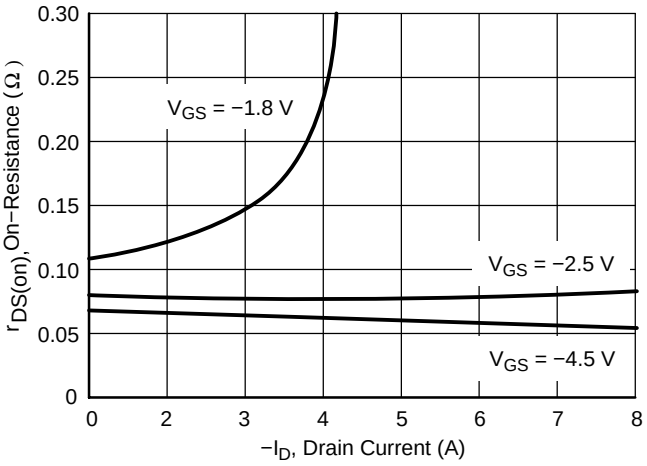


Figure 3. On−Resistance vs. Drain Current and Gate Voltage

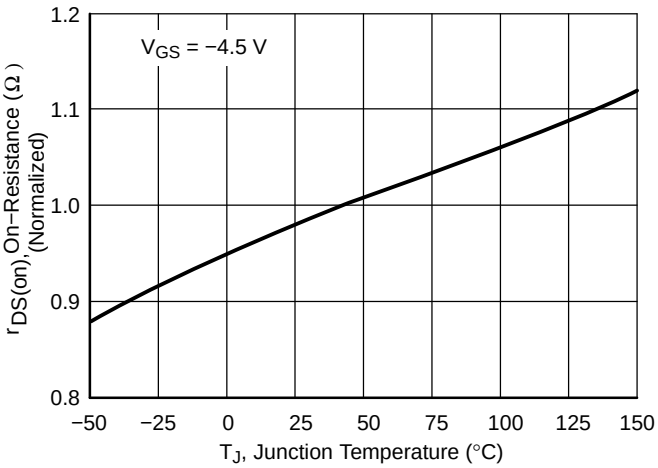


Figure 4. On−Resistance Variation vs. Temperature

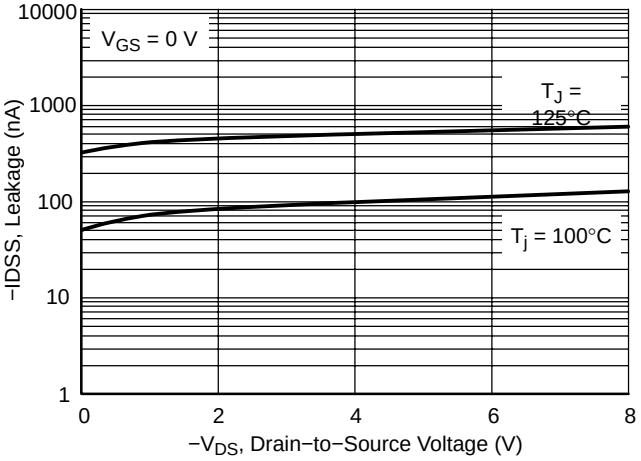


Figure 5. Drain−to−Source Leakage Current vs. Voltage

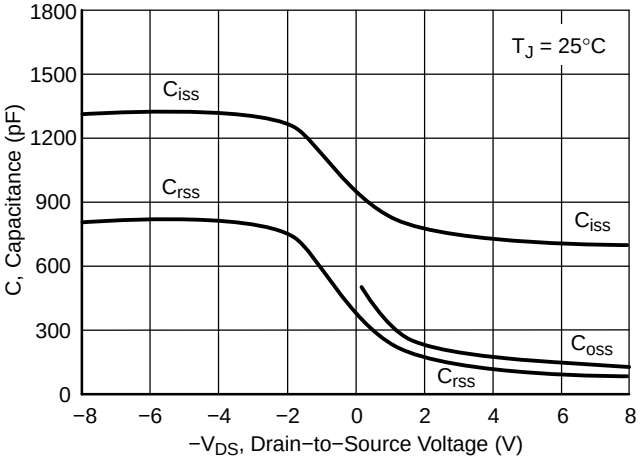


Figure 6. Capacitance Variation

TYPICAL ELECTRICAL CHARACTERISTICS

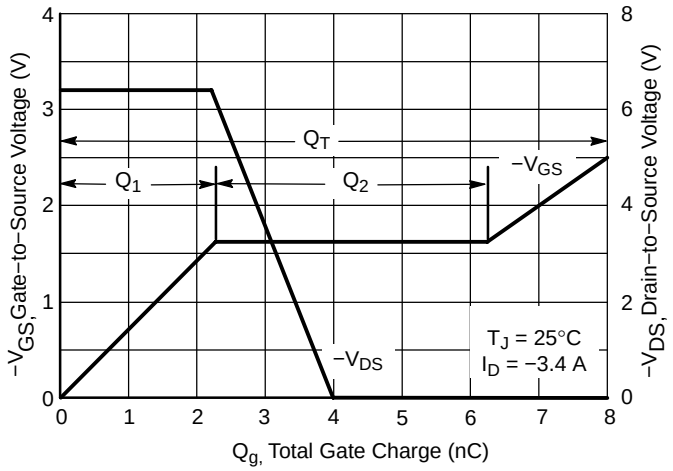


Figure 7. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

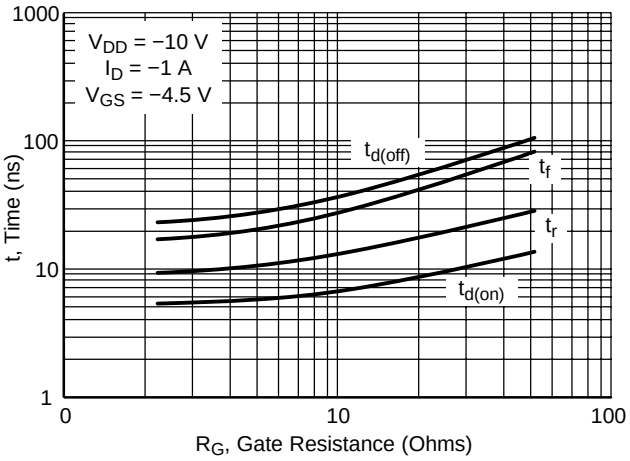


Figure 8. Resistive Switching Time Variation vs. Gate Resistance

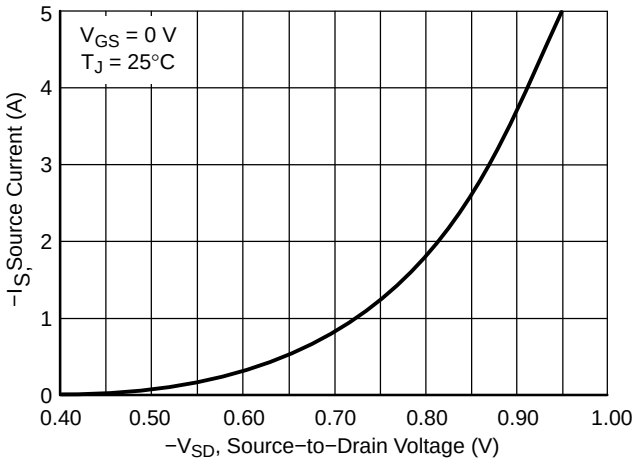


Figure 9. Diode Forward Voltage vs. Current

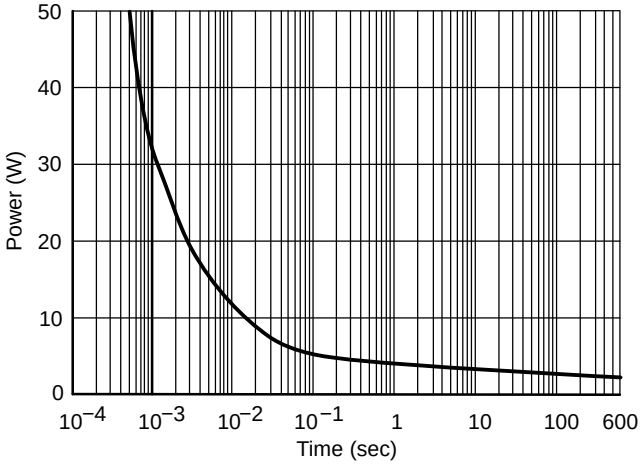


Figure 10. Single Pulse Power

TYPICAL ELECTRICAL CHARACTERISTICS

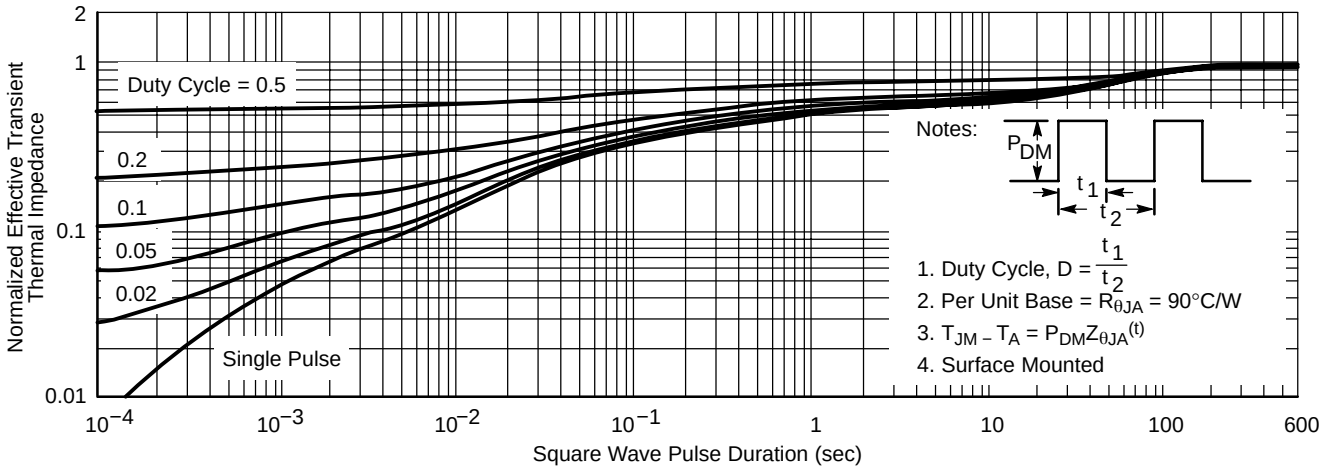


Figure 11. Normalized Thermal Transient Impedance, Junction−to−Ambient

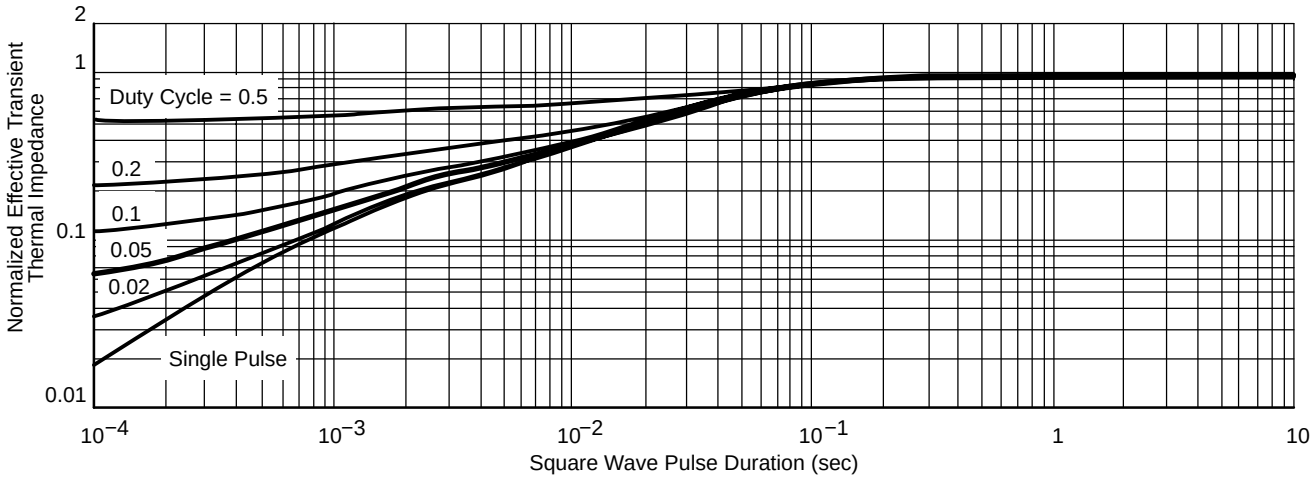


Figure 12. Normalized Thermal Transient Impedance, Junction−to−Foot

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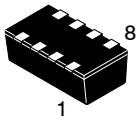
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

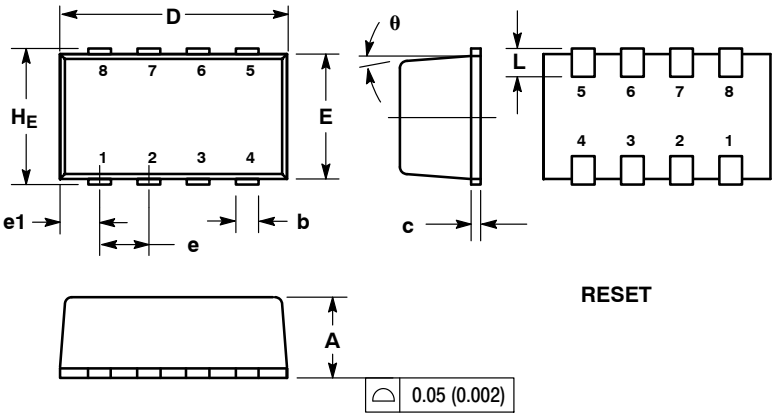
ON Semiconductor®

ChipFET™
CASE1206A−03
ISSUE K

DATE 19 MAY 2009



SCALE 1:1



RESET

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.00	1.05	1.10	0.039	0.041	0.043
b	0.25	0.30	0.35	0.010	0.012	0.014
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.95	3.05	3.10	0.116	0.120	0.122
E	1.55	1.65	1.70	0.061	0.065	0.067
e	0.65 BSC			0.025 BSC		
e1	0.55 BSC			0.022 BSC		
L	0.28	0.35	0.42	0.011	0.014	0.017
H_E	1.80	1.90	2.00	0.071	0.075	0.079
θ	5° NOM			5° NOM		

STYLE 1:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 2:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

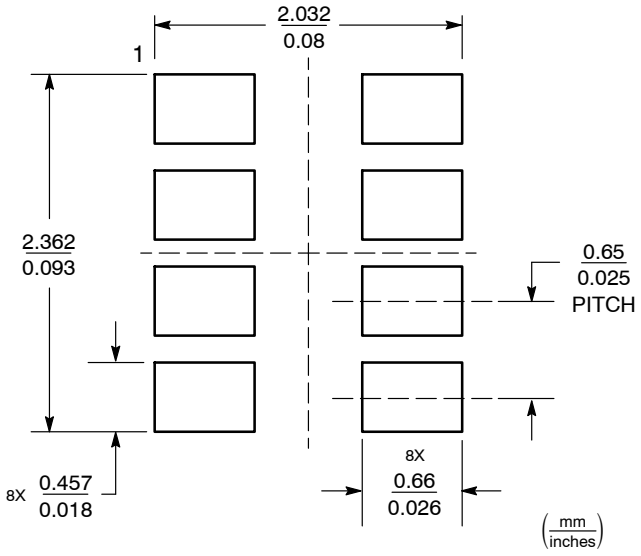
STYLE 3:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. COLLECTOR
4. BASE
5. EMITTER
6. COLLECTOR
7. COLLECTOR
8. COLLECTOR

STYLE 5:
PIN 1. ANODE
2. ANODE
3. DRAIN
4. DRAIN
5. SOURCE
6. GATE
7. CATHODE
8. CATHODE

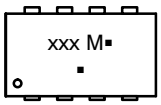
STYLE 6:
PIN 1. ANODE
2. DRAIN
3. DRAIN
4. GATE
5. SOURCE
6. DRAIN
7. DRAIN
8. CATHODE / DRAIN

SOLDERING FOOTPRINT



Basic Style

GENERIC MARKING DIAGRAM*



xxx = Specific Device Code
M = Month Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

OPTIONAL SOLDERING FOOTPRINTS ON PAGE 2

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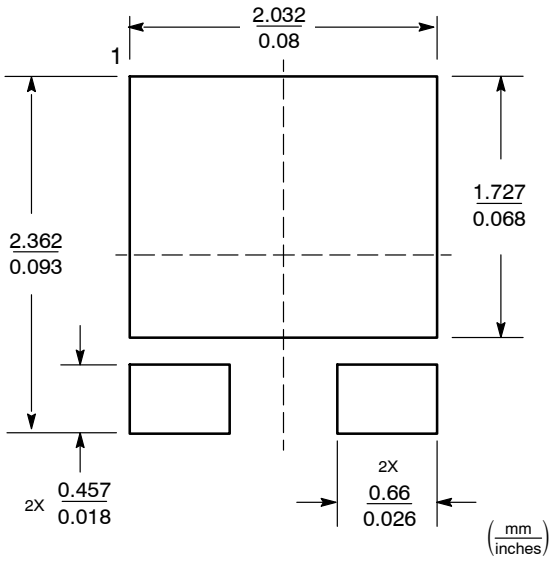
DESCRIPTION:	**ChipFET**	**PAGE 1 OF 2**

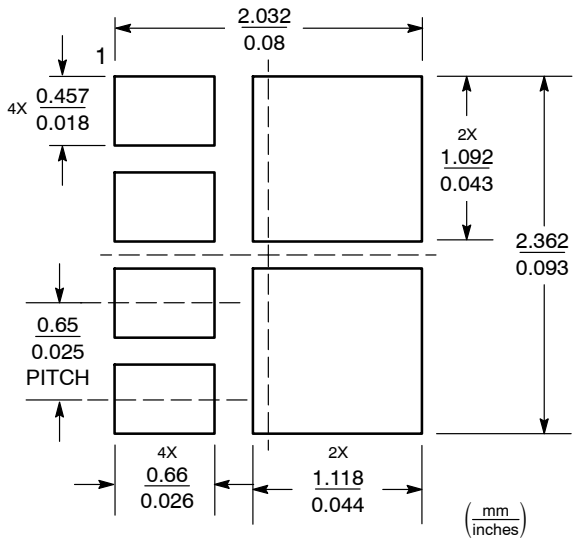
ChipFET™
CASE 1206A−03
ISSUE K

DATE 19 MAY 2009

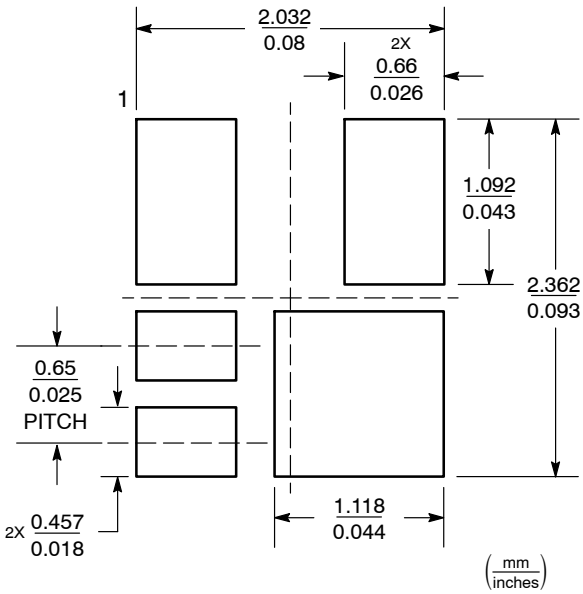
ADDITIONAL SOLDERING FOOTPRINTS*



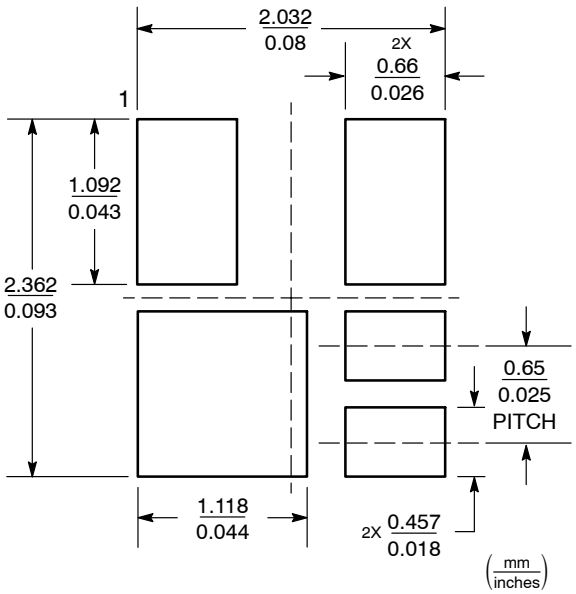
Styles 1 and 4



Style 2



Style 3



Style 5

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**ChipFET**	**PAGE 2 OF 2**

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