# NTD4905N

## Power MOSFET

### 30 V, 67 A, Single N−Channel, DPAK/IPAK

**Features**

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- These are Pb−Free Devices

**Applications**

- CPU Power Delivery
- DC−DC Converters

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| Drain−to−Source Voltage | | | $V_{DSS}$ | 30 | V |
| Gate−to−Source Voltage | | | $V_{GS}$ | ±20 | V |
| Continuous Drain Current ($R_{\theta JA}$) (Note 1) | Steady State | $T_A$ = 25°C | $I_D$ | 16.3 | A |
| | | $T_A$ = 100°C | | 11.5 | |
| Power Dissipation ($R_{\theta JA}$) (Note 1) | | $T_A$ = 25°C | $P_D$ | 2.63 | W |
| Continuous Drain Current ($R_{\theta JA}$) (Note 2) | | $T_A$ = 25°C | $I_D$ | 12 | A |
| | | $T_A$ = 100°C | | 8.3 | |
| Power Dissipation ($R_{\theta JA}$) (Note 2) | | $T_A$ = 25°C | $P_D$ | 1.4 | W |
| Continuous Drain Current ($R_{\theta JC}$) (Note 1) | | $T_C$ = 25°C | $I_D$ | 67 | A |
| | | $T_C$ = 100°C | | 47 | |
| Power Dissipation ($R_{\theta JC}$) (Note 1) | | $T_C$ = 25°C | $P_D$ | 44 | W |
| Pulsed Drain Current | $t_p$=10μs | $T_A$ = 25°C | $I_{DM}$ | 264 | A |
| Current Limited by Package | | $T_A$ = 25°C | $I_{DmaxPkg}$ | 90 | A |
| Operating Junction and Storage Temperature | | | $T_J$, $T_{stg}$ | −55 to 175 | °C |
| Source Current (Body Diode) | | | $I_S$ | 40 | A |
| Drain to Source dV/dt | | | dV/dt | 6.5 | V/ns |
| Single Pulse Drain−to−Source Avalanche Energy ($T_J$ = 25°C, $V_{DD}$ = 24 V, $V_{GS}$ = 10 V, L = 0.1 mH, $I_{L(pk)}$ = 35 A, $R_G$ = 25 Ω) | | | $E_{AS}$ | 61 | mJ |
| Lead Temperature for Soldering Purposes (1/8″ from case for 10 s) | | | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

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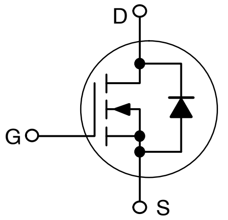
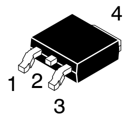
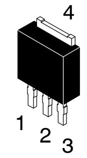
| $V_{(BR)DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| 30 V | 4.5 mΩ @ 10 V | 67 A |
| | 7.0 mΩ @ 4.5 V | |



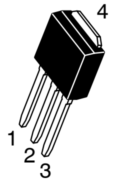
**N−Channel**



**CASE 369AA**
**DPAK**
**(Bent Lead)**
**STYLE 2**

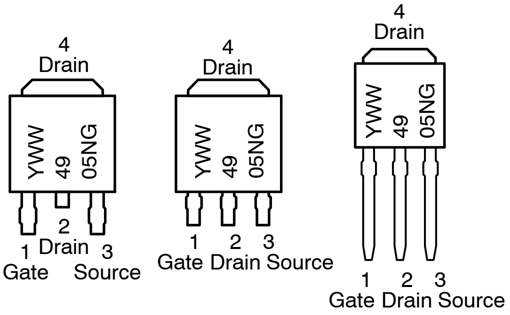


**CASE 369AD**
**IPAK**
**(Straight Lead)**



**CASE 369D**
**IPAK**
**(Straight Lead**
**DPAK)**

**MARKING DIAGRAMS**
**& PIN ASSIGNMENTS**



Y = Year
WW = Work Week
4905N = Device Code
G = Pb−Free Package

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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## THERMAL RESISTANCE MAXIMUM RATINGS

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Junction−to−Case (Drain) | $R_{\theta JC}$ | 3.4 | °C/W |
| Junction−to−Tab (Drain) | $R_{\theta JC-TAB}$ | 4.3 | |
| Junction−to−Ambient − Steady State (Note 1) | $R_{\theta JA}$ | 57 | |
| Junction−to−Ambient − Steady State (Note 2) | $R_{\theta JA}$ | 109 | |

1. Surface−mounted on FR4 board using 1 in sq pad size, 1 oz Cu.
2. Surface−mounted on FR4 board using the minimum recommended pad size.

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain−to−Source Breakdown Voltage | $V_{(BR)DSS}$ | $V_{GS}$ = 0 V, $I_D$ = 250 μA | | 30 | | | V |
| Drain−to−Source Breakdown Voltage Temperature Coefficient | $V_{(BR)DSS}/T_J$ | | | | 15 | | mV/°C |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{GS}$ = 0 V,<br>$V_{DS}$ = 24 V | $T_J$ = 25°C | | | 1.0 | μA |
| | | | $T_J$ = 125°C | | | 10 | |
| Gate−to−Source Leakage Current | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | | | | ±100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | | |
| Gate Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250 μA | | 1.0 | 1.6 | 2.2 | V |
| Negative Threshold Temperature Coefficient | $V_{GS(TH)}/T_J$ | | | | 4.0 | | mV/°C |
| Drain−to−Source On Resistance | $R_{DS(on)}$ | $V_{GS}$ = 10 V | $I_D$ = 30 A | | 3.9 | 4.5 | mΩ |
| | | | $I_D$ = 15 A | | 3.9 | | |
| | | $V_{GS}$ = 4.5 V | $I_D$ = 30 A | | 5.4 | 7.0 | |
| | | | $I_D$ = 15 A | | 5.4 | | |
| Forward Transconductance | gFS | $V_{DS}$ = 1.5 V, $I_D$ = 30 A | | | 65 | | S |
| **CHARGES AND CAPACITANCES** | | | | | | | |
| Input Capacitance | $C_{iss}$ | $V_{GS}$ = 0 V, f = 1.0 MHz,<br>$V_{DS}$ = 15 V | | | 2340 | | pF |
| Output Capacitance | $C_{oss}$ | | | | 763 | | |
| Reverse Transfer Capacitance | $C_{rss}$ | | | | 27 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V,<br>$I_D$ = 30 A | | | 14 | | nC |
| Threshold Gate Charge | $Q_{G(TH)}$ | | | | 3.7 | | |
| Gate−to−Source Charge | $Q_{GS}$ | | | | 6.8 | | |
| Gate−to−Drain Charge | $Q_{GD}$ | | | | 2.2 | | |
| Total Gate Charge | $Q_{G(TOT)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V,<br>$I_D$ = 30 A | | | 33 | | nC |
| **SWITCHING CHARACTERISTICS** (Note 4) | | | | | | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 4.5 V, $V_{DS}$ = 15 V,<br>$I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 13.8 | | ns |
| Rise Time | $t_r$ | | | | 20.5 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 21.3 | | |
| Fall Time | $t_f$ | | | | 5.4 | | |
| Turn−On Delay Time | $t_{d(on)}$ | $V_{GS}$ = 10 V, $V_{DS}$ = 15 V,<br>$I_D$ = 15 A, $R_G$ = 3.0 Ω | | | 9.7 | | ns |
| Rise Time | $t_r$ | | | | 19.7 | | |
| Turn−Off Delay Time | $t_{d(off)}$ | | | | 27.8 | | |
| Fall Time | $t_f$ | | | | 3.6 | | |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Test Condition | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DRAIN–SOURCE DIODE CHARACTERISTICS** | | | | | | | |
| Forward Diode Voltage | $V_{SD}$ | $V_{GS}$ = 0 V,<br>$I_S$ = 30 A | $T_J$ = 25°C | | 0.86 | 1.1 | V |
| | | | $T_J$ = 125°C | | 0.74 | | |
| Reverse Recovery Time | $t_{RR}$ | $V_{GS}$ = 0 V, dIs/dt= 100 A/μs,<br>$I_S$ = 30 A | | | 37.5 | | ns |
| Charge Time | ta | | | | 19 | | |
| Discharge Time | tb | | | | 18.5 | | |
| Reverse Recovery Time | $Q_{RR}$ | | | | 31 | | nC |
| **PACKAGE PARASITIC VALUES** | | | | | | | |
| Source Inductance (Note 5) | $L_S$ | $T_A$ = 25°C | | | 2.85 | | nH |
| Drain Inductance, DPAK | $L_D$ | | | | 0.0164 | | |
| Drain Inductance, IPAK (Note 5) | $L_D$ | | | | 1.88 | | |
| Gate Inductance (Note 5) | $L_G$ | | | | 4.9 | | |
| Gate Resistance | $R_G$ | | | | 1.0 | 2.0 | Ω |

5. Assume terminal length of 110 mils.

## TYPICAL PERFORMANCE CURVES

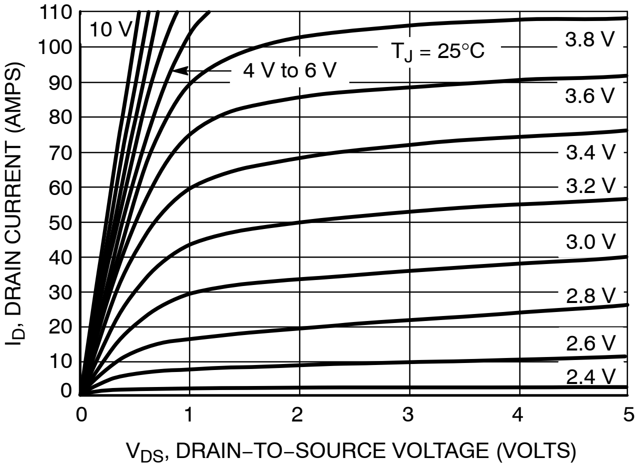


**Figure 1. On−Region Characteristics**

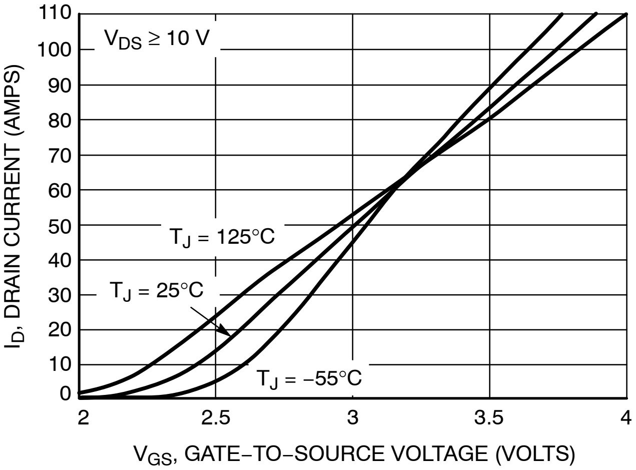


**Figure 2. Transfer Characteristics**

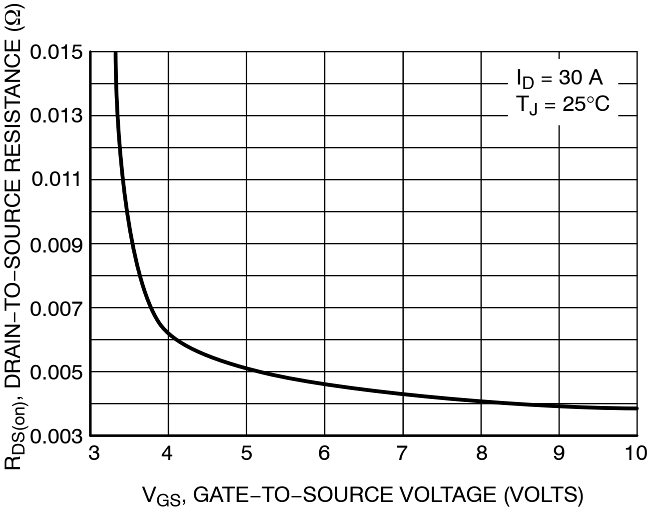


**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

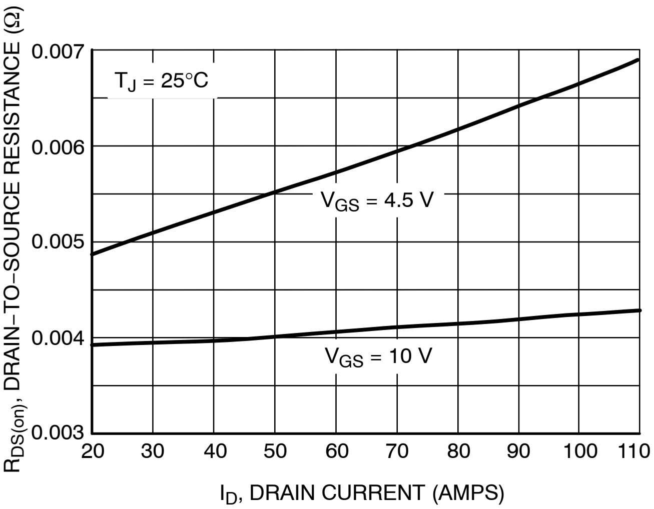


**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

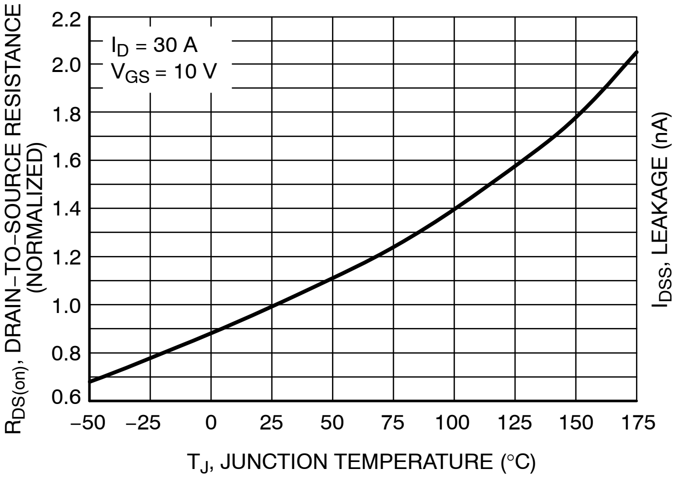


**Figure 5. On−Resistance Variation with Temperature**

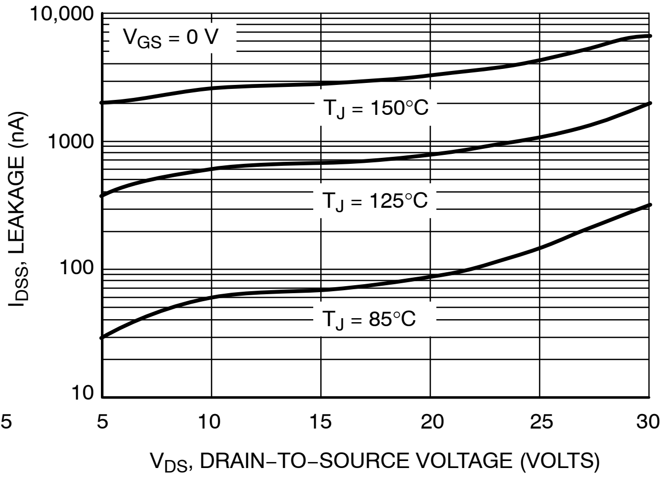
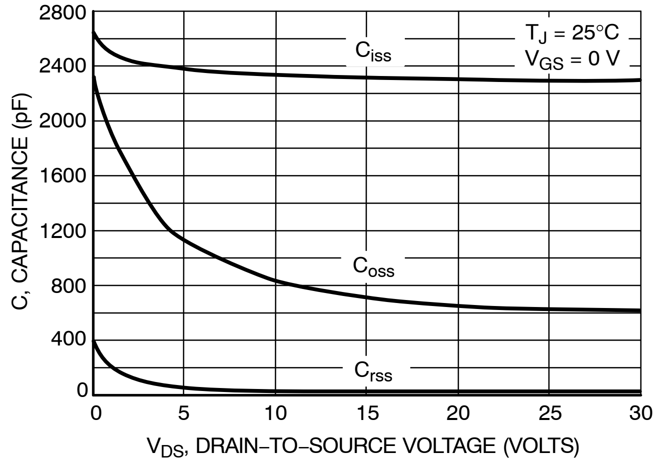


**Figure 6. Drain−to−Source Leakage Current vs. Drain Voltage**

## TYPICAL PERFORMANCE CURVES



3600

3200

**Figure 7. Capacitance Variation**

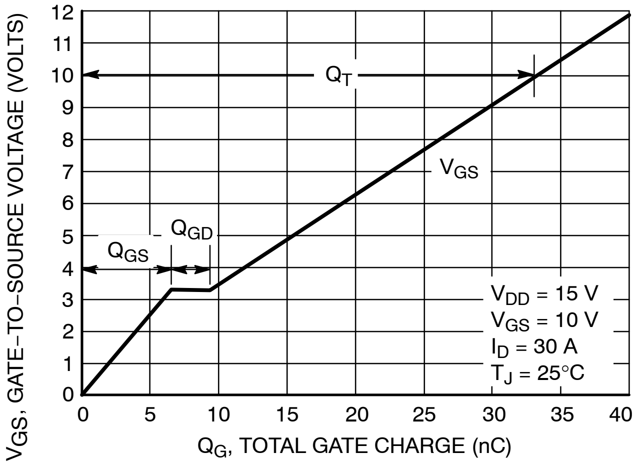


**Figure 8. Gate−To−Source and Drain−To−Source Voltage vs. Total Charge**

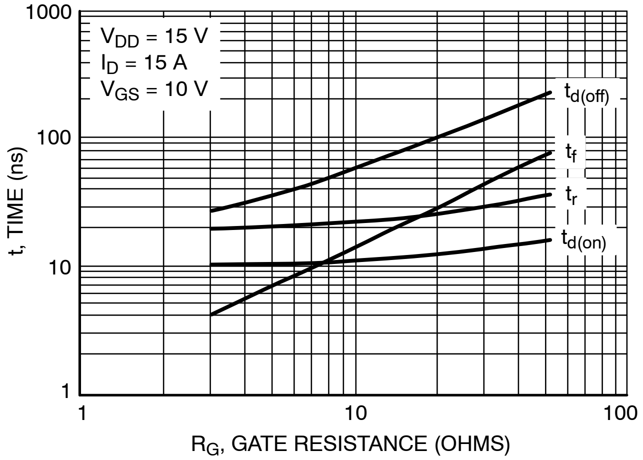


**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

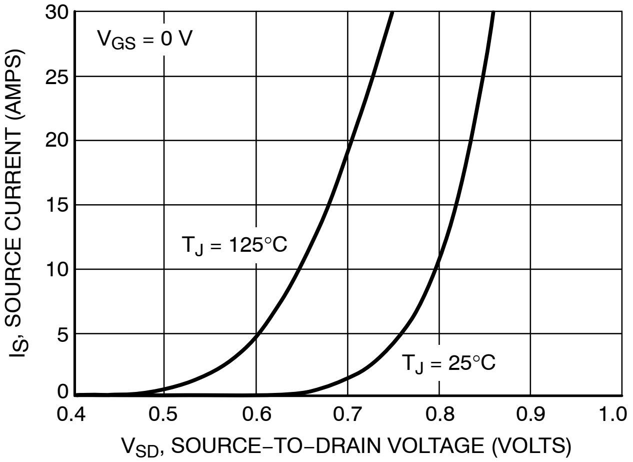


**Figure 10. Diode Forward Voltage vs. Current**

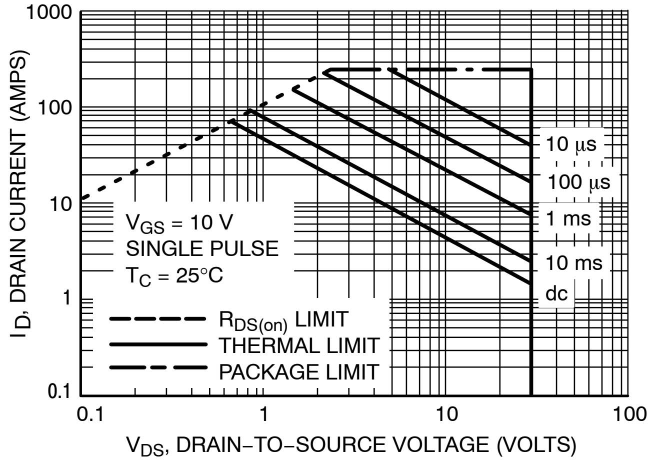


**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

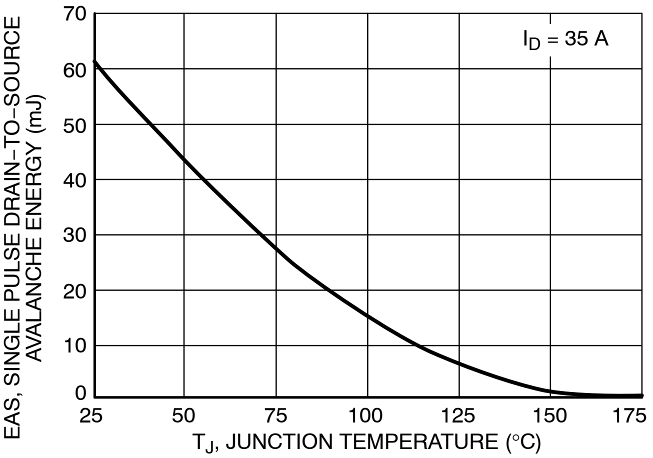


**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

## TYPICAL PERFORMANCE CURVES

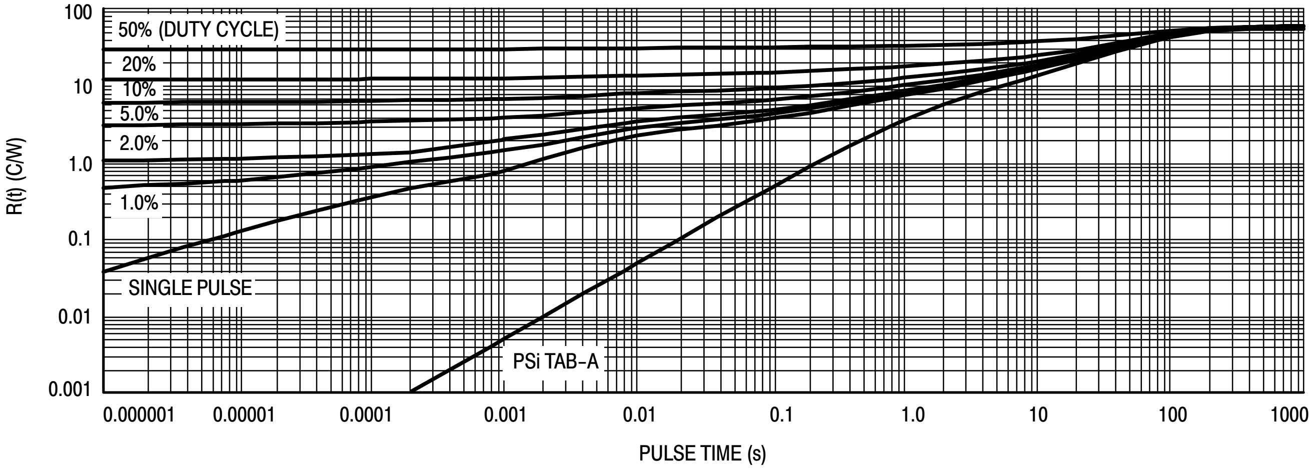


**Figure 13. FET Thermal Response**

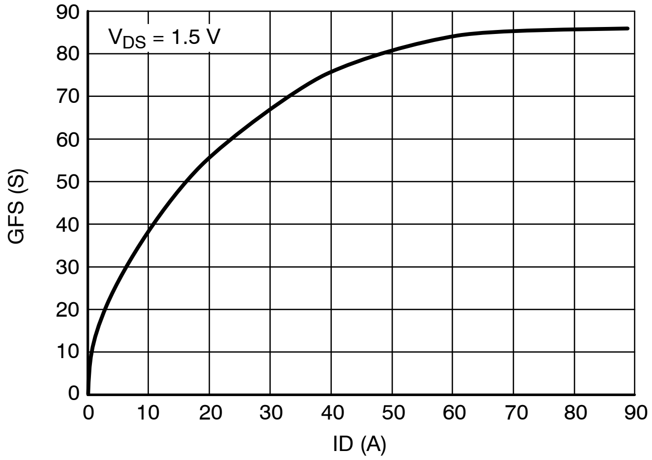


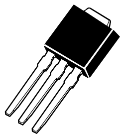
**Figure 14. GFS vs ID**

### ORDERING INFORMATION

| Order Number | Package | Shipping[†] |
|---|---|---|
| NTD4905NT4G | DPAK<br>(Pb−Free) | 2500 / Tape & Reel |
| NTD4905N−1G | IPAK<br>(Pb−Free) | 75 Units / Rail |
| NTD4905N−35G | IPAK Trimmed Lead<br>(Pb−Free) | 75 Units / Rail |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

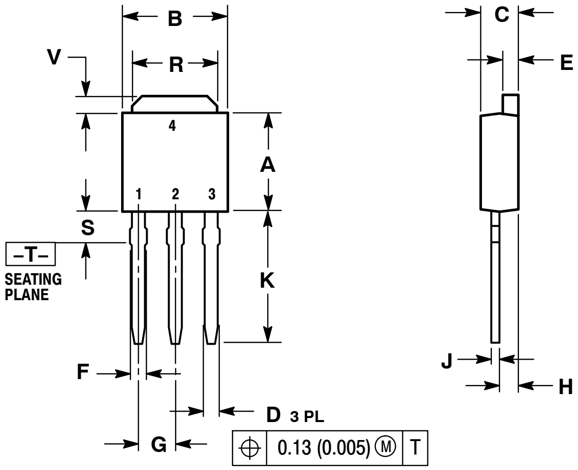
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



SCALE 1:1

## DPAK INSERTION MOUNT
CASE 369
ISSUE O

DATE 02 JAN 2000



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.235 | 0.250 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.033 | 0.040 | 0.84 | 1.01 |
| F | 0.037 | 0.047 | 0.94 | 1.19 |
| G | 0.090 BSC | | 2.29 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.350 | 0.380 | 8.89 | 9.65 |
| R | 0.175 | 0.215 | 4.45 | 5.46 |
| S | 0.050 | 0.090 | 1.27 | 2.28 |
| V | 0.030 | 0.050 | 0.77 | 1.27 |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

| | | |
|---|---|---|
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| **DESCRIPTION:** | **DPAK INSERTION MOUNT** | **PAGE 1 OF 1** |

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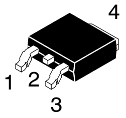
# DPAK (SINGLE GUAGE)

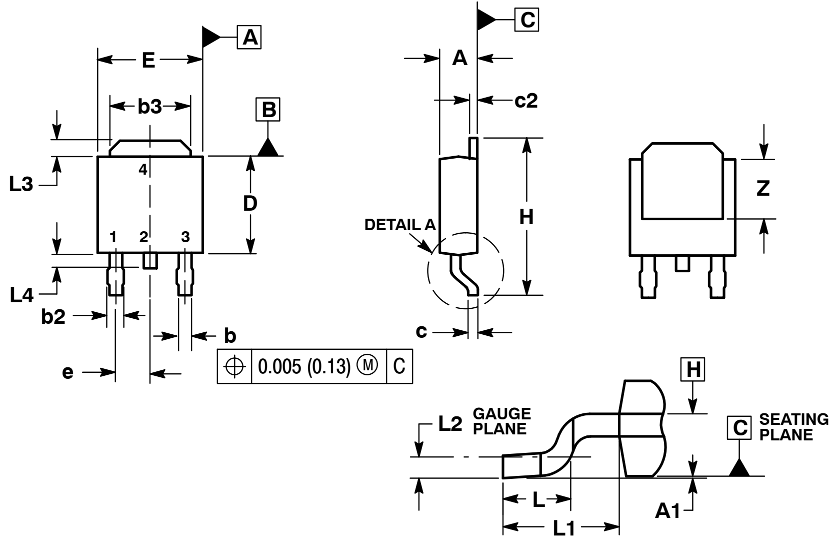
CASE 369AA
ISSUE B

DATE 03 JUN 2010



**SCALE 1:1**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.



**DETAIL A**
**ROTATED 90° CW**

| DIM | INCHES |  | MILLIMETERS |  |
|---|---|---|---|---|
|  | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC |  | 2.29 BSC |  |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF |  | 2.74 REF |  |
| L2 | 0.020 BSC |  | 0.51 BSC |  |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

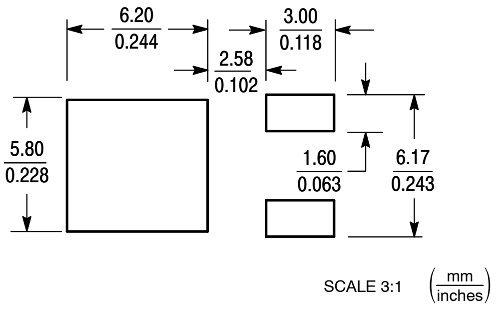
STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

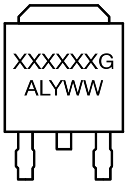
STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

## SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## GENERIC MARKING DIAGRAM*



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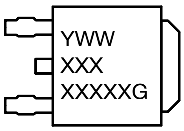

**Discrete**

| | |
|---|---|
| XXXXXX | = Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **DPAK (SINGLE GAUGE)** | **PAGE 1 OF 1** |

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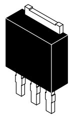
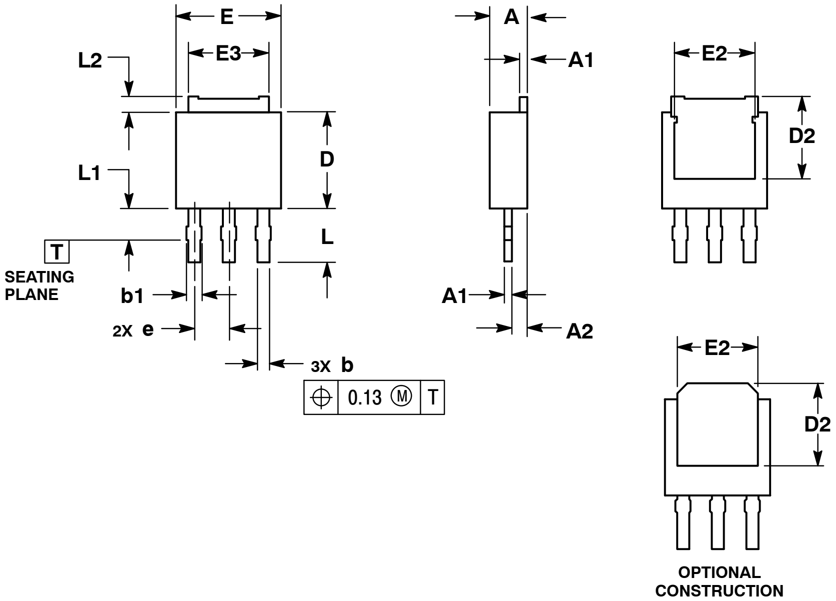
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



### 3.5 MM IPAK, STRAIGHT LEAD
CASE 369AD
ISSUE B

DATE 18 APR 2013

SCALE 1:1

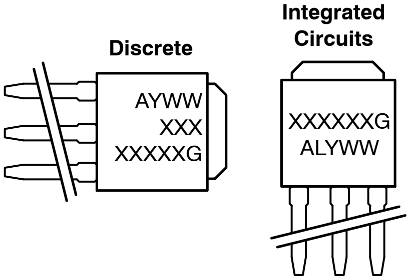


OPTIONAL CONSTRUCTION

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL TIP.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD GATE OR MOLD FLASH.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 2.19 | 2.38 |
| A1 | 0.46 | 0.60 |
| A2 | 0.87 | 1.10 |
| b | 0.69 | 0.89 |
| b1 | 0.77 | 1.10 |
| D | 5.97 | 6.22 |
| D2 | 4.80 | --- |
| E | 6.35 | 6.73 |
| E2 | 4.57 | 5.45 |
| E3 | 4.45 | 5.46 |
| e | 2.28 BSC | |
| L | 3.40 | 3.60 |
| L1 | --- | 2.10 |
| L2 | 0.89 | 1.27 |

### GENERIC MARKING DIAGRAMS*



Discrete

Integrated Circuits

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2

STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

XXXXXX = Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **3.5 MM IPAK, STRAIGHT LEAD** | **PAGE 1 OF 1** |

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