**NOIV1SN025KA**

**VITA 25K Image Sensor**

**Features**

- 5120 x 5120 Active Pixels
- 4.5 μm x 4.5 μm Square Pixels
- 35 mm Optical Format
- Monochrome (SN) or Color (SE)
- 53 Frames per Second (fps) at Full Resolution
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- 32 Low-voltage Differential Signaling (LVDS) High-speed Serial Outputs
- Random Programmable Region of Interest (ROI) Readout
- Pipelined and Triggered Global Shutter, Rolling Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- Serial Peripheral Interface (SPI)
- Operational Range: −40°C to +85°C
- 355-pin μPGA Package
- 3.4 W Power Dissipation
- These Devices are Pb–Free and are RoHS Compliant

**Applications**

- Machine Vision
- Motion Monitoring
- Intelligent Traffic Systems (ITS)
- Pick and Place Machines
- Inspection
- Metrology

**Description**

The VITA 25K is a 5120 x 5120 CMOS image sensor delivering high resolution images at frame rates up to 53 frames per second. The high sensitivity 4.5 μm x 4.5 μm pixels support pipelined and triggered global shutter readout modes and can also be operated in a low noise rolling shutter mode. In rolling shutter mode, the sensor supports correlated double sampling readout, reducing noise and increasing the dynamic range.

The sensor has on-chip programmable gain amplifiers and 10-bit A/D converters. The image’s black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest. Up to 32 regions can be programmed, achieving even higher frame rates.

The image data interface consists of 32 LVDS lanes. Each channel runs at 620 Mbps. A separate synchronization channel containing payload information is provided to facilitate the image reconstruction at the receive end.

The VITA 25K is packaged in a ceramic 355-pin μPGA package and is available in a monochrome, color and windowless versions.

Contact your local ON Semiconductor office for more information.

**ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Package</th>
</tr>
</thead>
<tbody>
<tr>
<td>NOIV1SN025KA-GDC</td>
<td>Mono micro lens</td>
<td>355-μPGA</td>
</tr>
<tr>
<td>NOIV1SE025KA-GDC</td>
<td>Color micro lens</td>
<td></td>
</tr>
<tr>
<td>NOIV1SN025KA-GWC</td>
<td>Mono micro lens windowless</td>
<td></td>
</tr>
</tbody>
</table>
Package Mark
Following is the VITA 25K production package mark:
   Side 1 near Pin 1: NOIV1S * 025KA–GDC, where N = mono micro lens, E = color micro lens
   Side 2: AWLYYWW, NNNN where AWLYYWW is the lot traceability, and NNNN is the serial number

Windowless Devices
The windowless devices are assembled in the same package as the windowed devices with the exception that the windowless devices are delivered with the glass lid (referenced in Figure 37 and Figure 39), taped on to the package. The glass lid is taped to the package in a clean room environment, soon after the wire bonding process, to maintain silicon integrity and wire dressing. The windowless devices are tested according to the Standard Acceptance Criteria and are electro optically identical to production devices WITH GLASS LID. Please note the RMA policy on Page NO TAG for windowless devices.

Please contact your local sales office for entering a windowless order.
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<th></th>
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Key Specifications

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<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active pixels</td>
<td>5120 (H) x 5120 (V)</td>
</tr>
<tr>
<td>Pixel size</td>
<td>4.5 μm x 4.5 μm</td>
</tr>
<tr>
<td>Pixel type</td>
<td>Global shutter pixel architecture</td>
</tr>
<tr>
<td>Shutter type</td>
<td>Pipelined and triggered global shutter, rolling shutter</td>
</tr>
<tr>
<td>Master clock</td>
<td>310 MHz (10-bit)</td>
</tr>
<tr>
<td></td>
<td>248 MHz (8-bit)</td>
</tr>
<tr>
<td>Windowing features</td>
<td>32 Randomly programmable windows. Normal, sub-sampled and binned readout modes</td>
</tr>
<tr>
<td>ADC resolution</td>
<td>10-bit, 8-bit</td>
</tr>
<tr>
<td>Number of LVDS outputs</td>
<td>32 data + 1 sync + 1 clock</td>
</tr>
<tr>
<td>Data rate</td>
<td>32 x 620 Mbps (10-bit)</td>
</tr>
<tr>
<td></td>
<td>32 x 496 Mbps (8-bit)</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>3.4 W</td>
</tr>
<tr>
<td>Package type</td>
<td>355 μPGA</td>
</tr>
<tr>
<td>Color</td>
<td>RGB color, mono</td>
</tr>
</tbody>
</table>

Electro–Optical Specifications

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
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<tbody>
<tr>
<td>Frame rate</td>
<td>53 fps at full resolution</td>
</tr>
<tr>
<td>Optical format</td>
<td>35 mm</td>
</tr>
<tr>
<td>Conversion gain</td>
<td>0.0644 LSB10/e−, 81.5 μV/e−</td>
</tr>
<tr>
<td>Dark noise</td>
<td>2.13 LSB10, 34e− in global shutter 1.42 LSB10, 23e− in rolling shutter</td>
</tr>
<tr>
<td>Responsivity at 550 nm</td>
<td>18 LSB10 /nJ/cm², 3.4 V/lux.s</td>
</tr>
<tr>
<td>Parasitic Light Sensitivity (PLS)</td>
<td>&lt;1/900 at 550 nm</td>
</tr>
<tr>
<td>Full well charge</td>
<td>22000 e−</td>
</tr>
<tr>
<td>Quantum efficiency (GE) x FF</td>
<td>50% at 550 nm</td>
</tr>
<tr>
<td>Pixel FPN</td>
<td>0.5% of RMS of maximum swing rolling shutter: 1.0 LSB10 global shutter: 2.0 LSB10</td>
</tr>
<tr>
<td>Row FPN</td>
<td>rolling &amp; global shutter: 0.2 LSB10</td>
</tr>
<tr>
<td>Column FPN</td>
<td>rolling &amp; global shutter: 1.0 LSB10</td>
</tr>
<tr>
<td>Dynamic range</td>
<td>56.2 dB in global shutter mode 59.6 dB in rolling shutter mode</td>
</tr>
<tr>
<td>Signal-to-Noise Ratio (SNR)</td>
<td>43.4 dB in global and rolling shutter mode</td>
</tr>
<tr>
<td>Dark signal</td>
<td>14 e−/s, 0.9 LSB10/s at +30°C</td>
</tr>
</tbody>
</table>

Recommended Operating Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Description</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>TJ</td>
<td>Operating temperature range</td>
<td>−40</td>
<td>+85</td>
<td>°C</td>
</tr>
</tbody>
</table>

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Min</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABS (1.0 V supply)</td>
<td>ABS rating for 1.0 V supply</td>
<td>−0.5</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>ABS (1.8 V supply group)</td>
<td>ABS rating for 1.8 V supply group</td>
<td>−0.5</td>
<td>2.2</td>
<td>V</td>
</tr>
<tr>
<td>ABS (3.3 V supply group)</td>
<td>ABS rating for 3.3 V supply group</td>
<td>−0.5</td>
<td>4.3</td>
<td>V</td>
</tr>
<tr>
<td>ABS (4.2 V supply)</td>
<td>ABS rating for 4.2 V supply</td>
<td>−0.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>ABS (4.5 V supply)</td>
<td>ABS rating for 4.5 V supply</td>
<td>−0.5</td>
<td>5.0</td>
<td>V</td>
</tr>
<tr>
<td>Tj (Notes 3 and 4)</td>
<td>ABS storage temperature range</td>
<td>0</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>ABS storage humidity range at 85°C</td>
<td>85</td>
<td>%RH</td>
<td></td>
</tr>
<tr>
<td>Electrostatic discharge (ESD) (Notes 2 and 3)</td>
<td>Human Body Model (HBM): JS−001–2010</td>
<td>2000</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Charged Device Model (CDM): JESD22–C101</td>
<td>500</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LU</td>
<td>Latch-up: JESD−78</td>
<td>140</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The ADC is 11-bit, down-scaled to 10-bit. The VITA 25K uses a larger word-length internally to provide 10-bit on the output.
2. Operating ratings are conditions in which operation of the device is intended to be functional.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561. Long term exposure toward the maximum storage temperature will accelerate color filter degradation.
4. Caution needs to be taken to avoid dried stains on the underside of the glass due to condensation. The glass lid glue is permeable and can absorb moisture if the sensor is placed in a high % RH environment.
Electrical Specifications

Power Supply Ratings

Table 5. POWER SUPPLY RATINGS
Limits in bold apply for for T_J = T_MIN to T_MAX, all other limits T_J = +30°C [5], [6], [7], [8]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Parameters</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>vdda_33</td>
<td>Analog supply - 3.3 V domain. gnda_33 is connected to substrate</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>ldda_33</td>
<td>Current consumption from analog supply</td>
<td>675</td>
<td>725</td>
<td>775</td>
<td>mA</td>
</tr>
<tr>
<td>vdddd_33</td>
<td>Digital supply - 3.3 V domain. gndd_33 is connected to substrate</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>lddd_33</td>
<td>Current consumption from 3.3 V digital supply</td>
<td>65</td>
<td>85</td>
<td>105</td>
<td>mA</td>
</tr>
<tr>
<td>vdd_18</td>
<td>Digital supply - 1.8 V domain. gndn_18 is connected to substrate</td>
<td>1.6</td>
<td>1.8</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>ldd_18</td>
<td>Current consumption 1.8 V digital supply</td>
<td>240</td>
<td>310</td>
<td>380</td>
<td>mA</td>
</tr>
<tr>
<td>vdd_pix</td>
<td>Pixel array supply</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>ldd_pix</td>
<td>Current consumption from pixel supply</td>
<td>25</td>
<td>35</td>
<td>45</td>
<td>mA</td>
</tr>
<tr>
<td>vdd_resfd</td>
<td>Floating diffusion reset supply</td>
<td>3.3</td>
<td>4.5</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>gnd_resfd</td>
<td>Floating diffusion reset ground. Not connected to substrate</td>
<td>0</td>
<td>0</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>vdd_respd</td>
<td>Photo diode reset supply</td>
<td>3.3</td>
<td>4.2</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>gnd_respd</td>
<td>Photo diode reset ground. Not connected to substrate.</td>
<td>0</td>
<td>0</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>vdd_trans</td>
<td>Pixel transfer supply</td>
<td>3.3</td>
<td>4.2</td>
<td>4.6</td>
<td>V</td>
</tr>
<tr>
<td>gnd_trans</td>
<td>Pixel transfer ground. Not connected to substrate</td>
<td>0</td>
<td>0</td>
<td>1.0</td>
<td>V</td>
</tr>
<tr>
<td>vdd_sel</td>
<td>Pixel select supply</td>
<td>3.0</td>
<td>3.3</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>gnd_sel</td>
<td>Pixel select ground. Not connected to substrate</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>V</td>
</tr>
<tr>
<td>vdd_casc</td>
<td>Cascode supply</td>
<td>0.9</td>
<td>1.0</td>
<td>1.1</td>
<td>V</td>
</tr>
<tr>
<td>vref_colmux</td>
<td>Column multiplexer reference supply</td>
<td>–</td>
<td>1.0</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>gnd_colbias</td>
<td>Column biasing ground. Dedicated ground signal for pixel biasing. Connected to substrate</td>
<td>–</td>
<td>0</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>gnd_colpc</td>
<td>Column precharge ground. Dedicated ground signal for pixel biasing. Not connected to substrate</td>
<td>–</td>
<td>0</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Ptot</td>
<td>Total power consumption</td>
<td>3000</td>
<td>3400</td>
<td>3800</td>
<td>mW</td>
</tr>
<tr>
<td>Pstby</td>
<td>Power consumption in standby mode</td>
<td>–</td>
<td>–</td>
<td>50</td>
<td>mW</td>
</tr>
<tr>
<td>Popt</td>
<td>Power consumption at lower pixel rates</td>
<td></td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

I/O - LVDS (EIA/TIA-644): Conforming to standard/additional specifications and deviations listed

<table>
<thead>
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<th>Parameter</th>
<th>Description</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>fserdata</td>
<td>Data rate on data channels in 10-bit mode DDR signaling - 32 data channels, 1 synchronization channel</td>
<td>620</td>
</tr>
<tr>
<td>fserdata</td>
<td>Data rate on data channels in 8-bit mode DDR signaling - 32 data channels, 1 synchronization channel</td>
<td>496</td>
</tr>
<tr>
<td>fserclock</td>
<td>Clock rate of output clock in 10-bit mode Clock output for mesochronous signaling</td>
<td>310</td>
</tr>
<tr>
<td>fserclock</td>
<td>Clock rate of output clock in 8-bit mode Clock output for mesochronous signaling</td>
<td>248</td>
</tr>
<tr>
<td>Vicm</td>
<td>LVDS input common mode level</td>
<td>0.3</td>
</tr>
<tr>
<td>Tccsk</td>
<td>Channel to channel skew (training pattern allows per-channel skew correction)</td>
<td>50</td>
</tr>
</tbody>
</table>

LVDS Electrical/Interface

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>fin</td>
<td>Input clock rate for 10-bit mode</td>
<td>310</td>
</tr>
<tr>
<td>fin</td>
<td>Input clock rate for 8-bit mode</td>
<td>248</td>
</tr>
</tbody>
</table>
Table 5. POWER SUPPLY RATINGS
Limits in bold apply for for $T_J = T_{MIN}$ to $T_{MAX}$; all other limits $T_J = +30^\circ C$ [5], [6], [7], [8]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tidc</td>
<td>Input clock duty cycle</td>
<td>40</td>
<td>50</td>
<td>60</td>
<td>%</td>
</tr>
<tr>
<td>tj</td>
<td>Input clock jitter</td>
<td>20</td>
<td></td>
<td></td>
<td>ps</td>
</tr>
<tr>
<td>fspi</td>
<td>SPI clock rate</td>
<td></td>
<td>10</td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>ratspi</td>
<td>10-bit: ratio: $F_{in}/f_{spi}$</td>
<td>30</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8-bit: ratio: $F_{in}/f_{spi}$</td>
<td></td>
<td>24</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Sensor Requirements**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>fps</td>
<td>Frame rate at full resolution (global shutter)</td>
<td>53</td>
<td></td>
<td></td>
<td>fps</td>
</tr>
<tr>
<td>fps_roi1</td>
<td>$X_{res} \times Y_{res} = 1920 \times 1080$</td>
<td>440</td>
<td></td>
<td></td>
<td>fps</td>
</tr>
<tr>
<td>fps_roi2</td>
<td>$X_{res} \times Y_{res} = 1024 \times 1024$</td>
<td>590</td>
<td></td>
<td></td>
<td>fps</td>
</tr>
<tr>
<td>fps_roi3</td>
<td>$X_{res} \times Y_{res} = 640 \times 480$</td>
<td>1380</td>
<td></td>
<td></td>
<td>fps</td>
</tr>
<tr>
<td>fps_roi4</td>
<td>$X_{res} \times Y_{res} = 512 \times 512$</td>
<td>1360</td>
<td></td>
<td></td>
<td>fps</td>
</tr>
<tr>
<td>fps_roi5</td>
<td>$X_{res} \times Y_{res} = 256 \times 256$</td>
<td>2750</td>
<td></td>
<td></td>
<td>fps</td>
</tr>
<tr>
<td>FOT</td>
<td>Frame overhead time</td>
<td>50</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>ROT</td>
<td>Row overhead time</td>
<td>1</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>fpix</td>
<td>Pixel rate (32 channels at 62 Mpix/s)</td>
<td>1984</td>
<td></td>
<td></td>
<td>Mpix/s</td>
</tr>
</tbody>
</table>

5. All parameters are characterized for DC conditions after thermal equilibrium is established.
6. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high-impedance circuit.
7. Minimum and maximum limits are guaranteed through test and design.
8. $V_{ref\_colmux}$ supply should be able to source and sink current

**Disclaimer:** Image sensor products and specifications are subject to change without notice. Products are warranted to meet the production data sheet and acceptance criteria specifications only.
Power Distribution Network

A power distribution network (PDN) is designed to ensure proper power management to the VITA 25K sensor. Table 6 provides the recommended power supplies for the VITA 25K power management. Please refer to the AN65466 for recommended linear regulator selection, decoupling capacitor network and BOM for the power distribution network.

Table 6. RECOMMENDED POWER SUPPLIES FOR VITA 25K

<table>
<thead>
<tr>
<th>Category</th>
<th>Power Supply</th>
<th>Source/Sink Stage</th>
<th>Min Rating (V)</th>
<th>Typ Rating (V)</th>
<th>Max Rating (V)</th>
<th>Max DC Current (mA)</th>
<th>Peak Currents at Allowable pk–pk Ripples</th>
</tr>
</thead>
<tbody>
<tr>
<td>Digital</td>
<td>VDDD_18</td>
<td>Sourcing</td>
<td>1.6</td>
<td>1.8</td>
<td>2</td>
<td>380</td>
<td>2 A at 200 mV</td>
</tr>
<tr>
<td></td>
<td>VDDD_33</td>
<td>Sourcing</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>105</td>
<td>0.6 A at 200 mV</td>
</tr>
<tr>
<td></td>
<td>VDD_sel</td>
<td>Sourcing</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>0</td>
<td>1 mA at 20 mV</td>
</tr>
<tr>
<td>Analog</td>
<td>VDDA_33</td>
<td>Sourcing</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>775</td>
<td>1.5 A at 50 mV</td>
</tr>
<tr>
<td></td>
<td>VDD_pix</td>
<td>Sourcing</td>
<td>3</td>
<td>3.3</td>
<td>3.6</td>
<td>45</td>
<td>700 mA at 100 mV</td>
</tr>
<tr>
<td></td>
<td>VDD_respd</td>
<td>Sourcing</td>
<td>3.3</td>
<td>4.2</td>
<td>4.6</td>
<td>7</td>
<td>300 mA at 20 mV</td>
</tr>
<tr>
<td></td>
<td>VDD_trans</td>
<td>Sourcing</td>
<td>3.3</td>
<td>4.2</td>
<td>4.6</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VDD_resfd</td>
<td>Sourcing</td>
<td>3.3</td>
<td>4.5</td>
<td>4.6</td>
<td>7</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VDD_casc</td>
<td>Sourcing</td>
<td>0.9</td>
<td>1</td>
<td>1.1</td>
<td>0</td>
<td>6 mA at 300 mV</td>
</tr>
<tr>
<td></td>
<td>Vref_colmux</td>
<td>Sourcing &amp; Sinking</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0.35 A at 0.5 mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td>gnd_respd</td>
<td>Sinking</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>30 mA sinking at 0.4 V</td>
<td>200 mA at 20 mV</td>
</tr>
</tbody>
</table>

9. Combining power supplies:
- VDD_sel can be combined with either VDDD_33 or VDDA_33
- VDD_respd and VDD_trans can be grouped together as VDD_42
- gnd_respd is be designed to be a 7 mA sinking supply, but can be tied to ground with no impact to image quality

Color Filter Array

The VITA 25K color sensor is processed with a Bayer RGB color pattern as shown in Figure 2. Pixel (0,0) has a red filter situated to the bottom left. Green1 and green2 have a slightly different spectral response due to (optical) cross talk from neighboring pixels. Green1 pixels are located on a green-red row, green2 pixels are located on a blue-green row.

Figure 3 depicts the spectral response for the mono and color devices. Figure 4 shows the photovoltaic response for the VITA 25K.

Figure 2. Color Filter Array for the Pixel Array
Figure 3. Mono and Color Spectral Response with Micro Lens

Note that green pixels on a Green–Red (Green 1) and Green–Blue (Green 2) row have similar responsivity to wavelength trend as is depicted by the legend “Green”.

Figure 4. Typical Photovoltaic Response
Figure 5 gives an overview of all functional blocks in the image sensor. The system clock is received by the LVDS clock receiver block and distributed to other blocks. The sequencer defines the sensor timing and controls the image core. The sequencer is started either autonomously (master mode) or on assertion of an external trigger (slave mode). The image core contains all pixels and readout circuits. The column structure selects pixels for readout and performs correlated double sampling (CDS) or double sampling (DS). The data comes out sequentially and is fed into the analog front end (AFE) block. The programmable gain amplifier (PGA) of the AFE adds the offset and gain. The output is a fully differential analog signal that goes to the ADC, where the analog signal is converted to a 10-bit data stream.

Depending on the operating mode, eight or ten bits are fed into the data formatting block. This block adds synchronization information to the data stream based on the frame timing. The data then goes to the low voltage serial (LVDS) interface block that sends the data out through the I/O ring.

On-chip programmability is controlled through the Serial Peripheral Interface (SPI). See Register Map on page 43 for register details. A bias block generates bias currents and voltages for all analog blocks on the chip. By controlling the bias current, the speed-versus-power of each block can be tuned. All biasing programmability is contained in the bias block.

The pixel array contains 5120 x 5120 readable pixels with a pixel pitch of 4.5 μm. Four dummy pixel rows and columns are placed at every side of the pixel array to eliminate possible edge effects. The sensor uses a 5T pixel architecture, which makes it possible to read out the pixel...
array in global shutter mode with DS, or rolling shutter mode with CDS.

The function of the row drivers is to access the image array line by line, or all lines together, to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array in global and rolling shutter modes.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

**Figure 6. Image Core Diagram**

**LVDS Clock Receiver**

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 310 MHz in 10-bit mode and 248 MHz in 8-bit mode. The clock input needs to be terminated with a 100 Ω resistor.

**Column Multiplexer**

The 5120 pixels of one image row are stored in 5120 column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 64 parallel differential outputs operating at a frequency of 31 MHz.

At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal. A programmable gain of 1x, 2x, or 4x can be applied to the signal at this stage. The column multiplexer also supports a subsampled readout mode (read-1-skip-1 for mono and read-2-skip-2 for color version). Enabling this mode can speed up the frame rate, with a decrease in resolution.

**Bias Generator**

The bias generator generates all required reference voltages and bias currents that the on-chip blocks use. An external resistor of 47 kΩ, connected between the pins ibias_master and gnda_33 is required for the bias generator to operate properly.

**Analog Front End**

The AFE contains 64 channels, each containing a PGA and a 10-bit ADC. The PGA can be programmed to apply a gain of 1x, 1.39x, 1.94x, and 2.72x to the image signal. Together with the gain applied in the column multiplexer, a total signal gain of 10x can be achieved.

For each of the 64 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

**Data Formatting**

The data block receives data from two ADCs and multiplexes this data to one LVDS block. A cyclic redundancy check (CRC) code is calculated on the passing data. For each LVDS output channel, one data block is instantiated. An extra data block is foreseen to transmit synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

**Serializer and LVDS Interface**

The serializer and LVDS interface block receives the formatted (10-bit or 8-bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10-bit mode, the maximum output data bit rate is 620 Mbps per channel. In 8-bit mode, the maximum output data bit rate is 496 Mbps per channel.

In addition to the 32 LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

**Sequencer**

The sequencer is responsible for the following tasks:

- Controls the image core. Starts and stops integration in rolling and global shutter modes and control pixel readout.
- Operates the sensor in master or slave mode.
- Applies the window settings. Organizes readouts so that only the configured windows are read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.
OPERATING MODES

This sensor supports multiple operation modes. The following list provides an overview.

- Global Shutter mode
  - Pipelined global shutter mode
    - Master mode
    - Slave mode
  - Triggered global shutter
    - Master mode
    - Slave mode
- Rolling shutter mode
- Multiple windowing readout
  - Flexible window configuration
  - Processing multiple windows in Global Shutter mode
- Subsampling and binning
  - Pixel binning
  - Subsampling

**Global Shutter Mode**

In a global shutter mode, light integration takes place on all pixels in sync, although subsequent readout is sequential, as shown in Figure 7. Figure 8 shows the integration and readout sequence for the global shutter. All pixels are light sensitive at the same time. The whole pixel core is reset simultaneously and, after the integration time, all pixel values are sampled together on the storage node inside each pixel. The pixel core is read out line by line after integration. The integration and readout can occur in parallel or sequentially.

The integration starts at a certain period, relative to the frame start.

**Pipelined Global Shutter Mode**

In pipelined shutter mode, the integration and readout are done in parallel. Images are continuously read and integration of frame N is ongoing during readout of the previous frame N–1. The readout of every frame starts with a frame overhead time (FOT), during which the analog value on the pixel diode is transferred to the pixel memory element. After the FOT, the sensor is read out line by line and the readout of each line is preceded by the row overhead time (ROT).

![Figure 7. Global Shutter Operation](image)

**Master Mode**

In this operation mode, the integration time is set through the register interface and the sensor integrates and reads out the images autonomously. The sensor acquires images without any user interaction.

**Slave Mode**

The slave mode adds more manual control to the sensor. The integration time registers are ignored in this mode and the integration time is instead controlled by an external pin. As soon as the control pin is asserted, the pixel array goes out of reset and integration starts. The integration continues until the user or system deasserts the external pin. Upon a falling edge of the trigger input, the image is sampled and the readout begins.
Triggereed Global Shutter
In this mode, manual intervention is required to control both the integration time and the start of readout. After the integration time, indicated by a user controlled pin, the image core is read out. After this sequence, the sensor goes to an idle mode until a new user action is detected.

The three main differences from the pipelined shutter master mode are:
- Upon user action, a single image is read.
- Normally, integration and readout are done sequentially. However, the user can control the sensor in such a way that two consecutive batches are overlapping, that is, having concurrent integration and readout.
- Integration and readout is user-controlled through an external pin.

The triggered global mode can also be controlled in a master or in a slave mode.

Master Mode
As shown in Figure 10, in the master mode a rising edge on the synchronization pin is used to trigger the start of integration and readout. The integration time is defined by a register setting. The sensor autonomously integrates during this predefined time, after which the FOT starts and the image array is read out sequentially. A falling edge on the synchronization pin does not have any impact on the readout or integration and subsequent frames are started again for each rising edge.

Slave Mode
Integration time control is identical to the pipelined shutter slave mode, in which both integration time and readout requests are controlled by an external trigger. An external synchronization pin controls the start of integration. The moment it is deasserted, the FOT starts. At this time, the analog value on the pixel diode is transferred to the pixel memory element and the image readout can start. A request for a new frame is started when the synchronization pin is asserted again.
Rolling Shutter Mode

The sensor also supports the rolling shutter mode. The shutter mechanism is an electronic rolling shutter and the sensor operates in streaming mode similar to a video. This mechanism is controlled by the on-chip sequencer logic. There are two Y pointers, as indicated in Figure 11. One of them points to the row that is to be reset for rolling shutter operation and the other points to the row to be read out. Functionally, a row is reset first and selected for readout later. The time elapsed between these two operations is the exposure time.

Figure 11 schematically indicates the relative shift of the integration times of different lines during rolling shutter operation. Each row is read and reset sequentially, as described in the previous paragraph. Each row in a particular frame is integrated for the same time, but all lines in a frame ‘see’ a different stare time. Therefore, fast horizontal moving objects in the field of view give rise to motion artifacts in the image; this is an unavoidable property of a rolling shutter.

In rolling shutter mode, a second pointer indicates the rows that need to be reset for the rolling shutter mechanism. The distance between the reset pointer and the readout pointer determines the integration time.

The VITA 25K supports dynamic exposure time updates without artifacts or interrupting the image data stream.
Operation Flowchart

Figure 12 shows the flow chart diagram of the sensor operation. The sensor can be in five different ‘states’. Every state is indicated with the oval circle. These states are:

- Power-Off
- Standby (1)
- Standby (2)
- Idle
- Running

The states above are ordered by power dissipation. Clearly, in ‘power-off’ state the power dissipation will be minimal; in ‘running’ state the power dissipation will be maximal.

On the other hand, the lower the power consumption, the more actions (and time) are required to put the sensor in ‘running’ state and grabbing images.

This flowchart provides the trade-offs between power saving and enabling time of the sensor.

Next to the ‘states’ a set of ‘user actions’, indicated by arrows, are included in the flow chart diagram. These user actions make it possible to move from one state to another.
The sensor can be in five different states:

**Power-off**
In this state, the sensor is inactive. All power supplies are down and the power dissipation is zero.

**Standby (1)**
The registers below address 40 can be configured.

**Standby (2)**
In this standby state all SPI registers are active, meaning that all SPI registers can be accessed for read and write operations. All other blocks are disabled.

Note: An Intermediate Standby state is traversed after a hard reset. In this state the sensor contains the default configurations. Uploads of reserved registers are required to traverse to the Standby (2) state.

**Idle**
In the idle state, all sensor clocks are running and all blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

**Running**
In running state, the sensor is enabled and grabbing images. The sensor can be operated in different rolling/global master/slave modes.

**User Actions: Functional Mode to Power Up Sequences**
To ‘travel’ between the five possible states, a set of actions is defined. Except for the power-up and power-down sequences, all actions consist of a set of SPI uploads.

The “Sensor reconfiguration actions” indicated in Figure 12 are used to reconfigure the operation modes of the sensor. The sensor state itself is not altered.

**Power-up Sequence**
Figure 13 shows the power-up timing of the sensor. Apply all power supplies in the order shown in the figure. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

When all the supplies are stable, enable the sensor clock signal; then deassert the reset_n signal. After leaving the hard-reset mode, the sensor enters the standby (1) state. To go to the standby (2) mode, the sensor requires the reconfiguration of some registers. This reconfiguration can be applied 10 µs after the hard reset is released.

### Table 7. CLOCK FREQUENCY OVERVIEW

<table>
<thead>
<tr>
<th>Parameter</th>
<th>8-bit Mode</th>
<th>10-bit Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Clock Frequency</td>
<td>248 MHz</td>
<td>310 MHz</td>
</tr>
</tbody>
</table>

Enable Clock Management
The next step consists of SPI uploads which configures the internal clock distribution. The required uploads are listed in Table 8. It is important to follow the upload sequence as listed.

### Table 8. ENABLE CLOCK MANAGEMENT UPLOAD

<table>
<thead>
<tr>
<th>No.</th>
<th>Address</th>
<th>Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>2</td>
<td>0x0000</td>
<td>NOIV1SN025KA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x0001</td>
<td>NOIV1SE025KA</td>
</tr>
<tr>
<td>2</td>
<td>32</td>
<td>0x2002</td>
<td>Configure Clock Management</td>
</tr>
<tr>
<td>3</td>
<td>34</td>
<td>0x0001</td>
<td>Enable Logic Blocks</td>
</tr>
</tbody>
</table>
Required Register Uploads

In this phase the ‘reserved’ register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 9.

Table 9. REQUIRED REGISTER UPLOADS

<table>
<thead>
<tr>
<th>No.</th>
<th>Address</th>
<th>Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>65</td>
<td>0x008B</td>
<td>General Biasing</td>
</tr>
<tr>
<td>2</td>
<td>66</td>
<td>0x53C6</td>
<td>AFE Biasing</td>
</tr>
<tr>
<td>3</td>
<td>67</td>
<td>0x0844</td>
<td>Mux Biasing</td>
</tr>
<tr>
<td>4</td>
<td>68</td>
<td>0x0086</td>
<td>LVDS Biasing</td>
</tr>
<tr>
<td>5</td>
<td>128</td>
<td>0x4520</td>
<td>Set desired output level to code 32 for 10-bit mode, code 8 for 8-bit mode. Set number of samples for black calibration to $2^5$.</td>
</tr>
<tr>
<td>6</td>
<td>204</td>
<td>0x09E5</td>
<td>Configure unity gain</td>
</tr>
<tr>
<td>7</td>
<td>224</td>
<td>0x3E04</td>
<td>Dummy rows upon integration start</td>
</tr>
<tr>
<td>8</td>
<td>225</td>
<td>0x6733</td>
<td>Configure internal latency</td>
</tr>
<tr>
<td>9</td>
<td>129[13]</td>
<td>0x0</td>
<td>10-bit Mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0x1</td>
<td>8-bit Mode</td>
</tr>
<tr>
<td>10</td>
<td>447</td>
<td>0x0BF1</td>
<td>Configure sequencer</td>
</tr>
<tr>
<td>11</td>
<td>448</td>
<td>0x0BC3</td>
<td>Configure sequencer</td>
</tr>
</tbody>
</table>

Soft Power Up

During the soft power-up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power-up uploads are listed in Table 10.

Table 10. SOFT POWER UP REGISTER UPLOADS

<table>
<thead>
<tr>
<th>No.</th>
<th>Address</th>
<th>Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>32</td>
<td>0x2003</td>
<td>Enable Analog Clock Distribution</td>
</tr>
<tr>
<td>2</td>
<td>64</td>
<td>0x0001</td>
<td>Enable Biasing Block</td>
</tr>
<tr>
<td>3</td>
<td>40</td>
<td>0x0003</td>
<td>Enable Column Multiplexer</td>
</tr>
<tr>
<td>4</td>
<td>48</td>
<td>0x0001</td>
<td>Enable Analog Front-End (AFE)</td>
</tr>
<tr>
<td>5</td>
<td>112</td>
<td>0x0007</td>
<td>Enable LVDS Transmitters</td>
</tr>
</tbody>
</table>

Enable Sequencer

During the ‘Enable Sequencer’-action, the frame grabbing sequencer is enabled. The sensor will start grabbing images in the configured operation mode. Refer to Operating Modes on page 11 for an overview of the possible operation modes.

The ‘Enable Sequencer’ action consists of a set of register uploads. The required uploads are listed in Table 11.

Table 11. ENABLE SEQUENCER REGISTER UPLOADS

<table>
<thead>
<tr>
<th>No.</th>
<th>Address</th>
<th>Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>192[0]</td>
<td>0x1</td>
<td>Set ‘reg_seq_enable’ to ‘1’. All other configuration bits of register 192 should remain unchanged.</td>
</tr>
</tbody>
</table>

User Actions: Functional Mode to Power Down Sequences

Disable Sequencer

During the ‘Disable Sequencer’-action, the frame grabbing sequencer is stopped. The sensor will stop grabbing images and returns to the idle mode.

The ‘Disable Sequencer’ action consists of a set of register uploads. The required uploads are listed in Table 12.

Table 12. DISABLE SEQUENCER REGISTER UPLOADS

<table>
<thead>
<tr>
<th>No.</th>
<th>Address</th>
<th>Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>192[0]</td>
<td>0x0</td>
<td>Disable of Sequencer. NOTE: This address contains other configuration bits to select the operation mode.</td>
</tr>
</tbody>
</table>

Soft Power Down

During the soft power-down action, the internal blocks are disabled and the sensor is put in standby state in order to reduce the current dissipation. This action exists of a set of register uploads. The soft power-down uploads are listed in Table 13.

Table 13. SOFT POWER DOWN REGISTER UPLOADS

<table>
<thead>
<tr>
<th>No.</th>
<th>Address</th>
<th>Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>112</td>
<td>0x0000</td>
<td>Disable LVDS Transmitters</td>
</tr>
<tr>
<td>2</td>
<td>48</td>
<td>0x0000</td>
<td>Disable Analog Front-End (AFE)</td>
</tr>
<tr>
<td>3</td>
<td>40</td>
<td>0x0000</td>
<td>Disable Column Multiplexer</td>
</tr>
<tr>
<td>4</td>
<td>64</td>
<td>0x0000</td>
<td>Disable Biasing Block</td>
</tr>
<tr>
<td>5</td>
<td>32</td>
<td>0x2002</td>
<td>Disable Analog Clock Distribution</td>
</tr>
</tbody>
</table>

Disable Clock Management

The ‘Disable Clock Management’-action stops the internal clocking in order to further decrease the power dissipation. This action exists of a set of register uploads as listed in Table 14.

Table 14. DISABLE CLOCK MANAGEMENT UPLOADS

<table>
<thead>
<tr>
<th>No.</th>
<th>Address</th>
<th>Data</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>34</td>
<td>0x0000</td>
<td>Disable Logic Blocks</td>
</tr>
</tbody>
</table>
Power-down Sequence

The timing diagram of the advised power-down sequence is given in Figure 14. Any other sequence might cause high peak currents.

NOTE: vdd_case should be powered down after vdd_respd, vdd_resfd, and vdd_trans.

![Timing diagram of power-down sequence](image)

**Figure 14. Power-down Sequence**

Shutter and Operation Mode Reconfiguration

The VITA 25K sensor operates in two shutter modes: global shutter and rolling shutter. The global shutter mode can be combined with a set of operation modes, as described Operation Modes on page 11.

These modes can be combined with subsampling and binning modes.

The shutter and operation modes are controlled by register 192, when the sensor is in standby or idle mode. Table 15 gives an overview of the available register settings to control the shutter and operation modes. During this action, only the fields listed in Table 15 are affected. All other settings encapsulated in register 192 must remain unchanged.

<table>
<thead>
<tr>
<th>Address</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>192 [1]</td>
<td>0x0</td>
<td>Shutter type selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Global shutter</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Rolling shutter</td>
</tr>
<tr>
<td>192 [4]</td>
<td>0x0</td>
<td>Triggered mode selection (global shutter only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Normal mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Triggered mode</td>
</tr>
<tr>
<td>192 [5]</td>
<td>0x0</td>
<td>Master/Slave selection (global shutter only)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Master mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Slave mode</td>
</tr>
<tr>
<td>192 [7]</td>
<td>0x0</td>
<td>Subsampling mode selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Subsampling disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Subsampling enabled</td>
</tr>
<tr>
<td>192 [8]</td>
<td>0x0</td>
<td>Binning mode selection</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0: Binning disabled</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1: Binning enabled</td>
</tr>
</tbody>
</table>

Windowing Reconfiguration

The windowing settings can be configured during standby, idle, and running mode.

The required regions of interest (ROI) can be programmed in the roi_configuration registers (addresses 256 up to 351). Registers roi_active0 and roi_active1 are used to activate the desired ROIs.

Default window configuration (after sensor reset) is one window, full frame (window #0).

Exposure/Gain Reconfiguration

The exposure time and gain settings can be configured during standby, idle, and running mode. Refer to Signal Gain Path on page 29 for more information.
Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 16. Table 16 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 16. STATIC READOUT PARAMETERS

<table>
<thead>
<tr>
<th>Group</th>
<th>Addresses</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock generator</td>
<td>32</td>
<td>Configure according to recommendation</td>
</tr>
<tr>
<td>Image core</td>
<td>40</td>
<td>Configure according to recommendation</td>
</tr>
<tr>
<td>AFE</td>
<td>48</td>
<td>Configure according to recommendation</td>
</tr>
<tr>
<td>Bias</td>
<td>64–71</td>
<td>Configure according to recommendation</td>
</tr>
<tr>
<td>LVDS</td>
<td>112</td>
<td>Configure according to recommendation</td>
</tr>
<tr>
<td>Sequencer mode selection</td>
<td>192</td>
<td>• Rolling shutter enable</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• triggered_mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• slave_mode</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• nzrot_xsm_delay_enable</td>
</tr>
<tr>
<td>All reserved registers</td>
<td></td>
<td>Keep reserved registers to their default state, unless otherwise described in the recommendation</td>
</tr>
</tbody>
</table>

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 17 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the reconfiguration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed. The effect is transient in nature and the new configuration is applied after the transient effect.

Table 17. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

<table>
<thead>
<tr>
<th>Group</th>
<th>Addresses</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Black level configuration</td>
<td>128–129</td>
<td>Reconfiguration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.</td>
</tr>
<tr>
<td></td>
<td>197[8]</td>
<td></td>
</tr>
<tr>
<td>Sync codes</td>
<td>129[13]</td>
<td>Incorrect sync codes may be generated during the frame in which these registers are modified.</td>
</tr>
<tr>
<td></td>
<td>130–135</td>
<td></td>
</tr>
<tr>
<td>Datablock test configurations</td>
<td>144–150</td>
<td>Modification of these registers may generate incorrect test patterns during a transient frame.</td>
</tr>
</tbody>
</table>

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame-related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 18.

Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.
Table 18. DYNAMIC READOUT PARAMETERS

<table>
<thead>
<tr>
<th>Group</th>
<th>Addresses</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Subsampling/binning</td>
<td>192[7]</td>
<td>Subsampling or binning is synchronized to a new frame start.</td>
</tr>
<tr>
<td></td>
<td>192[8]</td>
<td></td>
</tr>
<tr>
<td>Black lines</td>
<td>197</td>
<td>Reconfiguration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. No blanking in global shutter mode.</td>
</tr>
<tr>
<td>Dummy lines</td>
<td>198</td>
<td>Reconfiguration of these parameters causes one frame to be blanked out in rolling shutter operation mode, as the reset pointers need to be recalculated for the new frame timing. N/A for global shutter mode.</td>
</tr>
<tr>
<td>ROI configuration</td>
<td>195-196</td>
<td>Optionally, it is possible to blank out one frame after reconfiguration of the active ROIs in rolling shutter mode. Therefore, register 206[8] must be asserted (blank_roi_switch configuration). An ROI switch is only detected when a new window is selected as the active window (reconfiguration of registers 195, 196, or both). Reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image.</td>
</tr>
<tr>
<td></td>
<td>256–351</td>
<td></td>
</tr>
<tr>
<td>Exposure reconfiguration</td>
<td>199-201</td>
<td>Exposure reconfiguration does not cause artifact. However, a latency of one frame is observed unless reg_seq_exposure_sync_mode is set to ‘1’ in triggered global mode (master).</td>
</tr>
<tr>
<td>Gain reconfiguration</td>
<td>204</td>
<td>Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 204[13] - gain_lat_comp).</td>
</tr>
</tbody>
</table>

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure the exposure time in master global mode, both the fr_length and exposure registers need to be updated. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re-enable the synchronization. The sensor’s sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 15 shows a reconfiguration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

With sync_configuration = ‘1’. Configurations are synchronized to the frame boundaries (The registers exposure, fr_length, and mult_timer are not used in this mode)

Figure 16 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is deasserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries. As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

Figure 15. Frame Synchronization of Configurations (no freezing)
NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 19 lists the several sync_configuration possibilities along with the respective registers being frozen.

### Table 19. ALTERNATE SYNC CONFIGURATIONS

<table>
<thead>
<tr>
<th>Group</th>
<th>Affected Registers</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>sync_rs_x_length</td>
<td>rs_x_length</td>
<td>Update of x-length configuration (rolling shutter only) is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.</td>
</tr>
<tr>
<td>sync_black_lines</td>
<td>black_lines</td>
<td>Update of black line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.</td>
</tr>
<tr>
<td>sync_dummy_lines</td>
<td>dummy_lines</td>
<td>Update of dummy line configuration is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.</td>
</tr>
<tr>
<td>sync_exposure</td>
<td>mult_timer, fr_length, exposure</td>
<td>Update of exposure configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.</td>
</tr>
<tr>
<td>sync_gain</td>
<td>mux_gainsw, afe_gain</td>
<td>Update of gain configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations.</td>
</tr>
<tr>
<td>sync_roi</td>
<td>roi_active0[15:0], roi_active1[15:0], subsampling, binning</td>
<td>Update of active ROI configurations is not synchronized at start of frame when '0'. The sensor continues with its previous configurations. <strong>Note:</strong> The window configurations themselves are not frozen. Re-configuration of active windows is not gated by this setting.</td>
</tr>
</tbody>
</table>

### Window Configuration

**Global Shutter Mode**

Up to 32 windows can be defined in global shutter mode (pipelined or triggered). The windows are defined by registers 256 to 351. Each window can be activated or deactivated separately using registers 195 and 196. It is possible to reconfigure the inactive windows while acquiring images. Switching between predefined windows is achieved by activation of the respective windows. This way a minimum number of registers need to be uploaded when it is necessary to switch between two or more sets of windows. As an example of this, scanning the scene at higher frame rates using multiple windows and switching to full frame capture when the object is tracked. Switching between the two modes only requires an upload of one (if the total number of windows is smaller than 17) or two (if more than 16 windows are defined) registers.

**Rolling Shutter Mode**

In rolling shutter mode it is not possible to read multiple windows. Do not activate more than one window (registers 205–206). However, it is possible to configure more than one window and dynamically switch between the different window configurations. Note that switching between two different windows might result in a corrupted frame. This is inherent in the rolling shutter mechanism, where each line must be reset sequentially before being read out. This corrupted window can be blanked out by setting register 206[8]. In this case, a dead time is noted on the LVDS interface when the window-switch occurs in the sensor. During this blank out, training patterns are sent out on the data and sync channels for the duration of one frame.

### Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to ‘0’. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to ‘0’ when setting the black level target to ‘0’.

The black level is calibrated for the 64 columns contained in one kernel. This implies 64 black level offsets are generated and applied to the corresponding columns. Configurable parameters for the black-level algorithm are listed in Table 20.
## Table 20. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

<table>
<thead>
<tr>
<th>Group</th>
<th>Addresses</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Black Line Generation</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>197[7:0]</td>
<td>black_lines</td>
<td>This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 255.</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note:</strong> When the automatic black-level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black-level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Global Shutter - Each black line contains 80 kernels.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Rolling Shutter - As the line length is fundamental for rolling shutter operation, the length of a black line is defined by the active window.</td>
</tr>
<tr>
<td>197[8]</td>
<td>gate_first_line</td>
<td>When asserting this configuration, the first black line of the frame is blanked out and is not used for black calibration. It is recommended to enable this functionality, because the first line can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm.</td>
</tr>
<tr>
<td><strong>Black Value Filtering</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>129[0]</td>
<td>auto_blackcal_enable</td>
<td>Internal black-level calibration functionality is enabled when set to ‘1’. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to ‘0’, the automatic black-level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1].</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note:</strong> Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations.</td>
</tr>
<tr>
<td>129[9:1]</td>
<td>blackcal_offset</td>
<td>Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to ‘0’. The sign of the offset is determined by register 129[10] (blackcal_offset_dec).</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note:</strong> All channels use the same offset compensation when automatic black calibration is disabled. The calculated black calibration factors are frozen when this register is set to 0x1FF (all−1) in auto calibration mode. Any value different from 0x1FF re−enables the black calibration algorithm. This freezing option can be used to prevent eventual frame to frame jitter on the black level as the correction factors are recalculated every frame. It is recommended to enable the black calibration regularly to compensate for temperature changes.</td>
</tr>
<tr>
<td>129[10]</td>
<td>blackcal_offset_dec</td>
<td>Sign of blackcal_offset. If set to ‘0’, the black calibration offset is added to each pixel. If set to ‘1’, the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to ‘1’.</td>
</tr>
<tr>
<td>128[10:8]</td>
<td>black_samples</td>
<td>The black samples are low-pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate.</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Note:</strong> An error is reported by the device if more samples than available are requested (refer to registers 136 to 139).</td>
</tr>
<tr>
<td><strong>Black Level Filtering Monitoring</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>136</td>
<td>blackcal_error0</td>
<td>An error is reported by the device if there are requests for more samples than are available (each bit corresponding to one data path). The black level is not compensated correctly if one of the channels indicates an error. There are three possible methods to overcome this situation and to perform a correct offset compensation:</td>
</tr>
<tr>
<td>137</td>
<td>blackcal_error1</td>
<td>• Increase the number of black lines such that enough samples are generated at the cost of increasing frame time (refer to register 197).</td>
</tr>
<tr>
<td>138</td>
<td>blackcal_error2</td>
<td>• Relax the black calibration filtering at the cost of less accurate black level determination (refer to register 128).</td>
</tr>
<tr>
<td>139</td>
<td>blackcal_error3</td>
<td>• Disable automatic black level calibration and provide the offset via SPI register upload. Note that the black level can drift in function of the temperature. It is thus recommended to perform the offset calibration periodically to avoid this drift.</td>
</tr>
</tbody>
</table>

**NOTE:** The maximum number of samples taken into account for black level statistics is half the number of kernels.
Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:
- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor’s system clock. When the master wants to write or read a sensor’s register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 17 shows the communication protocol for read and write accesses of the SPI registers. The VITA 25K sensor uses 9-bit addresses and 16-bit data words.

Data driven by the system is colored blue in Figure 17, while data driven by the sensor is colored yellow. The data in grey indicates high-Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (moso sampling during read operations).

The access sequence is:
1. Select the sensor for read or write by pulling down the ss_n line.
2. One SPI clock cycle (100 ns) after selecting the sensor, the 9-bit address is transferred, most significant bit first. The sck clock is passed through to the sensor as indicated in Figure 17. The sensor samples this data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock).
3. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
4. Data transmission:
   - For write commands, the master continues sending the 16-bit data, most significant bit first.
   - For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
5. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Maximum frequency for the SPI is \(1/30^{th}\) (in 10-bit mode) and \(1/24^{th}\) (in 8-bit mode) of the LVDS input clock frequency. For nominal input frequency (310 MHz / 248 MHz), this is 10 MHz.

Bursts of SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

---

**Figure 17. SPI Read and Write Timing Diagram**
<table>
<thead>
<tr>
<th>Group</th>
<th>Addresses</th>
<th>Description</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>tsck</td>
<td>sck clock period</td>
<td>100 (*)</td>
<td>ns</td>
</tr>
<tr>
<td>tssck</td>
<td>ss_n low to sck rising edge</td>
<td>tsck</td>
<td>ns</td>
</tr>
<tr>
<td>tsckss</td>
<td>sck falling edge to ss_n high</td>
<td>tsck</td>
<td>ns</td>
</tr>
<tr>
<td>ts_mosi</td>
<td>Required setup time for mosi</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>th_mosi</td>
<td>Required hold time for mosi</td>
<td>20</td>
<td>ns</td>
</tr>
<tr>
<td>ts_miso</td>
<td>Setup time for miso</td>
<td>tsck/2-10</td>
<td>ns</td>
</tr>
<tr>
<td>th_miso</td>
<td>Hold time for miso</td>
<td>tsck/2-20</td>
<td>ns</td>
</tr>
<tr>
<td>tspi</td>
<td>Minimal time between two consecutive SPI accesses (not shown in figure)</td>
<td>2 x tsck</td>
<td>ns</td>
</tr>
</tbody>
</table>

*Value indicated is for nominal operation. The maximum SPI clock frequency depends on the sensor configuration (operation mode, input clock). tsck is defined as 1/fSPI. See text for more information on SPI clock frequency restrictions.
GLOBAL SHUTTER MODE

Pipelined Global Mode (Master)

The sensor timing in master global shutter mode is controlled by the user by means of configuration registers. One can distinguish three parameters for the frame timing in global shutter mode:

- Image Array Reset Length
- Integration Time
- Frame Length

The relation between these parameters is:

\[ \text{Frame Length} = \text{Reset Length} + \text{Integration Time} \]

The FOT time needs to be added to the frame length parameter to determine the total frame time:

\[ \text{Total Frame Time} = \text{FOT Time} + \text{Frame Length} \]

Frame and integration time configuration can be controlled in two ways:

1. fr_mode = 0x0
   The reset length and integration time is configured by the user. The sensor shall calculate the frame length as the sum of both parameters.
2. fr_mode = 0x1
   The frame length and integration time is configured by the user. The reset time during which the pixels are reset, is calculated by the sensor as being the difference between the frame length and the desired integration time.

The configuration registers are exposure[15:0] and fr_length[15:0]. The latter configuration registers is either used as Reset Length configuration (fr_mode = 0x0) or as Frame Length (fr_mode = 0x1). The granularity of both registers is defined by the mult_timer[15:0] register and is expressed in number of 62 MHz cycles (16.129 ns nominal).

Reset Length and Integration Time as Parameters

The reset time for the pixel array is controlled by the registers fr_length[15:0] and exposure[15:0]. The mult_timer configuration defines the granularity of the registers fr_length and exposure and is to be read as the number of 62 MHz cycles (16.129 ns nominal).

The exposure control for pipelined global master mode is depicted in Figure 18.

The pixel values are transferred to the storage node during the FOT, after which all photo diodes are reset. The reset state remains active for a certain time, defined by the fr_length and mult_timer registers, as shown in the figure. Meanwhile, the image array is read out line by line. After this reset period, the global photodiode reset condition is abandoned. This indicates the start of the integration or exposure time. The length of the exposure time is defined by the registers exposure and mult_timer.

NOTES:

- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in a reset state is extended to the start of a new line.
- Make sure that the sum of the reset time and exposure time exceeds the time required to read out all lines. If this is not the case, the exposure time is extended until all (active) lines are read out.

Frame Length and Integration Time as Parameters

When fr_mode is configured to 0x1, one configures the frame time and exposure. The reset_length is determined by the sequencer. This configuration mode is depicted in Figure 2.

The frame length is configured in register fr_length, while the integration time is configured in register exposure. The mult_timer register defines granularity of both settings. Note that the FOT needs to be added to the configured fr_length to calculate the total frame time.

Triggered Global Shutter (Master)

In master triggered global mode, the start of integration time is controlled by a rising edge on the trigger pin. The exposure or integration time is defined by the registers exposure and mult_timer, similar to the master pipelined global mode. The fr_length configuration is not used. This operation is graphically shown in Figure 20.

NOTES:

- The falling edge on the trigger pin does not have any impact. However, the trigger must be asserted for at least 100 ns.
- The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in reset state is extended to the start of a new line.
- The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (e.g. use monitor0, indicating the very first line when monitor_select = 0x5 = a new trigger can be initiated after a rising edge on monitor0).

If the exposure timer expires before the end of readout, the exposure time is extended until the end of the last active line.
Figure 18. Integration Control for Pipelined Global Shutter Mode (Master, fr_mode = 0x0)

Figure 19. Integration Control for Pipelined Global Shutter Mode (Master, fr_mode = 0x1)

Figure 20. Exposure Time Control in Triggered Global Mode (Master)

Triggered Global Shutter (Slave)
Exposure or integration time is fully controlled by means of the trigger pin in slave mode. The register’s fr_length, exposure, and mult_timer are ignored by the sensor.
A rising edge on the trigger pin indicates the start of the exposure time, while a falling edge initiates the transfer and readout of the image array. In other words, the high time of the trigger pin indicates the integration time, the period of the trigger pin indicates the frame time.
The use of the trigger during slave mode is shown in Figure 21.
NOTES:
• The start of the exposure time is synchronized to the start of a new line (during ROT) if the exposure period starts during a frame readout. Therefore, the effective time during which the image core is in a reset state is extended to the start of a new line.
• If the trigger is deasserted before the end of readout, the exposure time is extended until the end of the last active line. Consequently the FOT and start of frame readout is postponed accordingly.
• The trigger pin needs to be kept low during the FOT. The monitor pins can be used as a feedback to the FPGA/controller (e.g., use monitor0, indicating the very first line when monitor_select = 0x5 – a new trigger can be initiated after a rising edge on monitor0).
Rolling Shutter Mode

The exposure time during rolling shutter mode is always an integer multiple of line-times. The exposure time is defined by the register exposure and expressed in number of lines. The register fr_length and mult_timer are not used in this mode.

The maximum exposure time is limited by the frame time. It is possible to increase the exposure time at the cost of the frame rate by adding so-called dummy lines. A dummy line lasts for the same time as a regular line, but no pixel data is transferred to the system. The number of dummy lines is controlled by the register dummy_lines.

The rolling shutter exposure mechanism is graphically shown in Figure 22.

The duration of one line is the sum of ROT and the time required to read out one line (depending on the number of active kernels in the window). Optionally, this readout time can be extended by the configuration rs_x_length. This register, expressed in number of periods of the logic clock (16.129 ns nominal), determines the length of the x-readout. However, the minimum length is governed by the window size (x-size).
Multiple Window Readout

The sequencer supports multiple window readout. This means that small ROIs, which are read out sequentially, can be defined in the full image array. Therefore, the sequencer scans all requested kernels line by line.

Window Configuration

Figure 23. Region of Interest Configuration

Figure 23 shows the four parameters defining a region of interest (ROI). These parameters are explained here.

- **x-start[6:0]**
  x-start defines the x-starting point of the desired window. The sensor reads out 64 pixels in a single clock cycle. Therefore, the granularity for configuring the x-start position is also 64 pixels. To find the corresponding column in the pixel array, multiply the value in the x-start register by 64.

- **x-end[6:0]**
  This register defines the window end point on the x-axis. As for x-start, the granularity for this configuration is one kernel. x-end must be larger than x-start. The minimal window width is two kernels.

- **y-start[12:0]**
  This is the start line of the readout window. The granularity of this setting is one line.

- **y-end[12:0]**
  This is the end line of the readout window. y-end must be configured larger than y-start. This setting has the same granularity as the y-start configuration.

The configuration width of the required settings is mentioned between brackets. Seven bits are required for the x boundaries, 13 bits for the y boundaries.

Up to 32 windows can be defined, possibly (partially) overlapping. Figure 24 illustrates the use of overlapping windows. Note that pixel (0,0) is located in the left bottom corner.

For each line to be scanned, the sequencer control block analyzes which windows must be read out, from left to right. The following restrictions apply to the window configurations (they must be valid for each line):

- For each line, the windows are ordered from left to right, based on their x-start address:
  \[ x_{\text{start} \_\text{roi}(i)} \leq x_{\text{start} \_\text{roi}(j)} \text{ where } j > i \]

- Overlapping in the x-direction is restricted to simple window overlapping schemes. When a new window is started, it needs to continue at least until the end of the previous window. In other words, it is not possible to start a window M, overlap with a window M+1, and at the end of window M+1, re-enter window M. The end of window M+1 must coincide or be larger than the end of window M:
  \[ x_{\text{end} \_\text{roi}(i)} \leq x_{\text{end} \_\text{roi}(j)} \text{ where } j > i \]

- For subsampling and binning modes, the start addresses are restricted to even addresses; the end addresses are restricted to even addresses for subsampling and odd addresses for binning. Erroneous start and end addresses are corrected by the sensor logic.

- There are no restrictions on the y-start and y-end addresses for normal readout.

Processing Multiple Windows

Global Shutter

The multiple windowing mechanism described in this section is only valid for the global shutter operation mode. The sequencer control block houses two sets of counters to construct the image frame. As previously described, the y-counter indicates the line that needs to be read out and is incremented at the end of each line. For the start of the frame, the y-counter is initialized to the y-start address of the first window. It runs until the y-end address of the last window.
to be read out. Note that the last window is configured by the configuration registers and is not necessarily window #31.

The x-counter starts counting from the x-start address of the window with the lowest ID that is active on the addressed line. Only windows in which the current y-address is enclosed are taken into account for scanning. Other windows are skipped.

Figure 25 illustrates a practical example of a configuration with five windows. The current position of the read pointer (ys) is indicated by a red line crossing the image array. For this position, three windows need to be read out. The initial start position for the x-kernel pointer is the x-start configuration of ROI1. Kernels are scanned up to the ROI3 x-end position. From there, the x-pointer jumps to the next window, which is ROI4 in this illustration. When reaching ROI4’s x-end position, the read pointer is incremented to the next line and xs is reinitialized to the starting position of ROI1.

NOTES:

- The initial starting point for the readout pointer at the start of a frame is the y-start position of the first active window.
- The read pointer is not necessarily incremented by one, but depending on the configuration, it can jump in y-direction. For Figure 25, this is the case when reaching the end of ROI0 where the read pointer jumps to the y-start position of ROI1.
- The x-pointer starting position is equal to the x-start configuration of the first active window on the current line addressed. This window is not necessarily window #0.
- The x-pointer is not necessarily incremented by one each cycle. At the end of a window it can jump to the start of the next window.

**Rolling Shutter**

Multiple windowing is not supported in rolling shutter mode. Only single-window readout is possible. The active window can be selected among the 32 windows in the configuration. Dynamic window reconfiguration (or dynamic selection of a different window configuration) is supported. Eventual corrupted images due to transients are blanked out in the sensor.

**Subsampling and Binning**

Pixel binning and subsampling methods are used as way of decimating the image. The number of pixel samples is reduced by a factor of four, while the optical area is maintained.

**Pixel Binning**

Pixel binning is a technique in which different pixels belonging to a rectangular bin are averaged in the analog domain. Two-by-two pixel binning is implemented in the VITA 25K sensor. This implies that two adjacent pixels are averaged both in column and row. Binning is configurable using a register setting. Pixel binning is not supported on VITA 25K color option.

Note: register 194[9] needs to be configured to 0x1 for 2x2 pixel binning. When configuring to 0x0, 2x1 binning is obtained (binning in x only).

**Subsampling**

Subsampling is obtained by adapting the readout sequence. In subsampling mode, both lines and pixels are read in a read-N-skip-N mode. This reduces the number of lines in a frame and the number of pixels in a line. Overall frame time is reduced by a factor 4.

The monochrome sensor is read out in a read-one-skip-one pattern for both the rows and the columns, while the color version supports a read-two-skip-two subsampling scheme. This mode is selectable through register configuration. Figure 26 shows which pixels are read and which ones are skipped for monochrome and color sensors respectively. Readout direction is indicated as an x and y arrow.
Signal Gain Path
Table 22 and Table 23 show the available registers (fields) to program the desired exposure time and gain settings. Settings 199[1:0] and 199[15:14] should remain unchanged.

Table 22. EXPOSURE TIME CONFIGURATION REGISTERS

<table>
<thead>
<tr>
<th>Address</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
</table>
| 201     | 0x0000        | Exposure time  
Rolling shutter: granularity = lines  
Global shutter: granularity defined by ‘Mult Timer’ (register 199). |
| 199     | 0x0001        | Mult Timer (global shutter only)  
Defines granularity of exposure and reset length.  
unit = 1/62 MHz for normal ROT mode |
| 200     | 0x0000        | Reset length or Frame Length (global shutter only)  
Granularity defined by ‘Mult Timer’ (register 199) |

Table 23. GAIN CONFIGURATION REGISTERS

<table>
<thead>
<tr>
<th>Address</th>
<th>Unity Gain Configuration</th>
<th>Description</th>
</tr>
</thead>
</table>
| 204 [4:0] | 0x05 | Column gain setting  
0x07: column gain = 2/3x  
0x05: column gain = 1x  
0x09: column gain = 2x  
0x11: column gain = 4x  
Other settings are not supported. |
| 204 [12:5] | 0x4F | AFE gain setting  
0x4F: AFE gain = 1.00x  
0x33: AFE gain = 1.39x  
0x36: AFE gain = 1.94x  
0x66: AFE gain = 2.72x  
Other settings are not supported. |
| 204 [13] |              | Postpone gain update by one frame when ‘1’ to compensate for exposure time updates latency. |
| 205[11:0] | 0x080 | Digital Gain, 5.7 unsigned representation  
(5 bits before decimal point, 7 bits for fractional part). Maximum gain is 31.992 |
Mode Changes and Frame Blanking
Dynamically reconfiguring the sensor may lead to corrupted or non-uniformilly exposed frames. For some reconfigurations, the sensor automatically blanks out the image data during one frame. Frame blanking is summarized in the following table for the sensor’s image related modes.

NOTE: Major mode switching (i.e. switching between rolling and global shutter modes, master, triggered, slave modes) must be performed while the sequencer is disabled (reg_seq_enable = 0x0).

Table 24. DYNAMIC SENSOR RECONFIGURATION AND FRAME BLANKING

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Global Shutter</th>
<th>Rolling Shutter</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Corrupted Frame</td>
<td>Blanked Out Frame</td>
<td>Corrupted Frame</td>
</tr>
<tr>
<td>Shutter Mode and Operation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rolling_shutter_enable</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>triggered_mode</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>slave_mode</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>subsampling</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>binning</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Frame Timing</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>rs_x_length</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>black_lines</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>dummy_lines</td>
<td>N/A</td>
<td>N/A</td>
<td>No</td>
</tr>
<tr>
<td>Exposure Control</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mult_timer</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
</tr>
<tr>
<td>fr_length</td>
<td>No</td>
<td>No</td>
<td>N/A</td>
</tr>
<tr>
<td>exposure</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Gain</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>mux_gainsw</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>afe_gain</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>db_gain</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Window/ROI</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>roi_active</td>
<td>See Note</td>
<td>No</td>
<td>No</td>
</tr>
</tbody>
</table>
Table 24. DYNAMIC SENSOR RECONFIGURATION AND FRAME BLANKING

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Global Shutter</th>
<th>Rolling Shutter</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Corrupted Frame</td>
<td>Blanked Out Frame</td>
<td>Corrupted Frame</td>
</tr>
<tr>
<td>roi<em>_configuration</em></td>
<td>See Note</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Black Calibration

<table>
<thead>
<tr>
<th></th>
<th>No</th>
<th>No</th>
<th>No</th>
<th>No</th>
</tr>
</thead>
<tbody>
<tr>
<td>black_samples</td>
<td>See Note</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>auto_blackcal_enable</td>
<td>See Note</td>
<td>No</td>
<td>See Note</td>
<td>No</td>
</tr>
<tr>
<td>blackcal_offset</td>
<td>See Note</td>
<td>No</td>
<td>See Note</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>If configured within range of configured black lines</td>
<td>Manual correction factors become instantly active when auto_blackcal_enable is deasserted during operation.</td>
<td>Manual blackcal_offset updates are instantly active.</td>
<td></td>
</tr>
</tbody>
</table>

CRC Calculation

<table>
<thead>
<tr>
<th></th>
<th>No</th>
<th>No</th>
<th>No</th>
<th>No</th>
</tr>
</thead>
<tbody>
<tr>
<td>crc_seed</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>Impacts the transmitted CRC</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Sync Channel

<table>
<thead>
<tr>
<th></th>
<th>No</th>
<th>No</th>
<th>No</th>
<th>No</th>
</tr>
</thead>
<tbody>
<tr>
<td>bl</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>img</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>crc</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>tr</td>
<td>No</td>
<td>No</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>Impacts the Sync channel information, not the Data channels.</td>
<td>Impacts the Sync channel information, not the Data channels.</td>
<td>Impacts the Sync channel information, not the Data channels.</td>
<td></td>
</tr>
</tbody>
</table>

Sensor Status

The currently used exposure and gain parameters are reported by the sensor in registers 208 to 214. These status registers are updated at the start of the frame in which these parameters become active.

Temperature Diode

The temperature diode allows the monitoring of the sensor die temperature during operation. The diode can be connected through the pins td_anode and td_cathode.

The die temperature (T_die), as a function of the measured forward threshold voltage of the diode, with a known bias current (V_diode at bias 40 μA), is determined according to the following formula:

\[ T_{\text{die}} = (0.77 - V_{\text{diode at bias 40 μA}})/0.00158^\circ\text{C} \]

Monitor Pins

The sensor features three logic monitor output pins. These pins can provide internal state and synchronization information to the outside system. These status pins can be used during system setup or for system frame synchronization.

The pins are named monitor0, monitor1, and monitor2. The information provided on these pins is configured with the register monitor_select (register 192[13:11]).

NOTE: Monitor indications are generated in the sequencer. These signals lead the image and synchronization data on the LVDS channels.
Table 25. MONITOR SELECT

<table>
<thead>
<tr>
<th>Monitor Select</th>
<th>Monitor Output</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>monitor0: '0'</td>
<td>No information is provided on the output pins. All outputs are driven to logic '0'</td>
</tr>
<tr>
<td></td>
<td>monitor1: '0'</td>
<td></td>
</tr>
<tr>
<td></td>
<td>monitor2: '0'</td>
<td></td>
</tr>
<tr>
<td>0x1</td>
<td>monitor0: Integration time indication</td>
<td>High during integration</td>
</tr>
<tr>
<td></td>
<td>monitor1: ROT indication</td>
<td>High when ROT is active, low outside ROT</td>
</tr>
<tr>
<td></td>
<td>monitor2: Dummy line indication</td>
<td>High during dummy lines, low during all other lines</td>
</tr>
<tr>
<td>0x2</td>
<td>monitor0: Integration time indication</td>
<td>High during integration</td>
</tr>
<tr>
<td></td>
<td>monitor1: N/A</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td>monitor2: N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>0x3</td>
<td>monitor0: Start of X-readout</td>
<td>Pulse indicating the start of x-readout</td>
</tr>
<tr>
<td></td>
<td>monitor1: Black line indication</td>
<td>High during black lines, low during all other lines</td>
</tr>
<tr>
<td></td>
<td>monitor2: Dummy line indication</td>
<td>High during dummy lines, low during all other lines</td>
</tr>
<tr>
<td>0x4</td>
<td>monitor0: Frame start</td>
<td>Pulse indicating the start of a new frame</td>
</tr>
<tr>
<td></td>
<td>monitor1: Start of ROT</td>
<td>Pulse indicating the start of ROT</td>
</tr>
<tr>
<td></td>
<td>monitor2: Start of X-readout</td>
<td>Pulse indicating the start of x-readout</td>
</tr>
<tr>
<td>0x5</td>
<td>monitor0: First line indication</td>
<td>High during the first line of each frame, low for all others</td>
</tr>
<tr>
<td></td>
<td>monitor1: Start of ROT indication</td>
<td>Pulse indicating the start of ROT</td>
</tr>
<tr>
<td></td>
<td>monitor2: End of ROT indication</td>
<td>Pulse indicating the end of ROT</td>
</tr>
<tr>
<td>0x6</td>
<td>monitor0: ROT indication</td>
<td>High when ROT is active, low outside ROT</td>
</tr>
<tr>
<td></td>
<td>monitor1: Start of X-readout</td>
<td>Pulse indicating the start of x-readout</td>
</tr>
<tr>
<td></td>
<td>monitor2: End of X-readout</td>
<td>Pulse indicating the end of x-readout</td>
</tr>
<tr>
<td>0x7</td>
<td>monitor0: Start of X-readout for black lines</td>
<td>Pulse indicating the start of x-readout for black lines</td>
</tr>
<tr>
<td></td>
<td>monitor1: Start of X-readout for image lines</td>
<td>Pulse indicating the start of x-readout for image lines</td>
</tr>
<tr>
<td></td>
<td>monitor2: Start of X-readout for dummy lines</td>
<td>Pulse indicating the start of x-readout for dummy lines</td>
</tr>
</tbody>
</table>
LVDS Output Channels
The image data output occurs through 32 LVDS data channels, operating at 620 Mbps in 10-bit mode and 496 Mbps in 8-bit mode. A synchronization LVDS channel and an LVDS output clock signal synchronizes the data.

The 32 data channels are used to output the image data only. The sync channel transmits information about data sent over these data channels (includes codes indicating black pixels, normal pixels, and CRC).

To perform word synchronization on the output data stream, a predefined training pattern is sent after startup of the sensor and during idle times (during FOT, ROT, and in between frames and lines). This data is used to perform word alignment on the receiving side.

To decrease the data bit rate at the outputs (and reduce the power consumption), the sensor can operate in 8-bit mode.

In 10-bit mode, the words on data and sync channels have a 10-bit length. The words are serialized most significant bit first. The output data rate is 620 Mbps.

In 8-bit mode, the words on data and sync channels have an 8-bit length. The words are serialized most significant bit first. The output data rate is 496 Mbps.

This decreases the data bit rate on the LVDS data channels. Power consumption is reduced by reconfiguring the internal bias currents. LVDS channels run at 248 MHz (DDR) in 8-bit mode.

Table 26. LVDS OUTPUT CHANNELS CONFIGURATION

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Description</th>
<th>Output Data Rate Channel [Mbps]</th>
</tr>
</thead>
<tbody>
<tr>
<td>adc_mode (pin)</td>
<td>8-bit_mode (register)</td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>10-bit mode 620</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>8-bit mode 496</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Not supported N/A</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Not supported N/A</td>
</tr>
</tbody>
</table>

The 8-bit mode is selected using the adc_mode pin. The datablock sync channel is configured accordingly (8-bit mode configuration). In 8-bit mode, the eight most significant bits of the ADC data words are transmitted over the data channels.

Sync channel encoding is similar to the 10-bit mode. The two least significant bits of the (configured) sync codes are omitted and the window ID is transmitted after each frame synchronization word (the two LSBs are to be ignored).

NOTE: The 8-bit mode can only be used to reduce the data rate at the cost of image data resolution. Operating the sensor in 8-bit mode at a higher clock frequency to achieve higher frame rates is not supported.

Serial Link Interface Operation
This sensor’s serial link interface is based on a mesochronous clocking system. This means that all data and control links operate at the same frequency, but their phase may be different due to skew. The host provides an LVDS clock as input to the sensor. To compensate for possible large on-chip delays, the sensor retransmits this clock with the same delay as that seen by the data (32 data channels) and control path (one sync channel). The receiver end (generally an FPGA-based system) performs per-interface skew compensation.

The data on high-speed serial links can drift due to various reasons such as skew, jitter, PCB trace delays, process, voltage, and temperature variations. The receiver performs per-LVDS interface skew compensation using bit and word alignment techniques.

To support per-interface skew compensation, the sensor provides a training mode that allows the system to perform bit and word alignment on all interfaces.

During idle moments (when the sensor is not capturing images or during frame and line overhead), the image sensor transmits training patterns. These patterns are configurable by means of a register upload and should be chosen such that these can easily be detected by reducing the risk of mimicking in the regular data stream.

Bit Alignment
Bit alignment procedures position the sampling edge of the clock at the center of the data eye window by adding delay to the data path (using delay taps).

Word Alignment
Word alignment procedures ensure that the reconstructed parallel data bits are in correct order at the output of the deserializer. Word alignment is done by looking for well known training patterns.

All major FPGA vendors provide bit and word alignment methods for their FPGAs. Refer to the FPGA vendor’s application for more information on the use of these functionalities.

When the host succeeds in a lock for bit and word alignment procedures, the system enables the sensor for image acquisition. Specific frame alignment patterns are transmitted for image frame synchronization purposes.

Frame Format
The frame format is explained by example of the readout of two (overlapping) windows, as shown in Figure 27 (a).

The readout of a frame occurs on a line-by-line basis. In this representation, the read pointer goes from left to right, bottom to top.

Figure 27 indicates that, after the FOT is complete, a number of lines which only include information of ‘ROI 0’
are sent out, starting at position \( y_0_{\text{start}} \). When the line at position \( y_1_{\text{start}} \) is reached, a number of lines containing data of ‘ROI 0’ and ‘ROI 1’ are sent out, until the line position of \( y_0_{\text{end}} \) is reached. From there on, only data of ‘ROI 1’ appears on the data output channels until line position \( y_1_{\text{end}} \) is reached.

NOTE: Only frame start and frame end sync words are indicated in (b). CRC codes are also omitted from Figure 27.

During readout of image data over the data channels, the sync channel sends out frame synchronization codes, which provide information related to the image data being sent over the 32 data output channels.

Each line of a window starts with a line start (LS) indication and ends with a line end (LE) indication. The line start of the first line is replaced by a frame start; the line end of the last line is replaced with a frame end indication. Each such frame synchronization code is followed by a window ID (range 0 to 31).

The data channels contain valid pixel data during FS/FE/LS/LE and window ID synchronization codes.

NOTE: For overlapping windows, the line synchronization codes of the overlapping windows with lower IDs are not sent out. As shown in the illustration, no LE is transmitted for the overlapping part of window 0.

Black lines are read out at the start of a frame. These lines are enclosed by LS and LE indications (no frame start/end). The window ID for the black lines must be ignored.

![Diagram of frame sync codes](image)

**Figure 27. Frame Sync Codes**

Figure 28 and Figure 29 show the details of the readout of a number of lines for single window readout, at the beginning of the frame.

Figure 30 shows the details of the readout of a number of lines for two overlapping windows.
Figure 28. Timeline Showing Readout of Black Line for Global Shutter

NOTE: For rolling shutter, the number of black pixels on one line is reduced to the selected window’s length. The sequence shown is repeated if more than one black line is generated.

Figure 29. Timeline for Single Window Readout

NOTE: In the figure, the second image line is shown in more detail. The LS code is replaced by FS for the first line and the LE code is replaced by FE for the last line in the window.

Figure 30. Timeline Showing Readout of Two Overlapping Windows
Frame Format in 8-bit Mode

The frame format is identical to the 10-bit mode. Sync and data word depth is reduced to eight bits. Synchronization Words

Table 27. FRAME SYNCHRONIZATION CODE DETAILS FOR 10-BIT MODE

<table>
<thead>
<tr>
<th>Sync Word Bit Position</th>
<th>Register Address</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:7</td>
<td>N/A</td>
<td>0x5</td>
<td>Frame start indication</td>
</tr>
<tr>
<td>9:7</td>
<td>N/A</td>
<td>0x6</td>
<td>Frame end indication</td>
</tr>
<tr>
<td>9:7</td>
<td>N/A</td>
<td>0x1</td>
<td>Line start indication</td>
</tr>
<tr>
<td>9:7</td>
<td>N/A</td>
<td>0x2</td>
<td>Line end indication</td>
</tr>
<tr>
<td>6:0</td>
<td>131[6:0]</td>
<td>0x2A</td>
<td>These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting</td>
</tr>
</tbody>
</table>

Window Identification

Frame synchronization codes are always followed by a 5-bit window identification (bits 4:0). This is an integer number, ranging from 0 to 31, indicating the active window. If more than one window is active for the current cycle, the highest window ID is transmitted.

Data Classification Codes

For the remaining cycles, the sync channel indicates the type of data sent through the data links: black pixel data (BL), image data (IMG), or training pattern (TR). These codes are programmable by a register setting. The default values are listed in Table 28.

Table 28. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 10-BIT MODE

<table>
<thead>
<tr>
<th>Sync Word Bit Position</th>
<th>Register Address</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>9:0</td>
<td>132 [9:0]</td>
<td>0x015</td>
<td>Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.</td>
</tr>
<tr>
<td>9:0</td>
<td>133 [9:0]</td>
<td>0x035</td>
<td>Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).</td>
</tr>
<tr>
<td>9:0</td>
<td>134 [9:0]</td>
<td>0x059</td>
<td>CRC value. The data on the data output channels is the CRC code of the finished image data line.</td>
</tr>
<tr>
<td>9:0</td>
<td>135 [9:0]</td>
<td>0x3A6</td>
<td>Training pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.</td>
</tr>
</tbody>
</table>

Frame Synchronization in 8-bit Mode

The frame synchronization words are configured using the same registers as in 10-bit mode. The two least significant bits of these configuration registers are ignored and not sent out. Table 29 shows the structure of the frame synchronization code, together with the default value, as specified in SPI registers. The same restriction for overlapping windows applies in 8-bit mode.

Table 29. FRAME SYNCHRONIZATION CODE DETAILS FOR 8-BIT MODE

<table>
<thead>
<tr>
<th>Sync Word Bit Position</th>
<th>Register Address</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:5</td>
<td>N/A</td>
<td>0x5</td>
<td>Frame start (FS) indication</td>
</tr>
<tr>
<td>7:5</td>
<td>N/A</td>
<td>0x6</td>
<td>Frame end (FE) indication</td>
</tr>
<tr>
<td>7:5</td>
<td>N/A</td>
<td>0x1</td>
<td>Line start (LS) indication</td>
</tr>
<tr>
<td>7:5</td>
<td>N/A</td>
<td>0x2</td>
<td>Line end (LE) indication</td>
</tr>
<tr>
<td>4:0</td>
<td>[6:2]</td>
<td>0x0A</td>
<td>These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting.</td>
</tr>
</tbody>
</table>
Window Identification
Similar to 10-bit operation mode, the frame synchronization codes are followed by a window identification. The window ID is located in bits 6:2 (all other bit positions are ‘0’). The same restriction for overlapping windows applies in 8-bit mode.

Data Classification Codes
BL, IMG, CRC, and TR codes are defined by the same registers as in 10-bit mode. Bits 9:2 of the respective configuration registers are used as classification code. The default values are listed in Table 30.

<table>
<thead>
<tr>
<th>Sync Word Bit Position</th>
<th>Register Address</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>7:0</td>
<td>132 [9:2]</td>
<td>0x05</td>
<td>Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.</td>
</tr>
<tr>
<td>7:0</td>
<td>133 [9:2]</td>
<td>0x0D</td>
<td>Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).</td>
</tr>
<tr>
<td>7:0</td>
<td>134 [9:2]</td>
<td>0x16</td>
<td>CRC value. The data on the data output channels is the CRC code of the finished image data line.</td>
</tr>
<tr>
<td>7:0</td>
<td>135 [9:2]</td>
<td>0xE9</td>
<td>Training Pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.</td>
</tr>
</tbody>
</table>

Training Patterns on Data Channels
In 10-bit mode, during idle periods, the data channels transmit training patterns, indicated on the sync channel by a TR code. These training patterns are configurable independent of the training code on the sync channel as shown in Table 31. In 8-bit mode, the training pattern for the data channels is defined by the same register as in 8-bit mode, where the lower two bits are omitted; see Table 32.

<table>
<thead>
<tr>
<th>Sync Word Bit Position</th>
<th>Register Address</th>
<th>Default Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>[9:0]</td>
<td>130 [9:0]</td>
<td>0x3A6</td>
<td>Data channel training pattern. The data output channels send out the training pattern, which can be programmed by a register setting. The default value of the training pattern is 0x3A6, which is identical to the training pattern indication code on the sync channel.</td>
</tr>
</tbody>
</table>

Cyclic Redundancy Code
At the end of each line, a CRC code is calculated to allow error detection at the receiving end. Each data channel transmits a CRC code to protect the data words sent during the previous cycles. Idle and training patterns are not included in the calculation.

The sync channel is not protected. A special character (CRC indication) is transmitted whenever the data channels send their respective CRC code.

The polynomial in 10-bit operation mode is $x^{10}+x^9+x^6+x^3+x^2+x+1$. The CRC encoder is seeded at the start of a new line and updated for every (valid) data word received. The CRC seed is configurable using the crc_seed register. When ‘0’, the CRC is seeded by all-‘0’; when ‘1’ it is seeded with all-‘1’.

In 8-bit mode, the polynomial is $x^8+x^6+x^3+x^2+1$. The CRC seed is configured by means of the crc_seed register.

Black Reference
The sensor reads out one or more black lines at the start of every new frame. The number of black lines to be generated is programmable and is at a minimum, equal to 1. The length of the black lines depends on the operation mode. For rolling shutter mode, it is equal to the line length configured in the active window. For global shutter mode, the sensor always reads out the entire line (80 kernels), independent of window configurations.

The black references are used to perform black calibration and offset compensation in the data channels. The raw black pixel data is transmitted over the usual LVDS channels, while the regular image data is compensated (can be bypassed).

On the output interface, black lines can be seen as a separate window, without frame start and ends (only line start and ends). The window ID is to be ignored and data is indicated by a BL code. In 8-bit mode, the configuration of the black level calibration block automatically scales to 8-bit mode. No reconfiguration is required.
Example Using Multiple Windowing

Figure 31 shows an example of the synchronization codes sent when reading out multiple windows.

Figure 31. Synchronization Codes for Multiple Windows (applicable for Global Shutter only)

where

\[ x_{size 0} = x_{end 0} - x_{start 0} + 1 \]
\[ x_{size 1} = x_{end 1} - x_{start 1} + 1 \]

DC = “Don’t Care”
Data Order

To read out the image data through the output channels, the pixel array is organized in kernels. The kernel size is 64 pixels in x-direction by one pixel in y-direction. The data order in 8-bit mode is identical to the 10-bit mode. Figure 32 indicates how the kernels are organized. The data order of this image data on the data output channels depends on the subsampling mode.

Figure 32. Kernel Organization in Pixel Array

- No Subsampling
  The image data is read out in kernels of 64 pixels in x-direction by one pixel in y-direction. One data channel output delivers two pixel values of one kernel sequentially.

Figure 33 shows how a kernel is read out over the 32 output channels. For even positioned kernels, the kernels are read out ascending, and for odd positioned kernels the data order is reversed (descending).

Figure 33. Data Output Order when Subsampling is Disabled

- Subsampling on monochrome sensor
  During subsampling, every other pixel is read out and the lines are read in a read-1-skip-1 manner. To read out the image data with subsampling enabled, two neighboring kernels are combined to a single kernel of 128 pixels in the x-direction and one pixel in the y-direction. Only the pixels at the even pixel positions inside that kernel are read out. Figure 34 shows the data order.

Note that there is no difference in data order for even and odd kernel numbers. This is opposed to the ‘no-sampling’ readout described earlier.
Binning Mode
The output order in binning mode is identical to the subsampled mode.

- Subsampling on color sensor
To read out the image data with subsampling enabled on a color sensor, two neighboring kernels are combined to a single kernel of 128 pixels in the x-direction and 1 pixel in the y-direction. Only the pixels 0, 1, 4, 5, 8, 9, 12, 13 to 124, and 125 are read out. Figure 35 shows the data order. There is no difference in data order for even/odd kernel numbers, as opposed to the ‘no-subsampling’ readout described in section.

Frame Rate
Frame rate for subsampling and binning mode is compared to the normal mode. Assume the y-resolution is the programmed number of lines to read out.

Normal Readout
The frame time in normal readout mode is shown by the following formula:
\[
\text{Frame Time} = t_{\text{FOT}} + (\text{y-resolution}) \times (t_{\text{ROT}} + t_{\text{readout}})
\]
The frame rate is equal to \(1/\text{Frame Time}\). Nominal frame rate for full frame readout is 53 fps.

Subsampling Mode
The frame time for subsampled readout is shown by the following formula:
\[
\text{Frame Time} = t_{\text{FOT}} + (\text{y-resolution} / 2) \times (t_{\text{ROT}} + t_{\text{readout}} / 2),
\]
where \(t_{\text{ROT}}\) represents the equivalent ROT time for a normal readout of the same frame. Analogous readout represents the equivalent readout time for normal readout.
The maximum frame rate in subsampled readout of the full resolution of the sensor is \(~160\ \text{fps}\).
Binning Mode

The frame time for subsampled readout is given by the following formula:

\[ \text{Frame Time} = t_{\text{FOT}} + \left( \frac{y \text{-resolution}}{2} \right) \times (t_{\text{ROT}} \times 2 + \frac{t_{\text{readout}}}{2}) \]

where \( t_{\text{ROT}} \) represents the equivalent ROT time for a normal readout of the same frame. Analogous readout represents the equivalent readout time for normal readout.

In binning mode, the maximum frame rate in subsampled readout of the full resolution of the sensor is \(~110 \text{ fps}~\).

Test Pattern Generation

The data block provides several test pattern generation capabilities. Figure 36 shows the functional diagram for the data channels. It is possible to inject synthesized test patterns at various points. Refer to the Register Map on page 43 for the test mode configuration registers (registers 144 to 150).

In 8-bit mode, test patterns are generated as in 10-bit mode, however the two least significant bits of the resulting data are not transmitted.

The test pattern modes are summarized in Table 33. Note that these modes only exist for the data channel. The sync and clock channels do not provide this functionality.

For each test mode, the user can select whether the generated data is framed. When the register frame_testpattern is asserted, the test data simply replaces the ADC data. This means that the test data is only sent between frame/line start and frame/line end indications. Outside these windows, regular training patterns are sent, as during normal operation. CRC is calculated and inserted as for normal data for the fixed and incrementing test pattern generation.

<table>
<thead>
<tr>
<th>Register Configuration</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>prbs_en</td>
<td>testpattern_en</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
</tr>
</tbody>
</table>

When frame_testpattern is deasserted, the output is constantly replaced by the generated test data. No training patterns are generated.

Figure 36. Functional Block Diagrams for the Data Channels

NOTE: In the figure, register configurations are indicated in red.

The sync channel continues to send regular frame timing information when the sequencer is enabled (independently of the test pattern configurations).

The synthesized test patterns are injected directly into the data channels. Therefore, no data demultiplexing is required at the receiving end (as opposed to regular image data capture).
**Fixed Pattern**

A configured word can be continuously repeated on the output. This word is configurable for each data channel separately (testpattern). The testpattern is inserted when testpattern_en is asserted.

**Incrementing Test Pattern**

In each cycle, the test pattern word is incremented by one, when inc_testpattern is asserted. After reaching the maximum value, the incremenet is reset to its start value (testpattern). When the testdata is framed, the incremenet is also reset to the testpattern value at each line start.

To enable this mode, enable the digital testpattern mode (assert testpattern_en) and assert inc_testpattern.

**Pseudo Random Bit Sequence Generation**

In this test mode, the output channels are sourced with pseudo random bit sequence (PRBS) pattern. The PRBS seed can be configured for each data channel using the testpattern register. For the other test pattern generation mode, the datastream is not interrupted when frame_testpattern is deasserted.

**NOTES:**

- The CRC generator is not functional in this mode, and no real CRC can be calculated. Instead, the CRC slot is used to send one more PRBS word.
- A PRBS generator does not generate random data when the seed is all zero. Therefore, it is advisable to configure the testpattern registers to a value different from ‘0’. Using different seeds for each channel results in different sequences for each data channel.
Each functional entity has a dedicated address space, starting at a block offset. The register address is obtained by adding the address offset to the block offset. This address must be used to perform SPI uploads and is shown in the Address column of the register map table.

Table 34. REGISTER MAP

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Address</th>
<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
<th>Description</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chip ID [Block Offset: 0]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0  0</td>
<td>chip_id</td>
<td>[15:0] id</td>
<td>0x56FA</td>
<td>22266</td>
<td>RO</td>
<td>ON Semiconductor Chip ID</td>
<td></td>
</tr>
<tr>
<td>1  1</td>
<td>revision</td>
<td>[3:0] rev</td>
<td>0x0001</td>
<td>1</td>
<td>RO</td>
<td>Chip Revision Numbering Note: Refer to ES1 data sheet if 0x0.</td>
<td></td>
</tr>
<tr>
<td>2  2</td>
<td>chip_configuration</td>
<td>[0] color</td>
<td>0x00000</td>
<td>0</td>
<td>RO</td>
<td>Configure according to part number: NOIV1SN025KA-GDC: 0x0 NOIV1SE025KA-GDC: 0x1</td>
<td></td>
</tr>
<tr>
<td>Clock Generator [Block Offset: 32]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0  32</td>
<td>config</td>
<td>[0] enable</td>
<td>0x00004</td>
<td>4</td>
<td>RW</td>
<td>Enable analogue clocks '0' = disabled, '1' = enabled</td>
<td></td>
</tr>
<tr>
<td>14:1 reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>General Logic [Block Offset: 34]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0  34</td>
<td>config</td>
<td>[0] enable</td>
<td>0x00000</td>
<td>0</td>
<td>RW</td>
<td>Logic General Enable Configuration '0' = Disable '1' = Enable</td>
<td></td>
</tr>
<tr>
<td>Image Core [Block Offset: 40]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0  40</td>
<td>image_core_config</td>
<td>[0] reserved</td>
<td>0x00000</td>
<td>0</td>
<td>RW</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1  41</td>
<td>image_core_config</td>
<td>[1] mux_psd_n</td>
<td>0x0B5A</td>
<td>2906</td>
<td>RW</td>
<td>Column Multiplexer Power Down '0' = powered down, '1' = powered up</td>
<td></td>
</tr>
<tr>
<td>12:0 reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>13 testpattern</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Testpattern generation in the columns</td>
<td></td>
</tr>
<tr>
<td>14 injectlevel</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Inject level for testpattern generation</td>
<td></td>
</tr>
<tr>
<td>15 reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>AFE [Block Offset: 48]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0  48</td>
<td>power_down</td>
<td>[0] reserved</td>
<td>0x00000</td>
<td>0</td>
<td>RW</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>
### Table 34. REGISTER MAP

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Address</th>
<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
<th>Description</th>
<th>Access</th>
</tr>
</thead>
</table>
| 0              | 64      |           | power_down    | 0x0000      | 0       | Power down bandgap
|                |         |           |               |             |         | '0' = powered down, '1' = powered up | RW     |
| 1              | 65      |           | configuration | 0x888B      | 34955   | External Resistor Selection
|                |         |           |               |             |         | '0' = internal resistor, '1' = external resistor | RW     |
|                |         | [3:1]     | bg_trim       | 0x5         | 5       | Bandgap Trim |        |
|                |         | [7:4]     | imc_colpc_ibias | 0x8        | 8       | Column Precharge ibias Configuration |        |
|                |         | [11:8]    | imc_colbias_ibias | 0x8       | 8       | Column Bias ibias Configuration |        |
|                |         | [15:12]   | reserved      | 0x8         | 8       | Reserved |        |
| 2              | 66      |           | afe_bias      | 0x53C8      | 21448   | AFE ibias Configuration | RW     |
|                |         | [3:0]     | afe_ias       | 0x8         | 8       | AFE ibias Configuration |        |
|                |         | [7:4]     | afe_adc_iref  | 0xC         | 12      | ADC iref Configuration |        |
|                |         | [14:8]    | afe_pga_iref  | 0x53        | 83      | PGA iref Configuration |        |
| 3              | 67      |           | mux_bias      | 0x8888      | 34952   | Column Multiplexer Stage 1 Bias Configuration | RW     |
|                |         | [3:0]     | mux_25u_stage1 | 0x8        | 8       | Column Multiplexer Stage 1 Bias Configuration |        |
|                |         | [7:4]     | mux_25u_stage2 | 0x8        | 8       | Column Multiplexer Stage 2 Bias Configuration |        |
|                |         | [11:8]    | mux_25u_delay | 0x8         | 8       | Column Multiplexer Delay Bias Configuration |        |
|                |         | [15:12]   | mux_25u_vcmbuff | 0x8      | 8       | Column Multiplexer Vcm Bias Configuration |        |
| 4              | 68      |           | lvds_bias     | 0x0088      | 136     | LVDS Bias | RW     |
|                |         | [3:0]     | lvds_ias      | 0x8         | 8       | LVDS Ibias |        |
|                |         | [7:4]     | lvds_iref     | 0x8         | 8       | LVDS Iref |        |
| 6              | 70      |           | reserved      | 0x8888      | 34952   | Reserved | RW     |
|                |         | [15:0]    | reserved      | 0x8888      | 34952   | Reserved |        |

#### Test [Block Offset: 80]

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Address</th>
<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
<th>Description</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>80</td>
<td></td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[9:0]</td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>81</td>
<td></td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15:0]</td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>96</td>
<td></td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[5:0]</td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>97</td>
<td></td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>RO</td>
<td></td>
</tr>
</tbody>
</table>
Table 34. REGISTER MAP

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Address</th>
<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
<th>Description</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0</td>
<td>[7:0]</td>
<td>reserved</td>
<td>0x00</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>Ser/lvds/io [Block Offset: 112]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>112</td>
<td></td>
<td>power_down</td>
<td>0x0000</td>
<td>0</td>
<td>Power down for Clock Output. ’0’ =powered down, ’1’ = powered up</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[0]</td>
<td>clock_out_pwd_n</td>
<td>0x00</td>
<td>0</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[1]</td>
<td>sync_pwd_n</td>
<td>0x00</td>
<td>0</td>
<td>Power down for Sync channel ’0’ = powered down, ’1’ = powered up</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[2]</td>
<td>data_pwd_n</td>
<td>0x00</td>
<td>0</td>
<td>Power down for data channels (4 channels) ’0’ = powered down, ’1’ = powered up</td>
<td></td>
</tr>
<tr>
<td>Data Block [Block Offset: 128]</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>0</td>
<td>128</td>
<td>[7:0]</td>
<td>blackcal</td>
<td>0x4008</td>
<td>16392</td>
<td>Desired black level at output</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[10:8]</td>
<td>black_samples</td>
<td>0x00</td>
<td>0</td>
<td>Black pixels taken into account for black calibration. Total samples = 2**black_samples</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[14:11]</td>
<td>reserved</td>
<td>0x8</td>
<td>8</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15]</td>
<td>crc_seed</td>
<td>0x00</td>
<td>0</td>
<td>CRC Seed ’0’ = All-0 ’1’ = All-1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>129</td>
<td>[9:0]</td>
<td>general_configuration</td>
<td>0xC001</td>
<td>49153</td>
<td></td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[9:1]</td>
<td>blackcal_offset</td>
<td>0x00</td>
<td>0</td>
<td>Black Calibration offset used when auto_black_cal_en = ’0’.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[10]</td>
<td>blackcal_offset_dec</td>
<td>0x00</td>
<td>0</td>
<td>blackcal_offset is added when 0, subtracted when 1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[11]</td>
<td>reserved</td>
<td>0x0</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[12]</td>
<td>reserved</td>
<td>0x0</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[13]</td>
<td>8bit_mode</td>
<td>0x0</td>
<td>0</td>
<td>Shifts window ID indications by 4 cycles. ’0’ = 10 bit mode, ’1’ = 8 bit mode</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15:14]</td>
<td>reserved</td>
<td>0x3</td>
<td>3</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>130</td>
<td></td>
<td>trainingpattern</td>
<td>0x03A6</td>
<td>934</td>
<td></td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[9:0]</td>
<td>trainingpattern</td>
<td>0x03A6</td>
<td>934</td>
<td>Training pattern sent on Data channels during idle mode. This data is used to perform word alignment on the LVDS data channels.</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[10]</td>
<td>reserved</td>
<td>0x0</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>131</td>
<td></td>
<td>sync_code0</td>
<td>0x002A</td>
<td>42</td>
<td></td>
<td>RW</td>
</tr>
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</table>
Table 34. REGISTER MAP

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Address</th>
<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
<th>Description</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>132</td>
<td>[6:0]</td>
<td>frame_sync</td>
<td>0x02A</td>
<td>42</td>
<td>Frame Sync LSBs</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Note: The three MSBs of the resulting 10-bit Frame sync word is not configurable. The tenth bit indicates frame/line sync code, ninth bit indicates start, eighth bit indicates end.</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>133</td>
<td>[9:0]</td>
<td>sync_code2</td>
<td>0x0035</td>
<td>53</td>
<td>Black Pixel Identification Sync Code</td>
<td>RW</td>
</tr>
<tr>
<td>6</td>
<td>134</td>
<td>[9:0]</td>
<td>sync_code3</td>
<td>0x0059</td>
<td>89</td>
<td>Valid Pixel Identification Sync Code</td>
<td>RW</td>
</tr>
<tr>
<td>7</td>
<td>135</td>
<td>[9:0]</td>
<td>sync_code4</td>
<td>0x03A6</td>
<td>934</td>
<td>Training Value Identification Sync Code</td>
<td>RW</td>
</tr>
<tr>
<td>8</td>
<td>136</td>
<td></td>
<td>blackcal_error0</td>
<td>0x0000</td>
<td>0</td>
<td>Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 0-15</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15:0]</td>
<td>blackcal_error[15:0]</td>
<td>0x0000</td>
<td>0</td>
<td>Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 0-15</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>137</td>
<td>[15:0]</td>
<td>blackcal_error1</td>
<td>0x0000</td>
<td>0</td>
<td>Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 16-31</td>
<td>RO</td>
</tr>
<tr>
<td>10</td>
<td>138</td>
<td>[15:0]</td>
<td>blackcal_error2</td>
<td>0x0000</td>
<td>0</td>
<td>Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 16-31</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15:0]</td>
<td>blackcal_error[47:32]</td>
<td>0x0000</td>
<td>0</td>
<td>Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 32-47</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>139</td>
<td>[15:0]</td>
<td>blackcal_error3</td>
<td>0x0000</td>
<td>0</td>
<td>Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 32-47</td>
<td>RO</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15:0]</td>
<td>blackcal_error[63:48]</td>
<td>0x0000</td>
<td>0</td>
<td>Black Calibration Error. This flag is set when not enough black samples are available. Black Calibration shall not be valid. Channels 48-63</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>140</td>
<td></td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15:0]</td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>141</td>
<td></td>
<td>reserved</td>
<td>0xFFFF</td>
<td>65535</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15:0]</td>
<td>reserved</td>
<td>0xFFFF</td>
<td>65535</td>
<td>Reserved</td>
<td></td>
</tr>
</tbody>
</table>

(Datablock - Test)

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Address</th>
<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
<th>Description</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>144</td>
<td></td>
<td>test_configuration</td>
<td>0x0000</td>
<td>0</td>
<td>Insert synthesized testpattern when '1', normal operation when '0'.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[0]</td>
<td>test_pattern_en</td>
<td>0x0000</td>
<td>0</td>
<td>Insert synthesized testpattern when '1', normal operation when '0'.</td>
<td></td>
</tr>
<tr>
<td>Address Offset</td>
<td>Address</td>
<td>Bit Field</td>
<td>Register Name</td>
<td>Default Hex</td>
<td>Default</td>
<td>Description</td>
<td>Access</td>
</tr>
<tr>
<td>----------------</td>
<td>---------</td>
<td>-----------</td>
<td>---------------</td>
<td>-------------</td>
<td>---------</td>
<td>-------------</td>
<td>--------</td>
</tr>
<tr>
<td>[1]</td>
<td></td>
<td></td>
<td>inc_testpattern</td>
<td>0x0</td>
<td>0</td>
<td>Incrementing testpattern when '1', constant testpattern when '0'</td>
<td></td>
</tr>
<tr>
<td>[2]</td>
<td></td>
<td></td>
<td>prbs_en</td>
<td>0x0</td>
<td>0</td>
<td>Incrementing testpattern when '1', constant testpattern when '0'. Lower bound is defined by testpattern*, upper bound is 1023. After reaching 1023, the counter is reloaded with configured start data.</td>
<td></td>
</tr>
<tr>
<td>[3]</td>
<td></td>
<td></td>
<td>frame_testpattern</td>
<td>0x0</td>
<td>0</td>
<td>Frame test patterns when '1', unframed testpatterns when '0'</td>
<td></td>
</tr>
<tr>
<td>[4]</td>
<td></td>
<td></td>
<td>reserved</td>
<td>0x0</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>145</td>
<td></td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td>[15:0]</td>
<td></td>
<td></td>
<td>reserved</td>
<td>0</td>
<td>0</td>
<td>Reserved</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>146</td>
<td></td>
<td>test_configuration0</td>
<td>0x0100</td>
<td>256</td>
<td>Testpattern (LSBs) used on datapath #0, #6, #16, #24 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td>RW</td>
</tr>
<tr>
<td>[7:0]</td>
<td></td>
<td></td>
<td>testpattern0_lsb</td>
<td>0x00</td>
<td>0</td>
<td>Testpattern (LSBs) used on datapath #0, #6, #16, #24 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td></td>
</tr>
<tr>
<td>[15:8]</td>
<td></td>
<td></td>
<td>testpattern1_lsb</td>
<td>0x01</td>
<td>1</td>
<td>Testpattern (LSBs) used on datapath #1, #9, #17, #25 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>147</td>
<td></td>
<td>test_configuration1</td>
<td>0x0302</td>
<td>770</td>
<td>Testpattern (LSBs) used on datapath #2, #10, #18, #26 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td>RW</td>
</tr>
<tr>
<td>[7:0]</td>
<td></td>
<td></td>
<td>testpattern2_lsb</td>
<td>0x02</td>
<td>2</td>
<td>Testpattern (LSBs) used on datapath #2, #10, #18, #26 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td></td>
</tr>
<tr>
<td>[15:8]</td>
<td></td>
<td></td>
<td>testpattern3_lsb</td>
<td>0x03</td>
<td>3</td>
<td>Testpattern (LSBs) used on datapath #3, #11, #19, #27 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>148</td>
<td></td>
<td>test_configuration2</td>
<td>0x0504</td>
<td>1284</td>
<td>Testpattern (LSBs) used on datapath #4, #12, #20, #28 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td>RW</td>
</tr>
<tr>
<td>[7:0]</td>
<td></td>
<td></td>
<td>testpattern4_lsb</td>
<td>0x04</td>
<td>4</td>
<td>Testpattern (LSBs) used on datapath #4, #12, #20, #28 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td></td>
</tr>
<tr>
<td>[15:8]</td>
<td></td>
<td></td>
<td>testpattern5_lsb</td>
<td>0x05</td>
<td>5</td>
<td>Testpattern (LSBs) used on datapath #5, #13, #21, #29 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>149</td>
<td></td>
<td>test_configuration3</td>
<td>0x0706</td>
<td>1798</td>
<td>Testpattern (LSBs) used on datapath #6, #14, #22, #30 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td>RW</td>
</tr>
<tr>
<td>[7:0]</td>
<td></td>
<td></td>
<td>testpattern6_lsb</td>
<td>0x06</td>
<td>6</td>
<td>Testpattern (LSBs) used on datapath #6, #14, #22, #30 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td></td>
</tr>
</tbody>
</table>
Table 34. REGISTER MAP

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Address</th>
<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
<th>Description</th>
<th>Access</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>150</td>
<td>[15:8]</td>
<td>testpattern7_lsb</td>
<td>0x07</td>
<td>7</td>
<td>Testpattern (LSBs) used on datapath #7, #15, #23, #31 when testpattern_en = '1'. Note: Most significant bits are configured in register 150.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[1:0]</td>
<td>testpattern0_msb</td>
<td>0x0</td>
<td>0</td>
<td>Testpattern (LSBs) used on datapath #0, #8, #16, #24 when testpattern_en = '1'. Note: Least significant bits are configured in register 146.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[3:2]</td>
<td>testpattern1_msb</td>
<td>0x0</td>
<td>0</td>
<td>Testpattern (MSBs) used on datapath #1, #9, #17, #25 when testpattern_en = '1'. Note: Least significant bits are configured in register 146.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[5:4]</td>
<td>testpattern2_msb</td>
<td>0x0</td>
<td>0</td>
<td>Testpattern (MSBs) used on datapath #2, #10, #18, #26 when testpattern_en = '1'. Note: Least significant bits are configured in register 147.</td>
<td>RW</td>
</tr>
<tr>
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<td></td>
<td>[7:6]</td>
<td>testpattern3_msb</td>
<td>0x0</td>
<td>0</td>
<td>Testpattern (MSBs) used on datapath #3, #11, #19, #27 when testpattern_en = '1'. Note: Least significant bits are configured in register 147.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[9:8]</td>
<td>testpattern4_msb</td>
<td>0x0</td>
<td>0</td>
<td>Testpattern (MSBs) used on datapath #4, #12, #20, #28 when testpattern_en = '1'. Note: Least significant bits are configured in register 148.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[11:10]</td>
<td>testpattern5_msb</td>
<td>0x0</td>
<td>0</td>
<td>Testpattern (MSBs) used on datapath #5, #13, #21, #29 when testpattern_en = '1'. Note: Least significant bits are configured in register 148.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
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<td>[13:12]</td>
<td>testpattern6_msb</td>
<td>0x0</td>
<td>0</td>
<td>Testpattern (MSBs) used on datapath #6, #14, #22, #30 when testpattern_en = '1'. Note: Least significant bits are configured in register 149.</td>
<td>RW</td>
</tr>
<tr>
<td></td>
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<td>[15:14]</td>
<td>testpattern7_msb</td>
<td>0x0</td>
<td>0</td>
<td>Testpattern (MSBs) used on datapath #7, #15, #23, #31 when testpattern_en = '1'. Note: Least significant bits are configured in register 149.</td>
<td>RW</td>
</tr>
<tr>
<td>26</td>
<td>154</td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td></td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td>27</td>
<td>155</td>
<td>reserved</td>
<td>0x0000</td>
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<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td>0</td>
<td>160</td>
<td>reserved</td>
<td>0x0000</td>
<td>0</td>
<td></td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[15:0]</td>
<td>reserved</td>
<td></td>
<td></td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td>31</td>
<td>191</td>
<td>reserved</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>RW</td>
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</tbody>
</table>
Table 34. REGISTER MAP

<table>
<thead>
<tr>
<th>Address Offset</th>
<th>Address</th>
<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
<th>Description</th>
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<tbody>
<tr>
<td>0</td>
<td>192</td>
<td>[15:0]</td>
<td>reserved</td>
<td></td>
<td>Reserved</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[0]</td>
<td>enable</td>
<td>0x0</td>
<td>0</td>
<td>Enable sequencer 0 = Idle, 1 = enabled</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[1]</td>
<td>rolling_shutter_enable</td>
<td>0x0</td>
<td>0</td>
<td>Operation Selection 0 = Global Shutter, 1 = Rolling Shutter</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>[2]</td>
<td>reserved</td>
<td>0x0</td>
<td>0</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[3]</td>
<td>reserved</td>
<td>0x0</td>
<td>0</td>
<td>Reserved</td>
<td>RW</td>
</tr>
<tr>
<td></td>
<td></td>
<td>[4]</td>
<td>triggered_mode</td>
<td>0x0</td>
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<td>Triggered Mode Selection (Global Shutter only) 0 = Normal Mode, 1 = Triggered Mode</td>
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Table 34. REGISTER MAP

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4 196  roi_active1 | 0x0000  | 0 | RW |
| [0]            | roi_active16 | 0x00 | Selection of ROI 16 | '0' = inactive, '1' = active |
| [1]            | roi_active17 | 0x00 | Selection of ROI 17 | '0' = inactive, '1' = active |
| [2]            | roi_active18 | 0x00 | Selection of ROI 18 | '0' = inactive, '1' = active |
| [3]            | roi_active19 | 0x00 | Selection of ROI 19 | '0' = inactive, '1' = active |
| [4]            | roi_active20 | 0x00 | Selection of ROI 20 | '0' = inactive, '1' = active |
| [5]            | roi_active21 | 0x00 | Selection of ROI 21 | '0' = inactive, '1' = active |
| [6]            | roi_active22 | 0x00 | Selection of ROI 22 | '0' = inactive, '1' = active |
### Table 34. REGISTER MAP

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<tr>
<th>Address Offset</th>
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<th>Bit Field</th>
<th>Register Name</th>
<th>Default Hex</th>
<th>Default</th>
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Table 34. REGISTER MAP

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NOTE: applicable to Production silicon only and is not backward compatible with "ES1" silicon
Pin Description
Refer to Electrical Specifications on page 5 for power supplies and references. The CMOS outputs follow the JEDEC Standard (JEDEC−JESD8C−01).

Table 35. PIN DESCRIPTION

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<tr>
<th>Pin No.</th>
<th>Name</th>
<th>Type</th>
<th>Direction</th>
<th>Description</th>
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<td>Digital supply - 1.8 V domain</td>
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### Mechanical Specifications

#### Table 36. MECHANICAL SPECIFICATIONS

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<td>0</td>
<td>50</td>
<td>μm</td>
</tr>
<tr>
<td></td>
<td>Die center, Y offset to the center of the package</td>
<td>50</td>
<td>0</td>
<td>50</td>
<td>μm</td>
</tr>
<tr>
<td></td>
<td>Die position, tilt to the die attach pad plane</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>deg</td>
</tr>
<tr>
<td></td>
<td>Die rotation accuracy between die scribe and lead fingers of package on all four sides</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>deg</td>
</tr>
<tr>
<td></td>
<td>Optical center referenced from the package center with Pin1 located bottom right (X-dir)</td>
<td>-50.2</td>
<td>-0.2</td>
<td>49.8</td>
<td>μm</td>
</tr>
<tr>
<td></td>
<td>Optical center referenced from the package center with Pin1 located bottom right (Y-dir)</td>
<td>3552</td>
<td>3602</td>
<td>3652</td>
<td>μm</td>
</tr>
<tr>
<td>Glass Lid</td>
<td>Distance from bottom of the package to top of the die surface</td>
<td>1.75</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td>Specification</td>
<td>Distance from top of the die surface to top of the glass lid</td>
<td>1.45</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td></td>
<td>XY size</td>
<td>32.47 x 39.4</td>
<td>(+10%)</td>
<td>mm²</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Thickness</td>
<td>0.7</td>
<td></td>
<td></td>
<td>mm</td>
</tr>
<tr>
<td></td>
<td>Spectral range for glass window</td>
<td>400</td>
<td>1000</td>
<td></td>
<td>nm</td>
</tr>
<tr>
<td></td>
<td>Transmission of the Glass lid (refer to Figure 44)</td>
<td></td>
<td></td>
<td>92</td>
<td>%</td>
</tr>
<tr>
<td>Mechanical Shock</td>
<td>JESD22-B104C; Condition G</td>
<td></td>
<td>2000</td>
<td></td>
<td>G</td>
</tr>
<tr>
<td>Vibration</td>
<td>JESD22-B103B; Condition 1</td>
<td>20</td>
<td>2000</td>
<td></td>
<td>Hz</td>
</tr>
<tr>
<td>Mounting Profile</td>
<td>Pb–free wave soldering profile for pin grid array package</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**NOTE:** Optical center min/max tolerance is calculated on X/Y package tolerances with Pin 1 as a reference.
Figure 37. VITA 25K Package Diagram

All dimensions are in mm, unless specified otherwise.
Optical Center Information

The center of the die (CD) is the center of the cavity.
The center of the die (CD) is exactly at 50% between the outsides of the two outer seal rings.
The center of the cavity is exactly at 50% between the insides of the finger pads.

- Die outer dimensions:
  - B4 is the reference for the Die (0,0) in μm
  - B1 is at (0,32500) μm
  - B2 is at (25500,32500) μm
  - B3 is at (25500,0) μm

- Active Area outer dimensions:
  - A1 is at (1214.1, 31387.8) μm
  - A2 is at (24285.6, 31387.8) μm
  - A3 is at (24285.6, 8316.3) μm
  - A4 is at (1214.1, 8316.3) μm

- Center of the Active Area:
  - AA is at (12749.8, 19852) μm

- Center of the Die:
  - CD is at (12750, 16250) μm

Figure 38. Graphical Representation of the Optical Center
Glass Lid
The VITA 25K image sensor uses a glass lid without any coatings. Figure 39 shows the transmission characteristics of the glass lid.

As seen in Figure 39, the sensor does not have an infrared attenuating filter glass. A filter must be provided in the optical path when color devices are used (source: http://www.pgo-online.com).

Figure 39. Transmission Characteristics of Glass Lid

SILICON ERRATA

This section describes the erratum for the VITA 25K family. Details include erratum trigger conditions, scope of impact, available workaround, and silicon revision applicability.

VITA 25K Qualification Status
Production Silicon

VITA 25K Errata Summary
This table defines how the errata applies to the VITA 25K.

<table>
<thead>
<tr>
<th>Items</th>
<th>Part Number</th>
<th>Silicon revision</th>
<th>Fix Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1]. Higher Standby current than rated in data sheet</td>
<td>VITA 25K family</td>
<td>Production Silicon</td>
<td>Silicon fix planned</td>
</tr>
</tbody>
</table>

Higher Standby Current

- **PROBLEM DEFINITION**
  In all states except for ‘idle’ and ‘running’ (including ‘reset’) there can be abnormal high power consumption on vdd\_33.

- **PARAMETERS AFFECTED**
  Power

- **TRIGGER CONDITION(S)**
  Entering an affected state (reset, standby(1), standby(2)).

- **SCOPE OF IMPACT**
  High power consumption, not influencing performance when grabbing images.

- **WORKAROUND**
  Maintain the device in ‘power-off’, ‘idle’ or ‘running’ modes.

- **FIX STATUS**
  The cause of this problem and its solution have been identified. Silicon fix is planned to correct the deficiency.

- **COMPLETION DATE**
  Production silicon with Stand-by current fix is planned.
Application Notes and other resources can be found linked to the product web page at www.onsemi.com. Additional information on this device may also be available in the Image Sensor Portal, accessible within the MyON section of www.onsemi.com. A signed NDA is required to access the Image Sensor Portal – please see your ON Semiconductor sales representative for more information.


The Product Acceptance Criteria document, which lists criteria to which this device is tested prior to shipment, is available upon request.
<table>
<thead>
<tr>
<th>Acronym</th>
<th>Description</th>
<th>Acronym</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>Analog-to-Digital Converter</td>
<td>LE</td>
<td>Line End</td>
</tr>
<tr>
<td>AFE</td>
<td>Analog Front End</td>
<td>LS</td>
<td>Line Start</td>
</tr>
<tr>
<td>BL</td>
<td>Black pixel data</td>
<td>LSB</td>
<td>least significant bit</td>
</tr>
<tr>
<td>CDM</td>
<td>Charged Device Model</td>
<td>LVDS</td>
<td>Low-Voltage Differential Signaling</td>
</tr>
<tr>
<td>CDS</td>
<td>Correlated Double Sampling</td>
<td>MSB</td>
<td>most significant bit</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary Metal Oxide Semiconductor</td>
<td>PGA</td>
<td>Programmable Gain Amplifier</td>
</tr>
<tr>
<td>CRC</td>
<td>Cyclic Redundancy Check</td>
<td>PLS</td>
<td>Parasitic Light Sensitivity</td>
</tr>
<tr>
<td>DAC</td>
<td>Digital-to-Analog Converter</td>
<td>PRBS</td>
<td>Pseudo-Random Binary Sequence</td>
</tr>
<tr>
<td>DDR</td>
<td>Double Data Rate</td>
<td>PRNU</td>
<td>Photo Response Non-Uniformity</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential Non-Linearity</td>
<td>QE</td>
<td>Quantum Efficiency</td>
</tr>
<tr>
<td>DS</td>
<td>Double Sampling</td>
<td>RGB</td>
<td>Red-Green-Blue</td>
</tr>
<tr>
<td>EIA</td>
<td>Electronic Industries Alliance</td>
<td>RMA</td>
<td>Return Material Authorization</td>
</tr>
<tr>
<td>ESD</td>
<td>Electrostatic Discharge</td>
<td>RMS</td>
<td>Root Mean Square</td>
</tr>
<tr>
<td>FE</td>
<td>Frame End</td>
<td>ROI</td>
<td>Region of Interest</td>
</tr>
<tr>
<td>FOT</td>
<td>Frame Overhead Time</td>
<td>ROT</td>
<td>Row Overhead Time</td>
</tr>
<tr>
<td>FPGA</td>
<td>Field Programmable Gate Array</td>
<td>S/H</td>
<td>Sample and Hold</td>
</tr>
<tr>
<td>FPN</td>
<td>Fixed Pattern Noise</td>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
</tr>
<tr>
<td>FPS</td>
<td>Frame per Second</td>
<td>SPI</td>
<td>Serial Peripheral Interface</td>
</tr>
<tr>
<td>FS</td>
<td>Frame Start</td>
<td>TIA</td>
<td>Telecommunications Industry Association</td>
</tr>
<tr>
<td>HBM</td>
<td>Human Body Model</td>
<td>Tj</td>
<td>Junction temperature</td>
</tr>
<tr>
<td>IMG</td>
<td>Image data (regular pixel data)</td>
<td>TR</td>
<td>Training pattern</td>
</tr>
<tr>
<td>INL</td>
<td>Integral Non-Linearity</td>
<td>% RH</td>
<td>Percent Relative Humidity</td>
</tr>
<tr>
<td>IP</td>
<td>Intellectual Property</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
GLOSSARY

conversion gain A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron (1.602E 19 Coulomb) and C is the capacitance of the photodiode or sense node.

CDS Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light.

CFA Color filter array. The materials deposited on top of pixels that selectively transmit color.

DNL Differential non-linearity (for ADCs)

DSNU Dark signal non-uniformity. This parameter characterizes the degree of non-uniformity in dark leakage currents, which can be a major source of fixed pattern noise.

fill-factor A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured.

INL Integral nonlinearity (for ADCs)

IR Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm.

Lux Photometric unit of luminance (at 550 nm, 1lux = 1 lumen/m² = 1/683 W/m²)

pixel noise Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane.

photometric units Units for light measurement that take into account human physiology.

PLS Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes.

PRNU Photo-response non-uniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination.

QE Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent.

read noise Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal.

reset The process by which a pixel photodiode or sense node is cleared of electrons. “Soft” reset occurs when the reset transistor is operated below the threshold. “Hard” reset occurs when the reset transistor is operated above threshold.

reset noise Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS.

responsivity The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.

ROI Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane.

sense node In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself.

sensitivity A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m²)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux is equal to 1 W/m²; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.

spectral response The photon wavelength dependence of sensitivity or responsivity.

SNR Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency.

temporal noise Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels.