NL17SH14

Single Schmitt-Trigger Inverter

The NL17SH14 is a single gate CMOS Schmitt−trigger inverter fabricated with silicon gate CMOS technology. The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The NL17SH14 input structure provides protection when voltages up to 7 V are applied, regardless of the supply voltage. This allows the NL17SH14 to be used to interface 5 V circuits to 3 V circuits.

The NL17SH14 can be used to enhance noise immunity or to square up slowly changing waveforms.

Features

- High Speed: t_{PD} = 4.0 ns (Typ) at V_{CC} = 5.0 V
- Low Power Dissipation: I_{CC} = 1.0 μA (Max) at T_A = 25°C
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Pin and Function Compatible with Other Standard Logic Families
- Chip Complexity: FETs = 101
- These Devices are Pb−Free and are RoHS Compliant

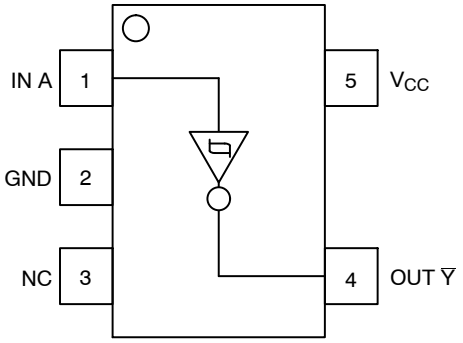


Figure 1. Pinout

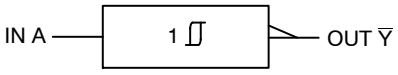


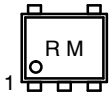
Figure 2. Logic Symbol

ON Semiconductor®

http://onsemi.com

MARKING DIAGRAM

SOT−953
CASE 527AE



R = Specific Device Code
M = Month Code

PIN ASSIGNMENT	
1	IN A
2	GND
3	NC
4	OUT $\overline{Y}$
5	V_{CC}

FUNCTION TABLE

Input A	Output $\overline{Y}$
L	H
H	L

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +7.0	V
V_{IN}	DC Input Voltage		−0.5 to +7.0	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	V_{IN} < GND	−20	mA
I_{OK}	DC Output Diode Current	V_{OUT} < GND, V_{OUT} > V_{CC}	±20	mA
I_{OUT}	DC Output Source/Sink Current		±12.5	mA
I_{CC}	DC Supply Current per Supply Pin		±25	mA
I_{GND}	DC Ground Current per Ground Pin		±25	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	
V_{ESD}	ESD Withstand Voltage	Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	>2000 >300 N/A	V
$I_{LATCHUP}$	Latchup Performance	Above V_{CC} and Below GND at 125°C (Note 5)	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm−by−1 inch, 2−ounce copper trace with no air flow.
2. Tested to EIA/JESD22−A114−A.
3. Tested to EIA/JESD22−A115−A.
4. Tested to JESD22−C101−A.
5. Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Characteristics		Min	Max	Unit
V_{CC}	Positive DC Supply Voltage		1.65	5.5	V
V_{IN}	Digital Input Voltage		0.0	5.5	V
V_{OUT}	Output Voltage		0.0	V_{CC}	V
T_A	Operating Temperature Range		−55	+125	°C
$\Delta t / \Delta V$	Input Transition Rise or Fail Rate	V_{CC} = 3.3 V ± 0.3 V V_{CC} = 5.0 V ± 0.5 V	0 0	No Limit No Limit	ns/V

DEVICE JUNCTION TEMPERATURE VERSUS TIME TO 0.1% BOND FAILURES

Junction Temperature °C	Time, Hours	Time, Years
80	1,032,200	117.8
90	419,300	47.9
100	178,700	20.4
110	79,600	9.4
120	37,000	4.2
130	17,800	2.0
140	8,900	1.0

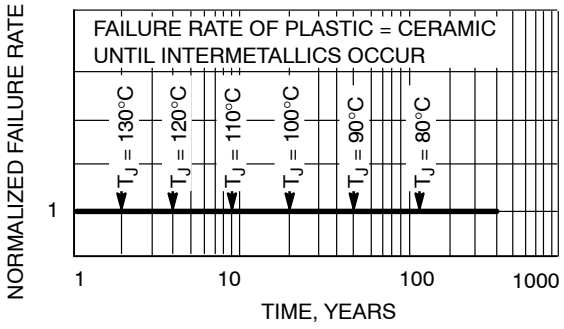


Figure 3. Failure Rate vs. Time Junction Temperature

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} (V)	T_A = 25°C			$T_A \leq$ 85°C		−55°C to 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
V_{T+}	Positive Threshold Voltage		3.0 4.5 5.5		2.0 3.0 3.6	2.2 3.15 3.85		2.2 3.15 3.85		2.2 3.15 3.85	V
V_{T-}	Negative Threshold Voltage		3.0 4.5 5.5	0.9 1.35 1.65	1.5 2.3 2.9		0.9 1.35 1.65		0.9 1.35 1.65		V
V_H	Hysteresis Voltage		3.0 4.5 5.5	0.3 0.4 0.5	0.57 0.67 0.74	1.2 1.4 1.6	0.3 0.4 0.5	1.2 1.4 1.6	0.3 0.4 0.5	1.2 1.4 1.6	V
V_{OH}	High−Level Output Voltage	$V_{IN} \leq V_{Tmin}$ I_{OH} = −50 μA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5		1.9 2.9 4.4		1.9 2.9 4.4		V
		$V_{IN} \leq V_{Tmin}$ I_{OH} = −4 mA I_{OH} = −8 mA	3.0 4.5	2.58 3.94			2.48 3.80		2.34 3.66		
V_{OL}	Low−Level Output Voltage	$V_{IN} \geq V_{Tmax}$ I_{OL} = 50 μA	2.0 3.0 4.5		0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V
		$V_{IN} \geq V_{Tmax}$ I_{OL} = 4 mA I_{OL} = 8 mA	3.0 4.5			0.36 0.36		0.44 0.44		0.52 0.52	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND	0 to 5.5			±0.1		±1.0		±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND	5.5			1.0		20		40	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f$ = 3.0 ns)

Symbol	Parameter	V_{CC} (V)	Test Conditions	T_A = 25°C			$T_A \leq$ 85°C		−55°C to 125°C		Unit
				Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A to $\overline{Y}$	3.0 to 3.6	C_L = 15 pF C_L = 50 pF		7.0 8.5	12.8 16.3	1.0 1.0	15.0 18.5	1.0 1.0	17.0 20.5	ns
		4.5 to 5.5	C_L = 15 pF C_L = 50 pF		4.0 5.5	8.6 10.6	1.0 1.0	10.0 12.0	1.0 1.0	11.5 13.5	
C_{IN}	Input Capacitance				5.0	10		10		10	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Note 6)	7.0	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: $I_{CC(OPR)} = C_{PD} \bullet V_{CC} \bullet f_{in} + I_{CC}$. C_{PD} is used to determine the no−load dynamic power consumption; $P_D = C_{PD} \bullet V_{CC}^2 \bullet f_{in} + I_{CC} \bullet V_{CC}$.

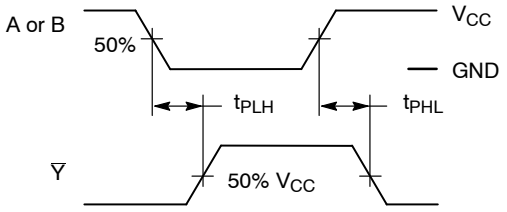
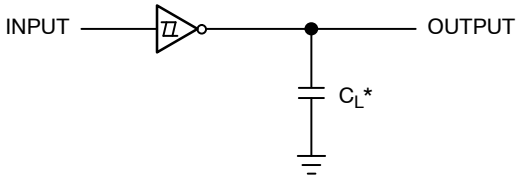


Figure 4. Switching Waveform



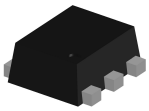
*Includes all probe and jig capacitance.
A 1 MHz square input wave is recommended for propagation delay tests.

Figure 5. Test Circuit

ORDERING INFORMATION

Device	Package	Shipping†
NL17SH14P5T5G	SOT−953 (Pb−Free)	8000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

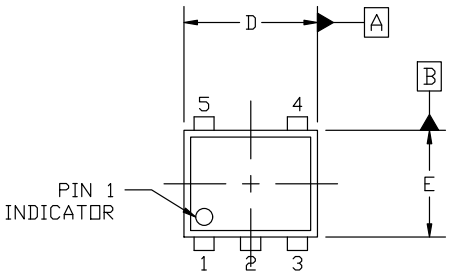


SOT−953 1.00x0.80x0.37, 0.35P
CASE 527AE
ISSUE F

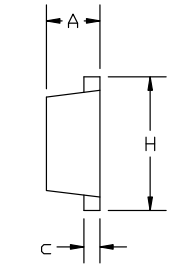
DATE 17 JAN 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

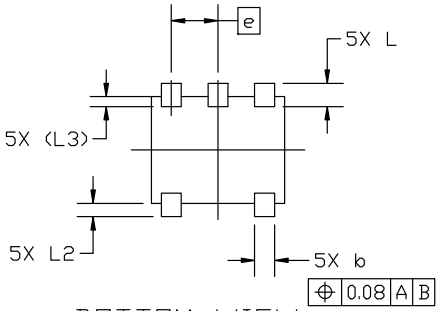
MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.34	0.37	0.40
b	0.10	0.15	0.20
C	0.07	0.12	0.17
D	0.95	1.00	1.05
E	0.75	0.80	0.85
e	0.35 BSC		
H	0.95	1.00	1.05
L	0.125	0.175	0.225
L2	0.05	0.10	0.15
L3	0.075 (REF)		



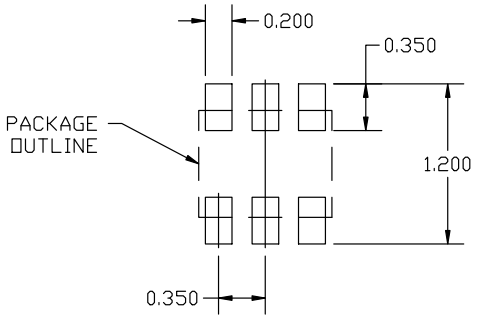
TOP VIEW



SIDE VIEW



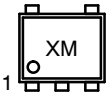
BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



X = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON26457D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SOT−953 1.00x0.80x0.37, 0.35P**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

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