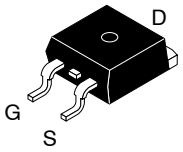
# N-Channel, Logic Level Enhancement Mode Field Effect Transistor

# NDB5060L




**D2PAK−3**
**(TO−263, 3−LEAD)**
**CASE 418AJ**

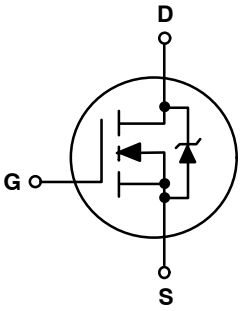
### General Description

These logic level N−Channel enhancement mode power field effect transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process has been especially tailored to minimize on−state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC−DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in−line power loss, and resistance to transients are needed.

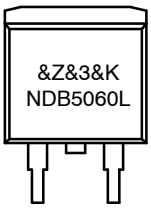
### Features

- 26 A, 60 V
  - $R_{DS(ON)}$ = 0.05 mΩ @ $V_{GS}$ = 5 V
  - $R_{DS(ON)}$ = 0.035 mΩ @ $V_{GS}$ = 10 V
- Critical DC Electrical Parameters Specified at Elevated Temperature
- Rugged Internal Source−Drain Diode Can Eliminate the Need for an External Zener Diode Transient Suppressor
- 175°C Maximum Junction Temperature Rating
- High Density Cell Design for Extremely Low $R_{DS(ON)}$
- $D^2PAK$ Package for Both Through Hole and Surface Mount Applications

### N−CHANNEL MOSFET




### MARKING DIAGRAM




&Z = Assembly Plan Code
&3 = 3−Digit Date Code Code (Year & Week)
&K = 2−Digits Lot Run Traceability Code
NDB5060L = Specific Device Code

### ABSOLUTE MAXIMUM RATINGS $T_C$ = 25°C unless otherwise noted

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $V_{DSS}$ | Drain−Source Voltage | 60 | V |
| $V_{DGR}$ | Drain−Gate Voltage ($R_{GS}$ ≤ 1 MΩ) | 60 | V |
| $V_{GSS}$ | Drain−Source Voltage<br>− Continuous<br>− Nonrepetiti ($t_p$ < 50 μs) | <br>±16<br>±25 | V |
| $I_D$ | Drain Current<br>− Continuous<br>− Pulsed | <br>26<br>78 | A |
| $P_D$ | Total Power Dissipatiion @ $T_C$ = 25°C | 68 | W |
| | − Derate above 25°C | 0.45 | W/°C |
| $T_J$,$T_{STG}$ | Operating and Storage Temperature Range | −65 to 175 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Rating | Value | Unit |
|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction−to−Case | 2.2 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction−to−Ambient | 62.5 | °C/W |

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NDB5060L | D2PAK−3<br>(Pb−Free) | 800 /<br>Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise specified)

| Symbol | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DRAIN−SOURCE AVALANCHE RATINGS** (Note 1) | | | | | | |
| $W_{DSS}$ | Single Pulse Drain−Source Avalanche Energy | $V_{DD}$ = 30 V, $I_D$ = 26 A | – | – | 100 | mJ |
| $I_{AR}$ | Maximum Drain−Source Avalanche Current | | – | – | 26 | A |
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain−Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 μA | 60 | – | – | V |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | – | – | 250 | μA |
| | | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V, $T_J$ = 125°C | – | – | 1 | mA |
| $I_{GSSF}$ | Gate−Body Leakage, Forward | $V_{GS}$ = 16 V, $V_{DS}$ = 0 V | – | – | 100 | nA |
| $I_{GSSR}$ | Gate−Body Leakage, Reverse | $V_{GS}$ = −16 V, $V_{DS}$ = 0 V | – | – | −100 | nA |
| **ON CHARACTERISTICS** (Note 1) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | 1 | 1.4 | 2 | V |
| | | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA, $T_J$ = 125°C | 0.65 | 1 | 1.5 | |
| $R_{DS(ON)}$ | Static Drain−Source On−Resistance | $V_{GS}$ = 5 V, $I_D$ = 13 A | – | 0.042 | 0.05 | Ω |
| | | $V_{GS}$ = 5 V, $I_D$ = 13 A, $T_J$ = 125°C | – | 0.07 | 0.08 | |
| | | $V_{GS}$ = 10 V, $V_{DS}$ = 13 A | – | 0.031 | 0.035 | |
| $I_{D(on)}$ | On−State Drain Current | $V_{GS}$ = 5 V, $V_{DS}$ = 10 V | 26 | – | – | A |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = 10 V, $I_D$ = 13 A | – | 16 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = 30 V, $V_{GS}$ = 0 V, f = 1.0 MHz | – | 840 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 230 | – | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 75 | – | pF |
| **SWITCHING CHARACTERISTICS** (Note 1) | | | | | | |
| $t_{D(on)}$ | Turn − On Delay Time | $V_{DD}$ = 30 V, $I_D$ = 26 A, $V_{GS}$ = 5 V, $R_{GEN}$ = 30 Ω, $R_{GS}$ = 30 Ω | – | 13 | 20 | nS |
| $t_r$ | Turn − On Rise Time | | – | 200 | 400 | nS |
| $t_{D(off)}$ | Turn − Off Delay Time | | – | 45 | 80 | nS |
| tf | Turn − Off Fall Time | | – | 102 | 200 | nS |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = 24 V, $I_D$ = 26 A, $V_{GS}$ = 5 V | – | 17 | 24 | nC |
| $Q_{gs}$ | Gate−Source Charge | | – | 4 | – | nC |
| $Q_{gd}$ | Gate−Drain Charge | | – | 10 | – | nC |
| **DRAIN−SOURCE DIODE CHARACTERISTICS** | | | | | | |
| $I_S$ | Maximum Continuos Drain−Source Diode Forward Current | | – | – | 26 | A |
| $I_{SM}$ | Maximum Pulsed Drain−Source Diode Forward Current | | – | – | 78 | A |
| $V_{SD}$ | Drain−Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = 13 A (Note 1) | – | 0.9 | 1.3 | V |
| $t_{rr}$ | Reverse Recovery Time | $V_{GS}$ = 0 V, $I_F$ = 26 A, $dI_F/dt$ = 100 A/μs | – | 54 | 120 | ns |
| $I_{rr}$ | Reverse Recovery Current | | – | 2.1 | 8 | A |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL CHARACTERISTICS

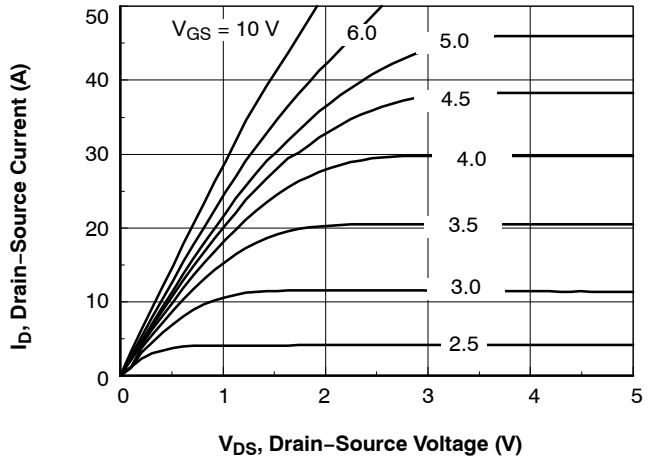



**Figure 1. On−Region Characteristics**

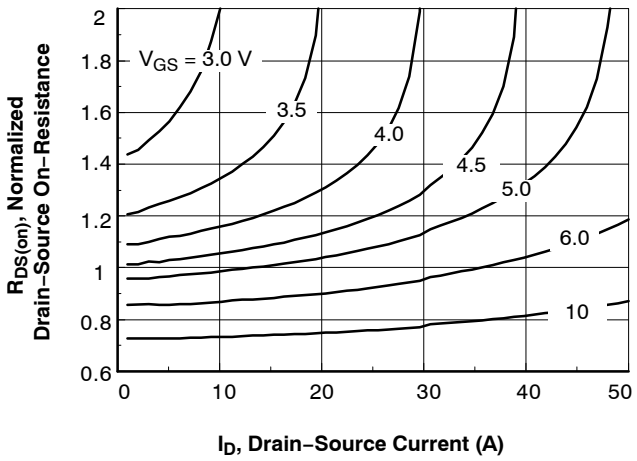



**Figure 2. On−Resistance Variation with Gate Voltage and Drain Current**

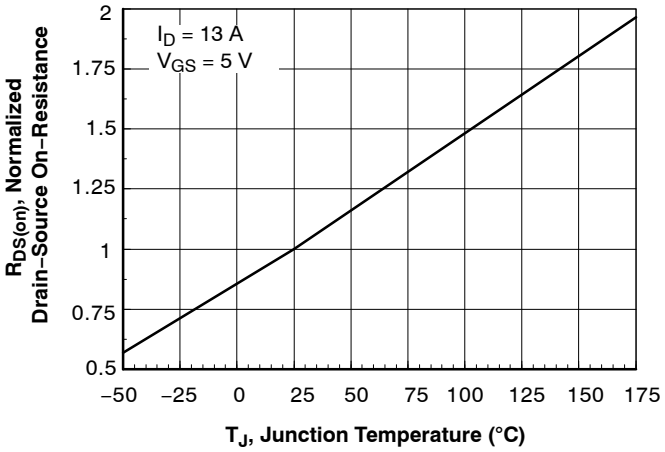



**Figure 3. On−Resistance Variation with Temperature**

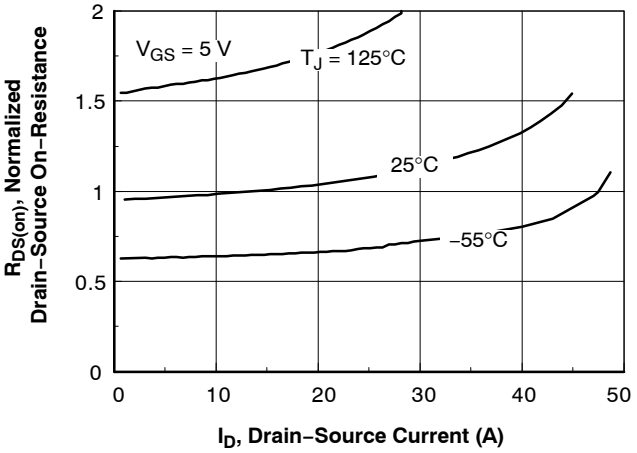



**Figure 4. On−Resistance Variation with Drain Current and Temperature**

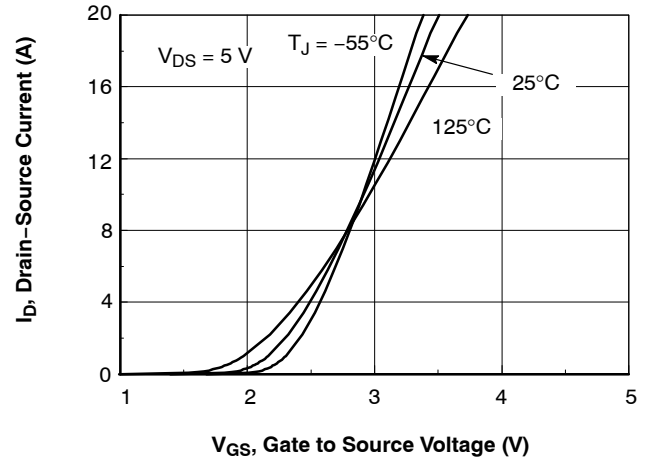



**Figure 5. Transfer Characteristics**

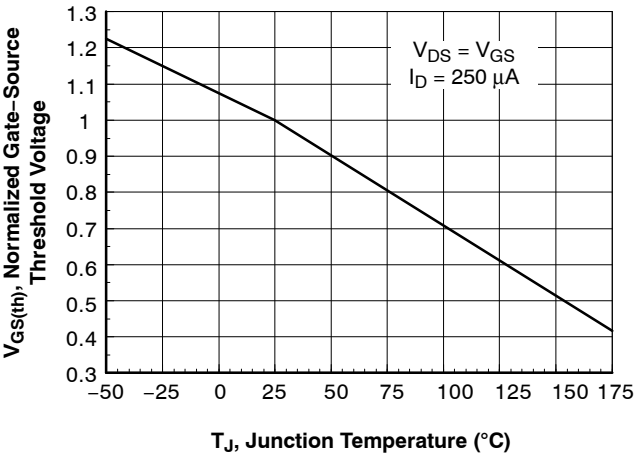



**Figure 6. Gate Threshold Variation with Temperature**

## TYPICAL CHARACTERISTICS (Continued)

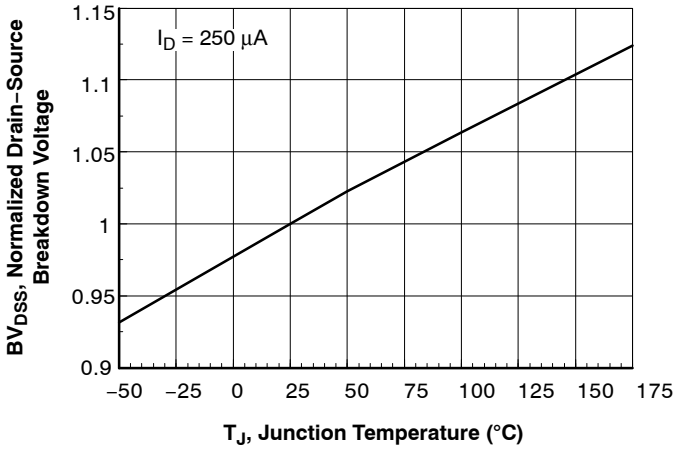



**Figure 7. Breakdown Voltage Variation with Temperature**

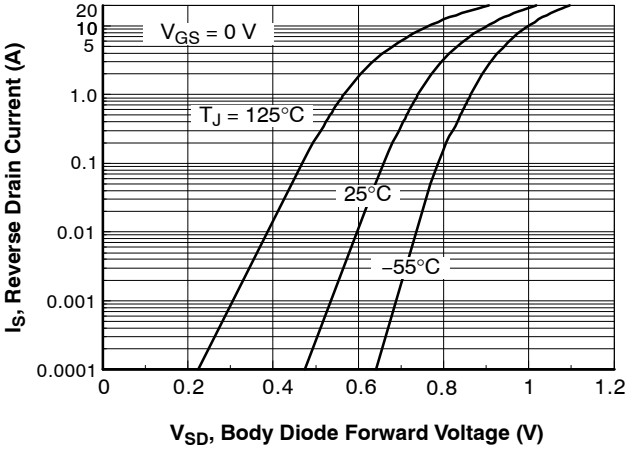



**Figure 8. Body Diode Forward Voltage Variation with Current and Temperature**

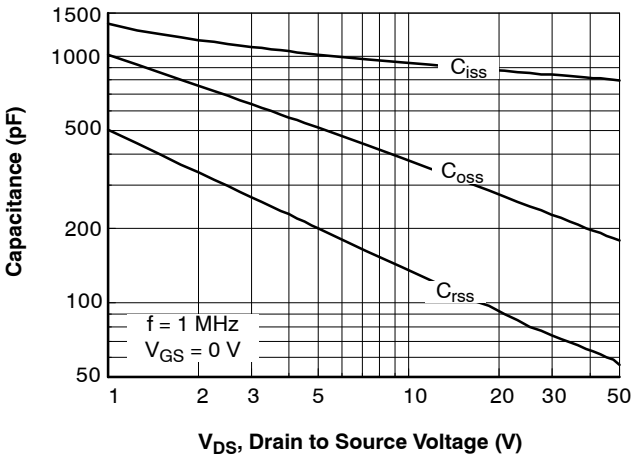



**Figure 9. Capacitance Characteristics**

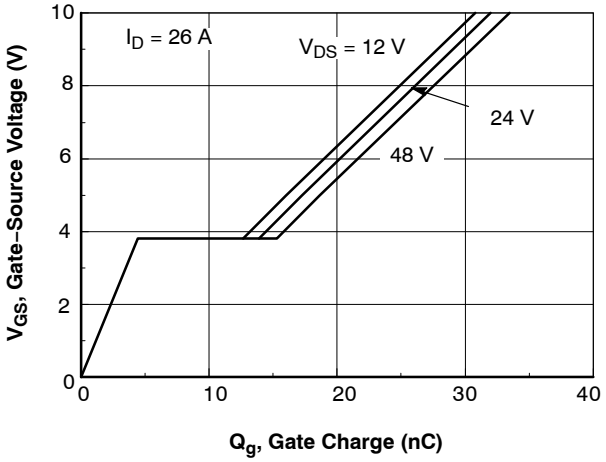



**Figure 10. Gate Charge Characteristics**

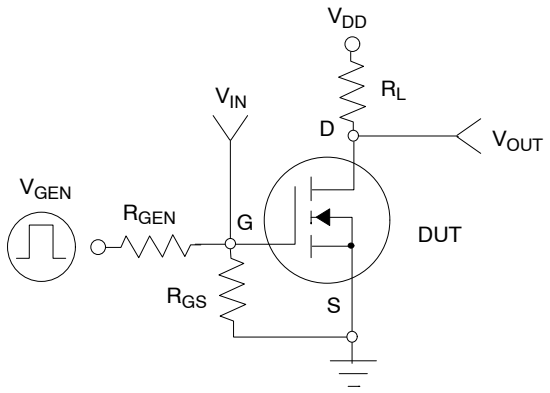



**Figure 11. Switching Test Circuit**

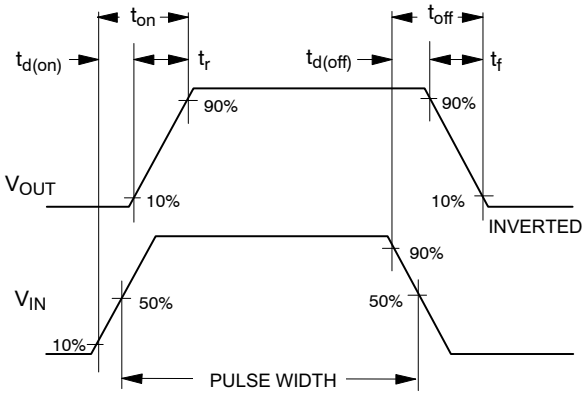



**Figure 12. Switching Waveforms**

## TYPICAL CHARACTERISTICS (Continued)

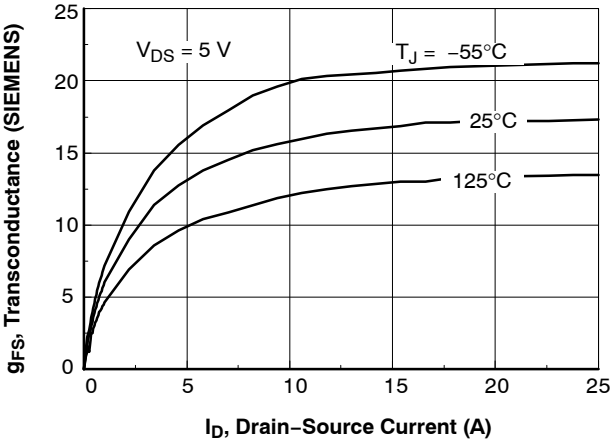



**Figure 13. Transconductance Variation with Drain Current and Temperature**

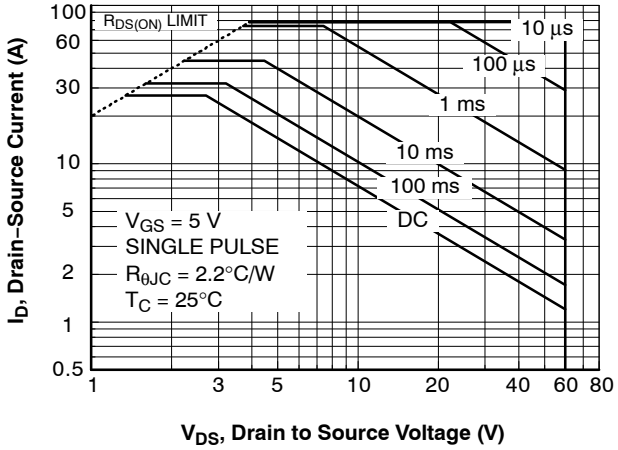



**Figure 14. Maximum Safe Operating Area**

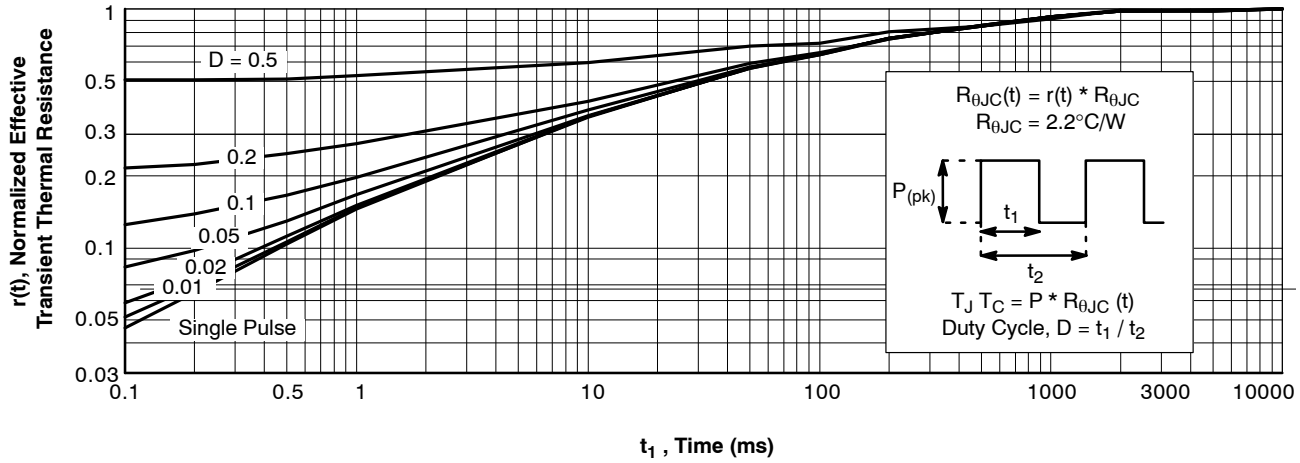
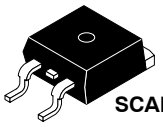


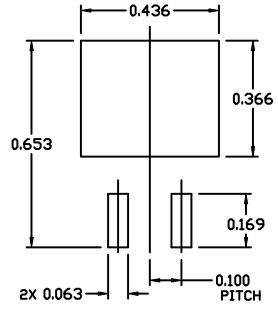

**Figure 15. Transient Thermal Response Curve**

# D²PAK–3 (TO–263, 3–LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021



**SCALE 1:1**



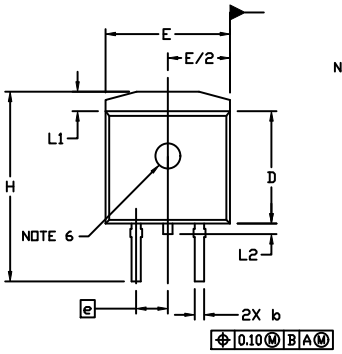

RECOMMENDED
MOUNTING FOOTPRINT

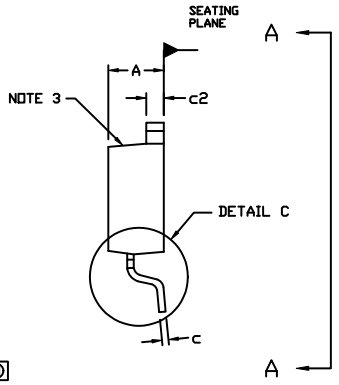
* For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

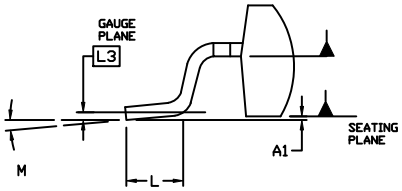
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② … OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

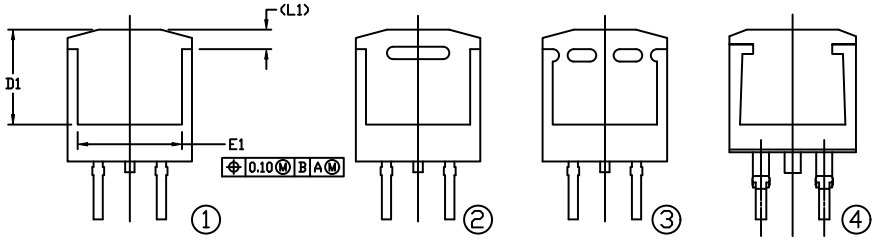
| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN. | MAX. | MIN. | MAX. |
| A | 0.160 | 0.190 | 4.06 | 4.83 |
| A1 | 0.000 | 0.010 | 0.00 | 0.25 |
| b | 0.020 | 0.039 | 0.51 | 0.99 |
| c | 0.012 | 0.029 | 0.30 | 0.74 |
| c2 | 0.045 | 0.065 | 1.14 | 1.65 |
| D | 0.330 | 0.380 | 8.38 | 9.65 |
| D1 | 0.260 | --- | 6.60 | --- |
| E | 0.380 | 0.420 | 9.65 | 10.67 |
| E1 | 0.245 | --- | 6.22 | --- |
| e | 0.100 BSC | | 2.54 BSC | |
| H | 0.575 | 0.625 | 14.60 | 15.88 |
| L | 0.070 | 0.110 | 1.78 | 2.79 |
| L1 | --- | 0.066 | --- | 1.68 |
| L2 | --- | 0.070 | --- | 1.78 |
| L3 | 0.010 BSC | | 0.25 BSC | |
| M | 0° | 8° | 0° | 8° |



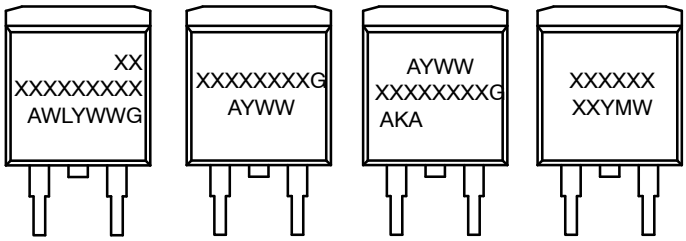

DETAIL C
TIP LEADFORM
ROTATED 90° CW




VIEW A–A

VIEW A–A
OPTIONAL CONSTRUCTIONS

## GENERIC MARKING DIAGRAMS*




**IC** **Standard** **Rectifier** **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb–Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON56370E** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **D²PAK–3 (TO–263, 3–LEAD)** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales