LDO Linear Voltage Regulator - Ultra-Low Quiescent Current, Ultra-Low Noise

200 mA

NCV8702

The NCV8702 is a low noise, low power consumption and low dropout Linear Voltage Regulator. With its excellent noise and PSRR specifications, the device is ideal for use in products utilizing RF receivers, imaging sensors, audio processors or any component requiring an extremely clean power supply. The NCV8702 uses an innovative Adaptive Ground Current circuit to ensure ultra low ground current during light load conditions.

Features

- Operating Input Voltage Range: 2.0 V to 5.5 V
- Available in Fixed Voltage Options: 0.8 to 3.5 V in 2.5 mV steps Contact Factory for Other Voltage Options
- Ultra−Low Quiescent Current of Typ. 10 μA
- Ultra−Low Noise: 11 μV_{RMS} from 100 Hz to 100 kHz
- Very Low Dropout: 140 mV Typical at 200 mA
- ±2% Accuracy Over Full Load/Line/Temperature
- High PSRR: 68 dB at 1 kHz
- Thermal Shutdown and Current Limit Protections
- Internal Soft−Start to Limit the Turn−On Inrush Current
- Stable with a 1 μF Ceramic Output Capacitor
- Available in TSOP−5 and XDFN 1.5 x 1.5 mm Package
- Active Output Discharge for Fast Output Turn−Off
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Satellite Radio Receivers, GPS
- Rear View Camera, Electronic Mirrors, Lane Change Detectors
- Portable Entertainment Systems
- Other Battery Powered Applications

Figure 1. Typical Application Schematic

TSOP−5
SN SUFFIX
CASE 483

XDFN−6
MX SUFFIX
CASE 711AE

MARKING DIAGRAMS

X, XXX = Specific Device Code
M = Date Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS

5−Pin TSOP−5
(Top View)

6−Pin XDFN 1.5 x 1.5 mm
(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information on page 18 of this data sheet.

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Figure 2. Simplified Schematic Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No. XDFN 6	Pin No. TSOP−5	Pin Name	Description
1	5	OUT	Regulated output voltage pin. A small 1 μF ceramic capacitor is needed from this pin to ground to assure stability.
2	4	N/C	Not connected. This pin can be tied to ground to improve thermal dissipation.
3	2	GND	Power supply ground.
4	3	EN	Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
5		N/C	Not connected. This pin can be tied to ground to improve thermal dissipation.
6	1	IN	Input pin. It is recommended to connect a 1 μF ceramic capacitor close to the device pin.

Table 2. ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	−0.3 V to 6 V	V
Output Voltage	V_{OUT}	−0.3 V to V_{IN} + 0.3 V	V
Enable Input	V_{EN}	−0.3 V to V_{IN} + 0.3 V	V
Output Short Circuit Duration	t_{SC}	Indefinite	s
Maximum Junction Temperature	$T_{J(MAX)}$	125	°C
Storage Temperature	T_{STG}	−55 to 150	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

Table 3. THERMAL CHARACTERISTICS (Note 3)

Rating	Symbol	Value	Unit
Thermal Characteristics, TSOP−5, Thermal Resistance, Junction−to−Air Thermal Characterization Parameter, Junction−to−Lead (Pin 2)	 θ_{JA} ψ_{JA}	 224 115	°C/W
Thermal Characteristics, XDFN6 1.5 x 1.5 mm Thermal Resistance, Junction−to−Air Thermal Characterization Parameter, Junction−to−Board	 θ_{JA} ψ_{JB}	 149 81	°C/W

3. Single component mounted on 1 oz, FR4 PCB with 645 mm^2 Cu area.

Table 4. ELECTRICAL CHARACTERISTICS
(−40°C ≤ T_J ≤ 125°C; V_{IN} = $V_{OUT(NOM)}$ + 0.3 V or 2.0 V, whichever is greater; V_{EN} = 0.9 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 μF. Typical values are at T_J = +25°C. Min/Max values are specified for T_J = −40°C and T_J = 125°C respectively.) (Note 4)

Parameter	Test Conditions		Symbol	Min	Typ	Max	Unit
Operating Input Voltage			V_{IN}	2.0		5.5	V
Undervoltage lock−out	V_{IN} rising		UVLO	1.2	1.6	1.9	V
Output Voltage Accuracy	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 0 − 200 mA		V_{OUT}	−2		+2	%
Line Regulation	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 4.5 V, I_{OUT} = 10 mA		Reg_{LINE}		290		μV/V
	V_{OUT} + 0.3 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA		Reg_{LINE}		440		μV/V
Load Regulation	I_{OUT} = 0 mA to 200 mA		Reg_{LOAD}		13		μV/mA
Dropout voltage (Note 5)	I_{OUT} = 200 mA, $V_{OUT(nom)}$ = 2.5 V		V_{DO}		140	200	mV
Output Current Limit	V_{OUT} = 90% $V_{OUT(nom)}$		I_{CL}	220	385	550	mA
Quiescent current	I_{OUT} = 0 mA		I_Q		10	16	μA
Ground current	I_{OUT} = 2 mA		I_{GND}		60		μA
	I_{OUT} = 200 mA		I_{GND}		160		μA
Shutdown current (Note 6)	V_{EN} ≤ 0.4 V		I_{DIS}		0.005		μA
	V_{EN} ≤ 0.4 V, V_{IN} = 4.5 V		I_{DIS}		0.01	1	μA
EN Pin Threshold Voltage High Threshold Low Threshold	 V_{EN} Voltage increasing V_{EN} Voltage decreasing		 V_{EN_HI} V_{EN_LO}	 0.9		 0.4	V
EN Pin Input Current	V_{EN} = V_{IN} = 5.5 V		I_{EN}		110	500	nA
Turn−On Time (Note 7)	C_{OUT} = 1.0 μF, I_{OUT} = 1 mA		t_{ON}		300		μs
Output Voltage Overshoot on Start−up (Note 8)	V_{EN} = 0 V to 0.9 V, 0 ≤ I_{OUT} ≤ 200 mA		ΔV_{OUT}			2	%
Load Transient	I_{OUT} = 1 mA to 200 mA or I_{OUT} = 200 mA to 1 mA in 10 μs, C_{OUT} = 1 μF		ΔV_{OUT}		−30/+30		mV
Power Supply Rejection Ratio	V_{IN} = 3 V, V_{OUT} = 2.5 V I_{OUT} = 150 mA	f = 100 Hz f = 1 kHz f = 10 kHz	PSRR		70 68 53		dB
Output Noise Voltage	V_{OUT} = 2.5 V, V_{IN} = 3 V, I_{OUT} = 200 mA f = 100 Hz to 100 kHz		V_N		11		μV_{rms}
Active Discharge Resistance	V_{EN} < 0.4 V		R_{DIS}		1		kΩ
Thermal Shutdown Temperature	Temperature increasing from T_J = +25°C		T_{SD}		160		°C
Thermal Shutdown Hysteresis	Temperature falling from T_{SD}		T_{SDH}	−	20	−	°C

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at T_J = T_A = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
5. Characterized when V_{OUT} falls 100 mV below the regulated voltage at V_{IN} = $V_{OUT(NOM)}$ + 0.3 V.
6. Shutdown Current is the current flowing into the IN pin when the device is in the disable state.
7. Turn−On time is measured from the assertion of EN pin to the point when the output voltage reaches 0.98 $V_{OUT(NOM)}$
8. Guaranteed by design.

TYPICAL CHARACTERISTICS

I_{OUT}	RMS Output Noise	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	21.74	21.17
10 mA	14.62	14.07
200 mA	10.74	10.02

Figure 3. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 1 μF

I_{OUT}	RMS Output Noise	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	14.16	13.43
10 mA	14.20	13.70
200 mA	10.99	10.48

Figure 4. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 4.7 μF

I_{OUT}	RMS Output Noise	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	12.94	12.11
10 mA	12.78	12.25
200 mA	11.33	10.83

Figure 5. Output Voltage Noise Spectral Density for V_{OUT} = 0.8 V, C_{OUT} = 10 μF

TYPICAL CHARACTERISTICS

I_{OUT}	RMS Output Noise	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	20.28	17.87
10 mA	16.73	13.90
200 mA	13.70	10.21

Figure 6. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 1 μF

I_{OUT}	RMS Output Noise	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	15.76	11.82
10 mA	17.09	13.88
200 mA	14.51	11.47

Figure 7. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 4.7 μF

I_{OUT}	RMS Output Noise	
	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	14.87	10.57
10 mA	16.00	12.65
200 mA	14.89	11.84

Figure 8. Output Voltage Noise Spectral Density for V_{OUT} = 3.3 V, C_{OUT} = 10 μF

TYPICAL CHARACTERISTICS

Figure 9. Power Supply Rejection Ratio, V_{OUT} = 0.8 V, C_{OUT} = 1 μF

Figure 10. Power Supply Rejection Ratio, V_{OUT} = 0.8 V, C_{OUT} = 4.7 μF

Figure 11. Power Supply Rejection Ratio, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

Figure 12. Power Supply Rejection Ratio, V_{OUT} = 3.3 V, C_{OUT} = 4.7 μF

Figure 13. Power Supply Rejection Ratio, V_{OUT} = 3.3 V, C_{OUT} = 10 μF

Figure 14. PSRR vs. Voltage Differential, C_{OUT} = 4.7 μF, I_{OUT} = 200 mA

TYPICAL CHARACTERISTICS

Figure 15. PSRR vs. Voltage Differential, C_{OUT} = 4.7 μF, I_{OUT} = 10 mA

Figure 16. Quiescent Current vs. Input Voltage, V_{OUT} = 3.3 V

Figure 17. Quiescent Current vs. Input Voltage, V_{OUT} = 0.8 V

Figure 18. Dropout Voltage vs. Output Current, V_{OUT} = 3.3 V

Figure 19. Dropout Voltage vs. Output Current, V_{OUT} = 2.5 V

Figure 20. Output Voltage vs. Temperature, V_{OUT} = 0.8 V

TYPICAL CHARACTERISTICS

Figure 21. Output Voltage vs. Temperature, V_{OUT} = 1.8 V

Figure 22. Output Voltage vs. Temperature, V_{OUT} = 3.3 V

Figure 23. Load Regulation vs. Temperature, V_{OUT} = 0.8 V

Figure 24. Load Regulation vs. Temperature, V_{OUT} = 1.8 V

Figure 25. Load Regulation vs. Temperature, V_{OUT} = 3.3 V

Figure 26. Line Regulation vs. Temperature, V_{OUT} = 0.8 V

TYPICAL CHARACTERISTICS

Figure 27. Line Regulation vs. Temperature, V_{OUT} = 1.8 V

Figure 28. Line Regulation vs. Temperature, V_{OUT} = 3.3 V

Figure 29. Disable Current vs. Temperature, V_{OUT} = 1.8 V

Figure 30. Disable Current vs. Temperature, V_{OUT} = 3.3 V

Figure 31. Disable Current vs. Temperature, V_{OUT} = 0.8 V

Figure 32. Output Current Limit vs. Temperature, V_{OUT} = 0.8 V

TYPICAL CHARACTERISTICS

Figure 33. Output Current Limit vs. Temperature, V_{OUT} = 3.3 V

Figure 34. Enable Low Threshold Voltage

Figure 35. Enable High Threshold Voltage

Figure 36. Enable Turn−On Response, V_{OUT} = 3.3 V, C_{OUT} = 1 μF

Figure 37. Enable Turn−On Response, V_{OUT} = 3.3 V, C_{OUT} = 3 μF

Figure 38. Enable Turn−On Response, V_{OUT} = 0.8 V, C_{OUT} = 1 μF

TYPICAL CHARACTERISTICS

Figure 39. Enable Turn−On Response, V_{OUT} = 0.8 V, C_{OUT} = 3 µF

Figure 40. Turn−On Inrush Current vs. Output Capacitance

Figure 41. Enable Turn−Off Response, V_{OUT} = 3.3 V, C_{OUT} = 1 µF

Figure 42. Enable Turn−Off Response, V_{OUT} = 3.3 V, C_{OUT} = 4.7 µF

Figure 43. Enable Turn−Off Response, V_{OUT} = 3.3 V, C_{OUT} = 10 µF

Figure 44. Slow Input Voltage Turn−On/Turn−Off, V_{OUT} = 3.3 V

TYPICAL CHARACTERISTICS

Figure 45. Line Transient Response – Rising Edge, V_{OUT} = 3.3 V

Figure 46. Line Transient Response – Falling Edge, V_{OUT} = 3.3 V

Figure 47. Load Transient Response – Rising Edge, I_{OUT} = 1 mA – 200 mA, V_{OUT} = 0.8 V

Figure 48. Load Transient Response – Falling Edge, I_{OUT} = 1 mA – 200 mA, V_{OUT} = 0.8 V

Figure 49. Load Transient Response – Rising Edge, I_{OUT} = 1 mA – 200 mA, C_{OUT} = 1.0 µF

Figure 50. Load Transient Response – Falling Edge, I_{OUT} = 1 mA – 200 mA, C_{OUT} = 1.0 µF

TYPICAL CHARACTERISTICS

Figure 51. Load Transient Response – Rising Edge, I_{OUT} = 1 mA – 200 mA, C_{OUT} = 4.7 μF

Figure 52. Load Transient Response – Falling Edge, I_{OUT} = 1 mA – 200 mA, C_{OUT} = 4.7 μF

Figure 53. Load Transient Response – Rising Edge, I_{OUT} = 1 mA – 200 mA, C_{OUT} = 10 μF

Figure 54. Load Transient Response – Falling Edge, I_{OUT} = 1 mA – 200 mA, C_{OUT} = 10 μF

Figure 55. Output Short Circuit Response

Figure 56. Cycling between Output Short Circuit and Thermal Shutdown

TYPICAL CHARACTERISTICS

Figure 57. Ground Current vs. Output Current, I_{OUT} = 0 mA to 5 mA

Figure 58. Ground Current vs. Output Current, I_{OUT} = 0 mA to 200 mA

Figure 59. EN Pin Input Current vs. Enable Pin Voltage

Figure 60. Output Capacitor ESR vs. Output Current

APPLICATIONS INFORMATION

General

The NCV8702 is a high performance 200 mA Low Dropout Linear Regulator. This device delivers excellent noise and dynamic performance.

Thanks to its adaptive ground current feature the device consumes only 10 μA of quiescent current at no−load condition.

The regulator features ultra−low noise of 11 μV_{RMS}, PSRR of 68 dB at 1 kHz and very good load/line transient performance. Such excellent dynamic parameters and small package size make the device an ideal choice for powering the precision analog and noise sensitive circuitry in portable applications. The LDO achieves this ultra low noise level output without the need for a noise bypass capacitor.

A logic EN input provides ON/OFF control of the output voltage. When the EN is low the device consumes as low as typ. 10 nA from the IN pin.

The LDO achieves ultra−low output voltage noise without the need for additional noise bypass capacitor.

The device is fully protected in case of output overload, output short circuit condition and overheating, assuring a very robust design.

Input Capacitor Selection (C_{IN})

It is recommended to connect a minimum of 1 μF Ceramic X5R or X7R capacitor close to the IN pin of the device. This capacitor will provide a low impedance path for unwanted AC signals or noise modulated onto constant input voltage.

There is no requirement for the min./max. ESR of the input capacitor but it is recommended to use ceramic capacitors for their low ESR and ESL. A good input capacitor will limit the influence of input trace inductance and source resistance during sudden load current changes.

Larger input capacitor may be necessary if fast and large load transients are encountered in the application.

Output Decoupling (C_{OUT})

The NCV8702 is designed to be stable with a small 1.0 μF ceramic capacitor on the output. To assure proper operation it is strongly recommended to use min. 1.0 μF capacitor with the initial tolerance of ±10%, made of X7R or X5R dielectric material types.

There is no requirement for the minimum value of Equivalent Series Resistance (ESR) for the C_{OUT} but the maximum value of ESR should be less than 700 mΩ.

Larger output capacitors could be used to improve the load transient response or high frequency PSRR as shown in typical characteristics. The initial tolerance requirements can be wider than ±10% when using capacitors larger than 1 μF.

It is not recommended to use tantalum capacitors on the output due to their large ESR. The equivalent series resistance of tantalum capacitors is also strongly dependent on the temperature, increasing at low temperature. The tantalum capacitors are generally more costly than ceramic capacitors.

The table on this page lists the capacitors which were used during the IC evaluation.

No−load Operation

The regulator remains stable and regulates the output voltage properly within the ±2% tolerance limits even with no external load applied to the output.

Figure 61. Typical Applications Schematics

LIST OF RECOMMENDED CAPACITORS:

Symbol	Manufacturer	Part Number	Description
C1, C2	Kemet	C0402C105K8PACTU	1 μF Ceramic ±10%, 10 V, 0402, X5R
	TDK	C1005X5R1A105K	−‖−
	Murata	GRM155R61A105KE15D	−‖−
	AVX	0402ZD105KAT2A	−‖−
	Multicomp	MCCA000571	1 μF Ceramic ±10%, 50 V, 1206, X7R
	Panason − ECG	ECJ−0EB0J475M	4.7 μF Ceramic ±20%, 6.3 V, 0402, X5R

APPLICATIONS INFORMATION

Enable Operation

The NCV8702 uses the EN pin to enable/disable its output and to deactivate/activate the active discharge function.

If the EN pin voltage is <0.4 V the device is guaranteed to be disabled. The pass transistor is turned−off so that there is virtually no current flow between the IN and OUT. The active discharge transistor is active so that the output voltage V_{OUT} is pulled to GND through a 1 kΩ resistor. In the disable state the device consumes as low as typ. 10 nA from the V_{IN}.

If the EN pin voltage >0.9 V the device is guaranteed to be enabled. The NCV8702 regulates the output voltage and the active discharge transistor is turned−off.

The EN pin has internal pull−down current source with typ. value of 110 nA which assures that the device is turned−off when the EN pin is not connected. A build in 2 mV of hysteresis in the EN prevents from periodic on/off oscillations that can occur due to noise.

In the case where the EN function isn't required the EN pin should be tied directly to IN.

Undervoltage Lockout

The internal UVLO circuitry assures that the device becomes disabled when the V_{IN} falls below typ. 1.5 V. When the V_{IN} voltage ramps−up the NCV8702 becomes enabled, if V_{IN} rises above typ. 1.6 V. The 100 mV hysteresis prevents on/off oscillations that can occur due to noise on V_{IN} line.

Reverse Current

The PMOS pass transistor has an inherent body diode which will be forward biased in the case that $V_{OUT} > V_{IN}$. Due to this fact in cases where the extended reverse current condition is anticipated the device may require additional external protection.

Output Current Limit

Output Current is internally limited within the IC to a typical 380 mA. The NCV8702 will source this amount of current measured with the output voltage 100 mV lower than the nominal V_{OUT}. If the Output Voltage is directly shorted to ground (V_{OUT} = 0 V), the short circuit protection will limit the output current to 390 mA (typ). The current limit and short circuit protection will work properly up to V_{IN} = 5.5 V at T_A = 25°C. There is no limitation for the short circuit duration.

Thermal Shutdown

When the die temperature exceeds the Thermal Shutdown threshold (T_{SD} − 160°C typical), Thermal Shutdown event is detected and the device is disabled. The IC will remain in this state until the die temperature decreases below the Thermal Shutdown Reset threshold (T_{SDU} − 140°C typical). Once the IC temperature falls below the 140°C the LDO is enabled again. The thermal shutdown feature provides protection from a catastrophic device failure due to accidental overheating. This protection is not intended to be used as a substitute for proper heat sinking.

Power Dissipation

As power dissipated in the NCV8702 increases, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and the ambient temperature affect the rate of junction temperature rise for the part.

The maximum power dissipation the NCV8702 can handle is given by:

$$P_{D(MAX)} = \frac{\left[T_{J(MAX)} - T_A\right]}{\theta_{JA}} \quad \text{(eq. 1)}$$

The power dissipated by the NCV8702 for given application conditions can be calculated from the following equations:

$$P_D \approx V_{IN}\left(I_{GND}@I_{OUT}\right) + I_{OUT}\left(V_{IN} - V_{OUT}\right) \quad \text{(eq. 2)}$$

Figure 62. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (TSOP5)

Figure 63. θ_{JA} and $P_{D(MAX)}$ vs. Copper Area (XDFN6)

Load Regulation

The NCV8702 features very good load regulation of maximum 2.6 mV in the 0 mA to 200 mA range. In order to achieve this very good load regulation a special attention to PCB design is necessary. The trace resistance from the OUT pin to the point of load can easily approach 100 mΩ which will cause a 20 mV voltage drop at full load current, deteriorating the excellent load regulation.

Line Regulation

The IC features very good line regulation of 0.44 mV/V measured from $V_{IN} = V_{OUT} + 0.3$ V to 5.5 V. For battery operated applications it may be important that the line regulation from $V_{IN} = V_{OUT} + 0.3$ V up to 4.5 V is only 0.29 mV/V.

Power Supply Rejection Ratio

The NCV8702 features very good Power Supply Rejection ratio. If desired the PSRR at higher frequencies in the range 100 kHz – 10 MHz can be tuned by the selection of C_{OUT} capacitor and proper PCB layout.

Output Noise

The IC is designed for ultra−low noise output voltage. Figures 3 – 8 illustrate the noise performance for different V_{OUT}, I_{OUT}, C_{OUT}. Generally the noise performance in the indicated frequency range improves with increasing output current, although even at $I_{OUT} = 1$ mA the noise levels are below 22 μV_{RMS}.

Turn−On Time

The turn−on time is defined as the time period from EN assertion to the point in which V_{OUT} will reach 98% of its nominal value. This time is dependent on $V_{OUT(NOM)}$, C_{OUT}, T_A. The turn−on time temperature dependence is shown below:

Figure 64. Turn−On Time vs. Temperature

Internal Soft-Start

The Internal Soft−Start circuitry will limit the inrush current during the LDO turn-on phase. Please refer to Figure 43 for typical inrush current values for given output capacitance.

The soft−start function prevents from any output voltage overshoots and assures monotonic ramp-up of the output voltage.

PCB Layout Recommendations

To obtain good transient performance and good regulation characteristics place C_{IN} and C_{OUT} capacitors close to the device pins and make the PCB traces wide. In order to minimize the solution size use 0402 capacitors. Larger copper area connected to the pins will also improve the device thermal resistance. The actual power dissipation can be calculated by the formula given in Equation 2.

ORDERING INFORMATION

Device*	Voltage Option	Marking	Package	Shipping†
NCV8702MX18TCG	1.8 V	P	XDFN6 (Pb−Free)	3000 or 5000 / Tape & Reel (Note 9)
NCV8702MX25TCG	2.5 V	V		
NCV8702MX28TCG (Note 9)	2.8 V	2		
NCV8702MX30TCG (Note 9)	3.0 V	3		
NCV8702MX33TCG	3.3 V	4		
NCV8702SN18T1G	1.8 V	A5J	TSOP-5 (Pb−Free)	3000 / Tape & Reel
NCV8702SN28T1G	2.8 V	ADV		
NCV8702SN30T1G	3.0 V	A5R		
NCV8702SN33T1G	3.3 V	A5T		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

9. Products processed after October 1, 2022 are shipped with quantity 5000 units / tape & reel.

TSOP−5 3.00x1.50x0.95, 0.95P
CASE 483
ISSUE P

DATE 01 APR 2024

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS (ANGLES IN DEGREES).
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OF GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSION D.
5. OPTIONAL CONSTRUCTION: AN ADDITIONAL TRIMMED LEAD IS ALLOWED IN THIS LOCATION. TRIMMED LEAD NOT TO EXTEND MORE THAN 0.2 FROM BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.900	1.000	1.100
A1	0.010	0.055	0.100
A2	0.950 REF.		
b	0.250	0.375	0.500
c	0.100	0.180	0.260
D	2.850	3.000	3.150
E	2.500	2.750	3.000
E1	1.350	1.500	1.650
e	0.950 BSC		
L	0.200	0.400	0.600
θ	0°	5°	10°

RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

Analog

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

Discrete/Logic

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	98ARB18753C	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TSOP−5 3.00x1.50x0.95, 0.95P	PAGE 1 OF 1

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SCALE 4:1

XDFN6 1.5x1.5, 0.5P
CASE 711AE
ISSUE B

DATE 27 AUG 2015

TOP VIEW

SIDE VIEW

DETAIL A
ALTERNATE TERMINAL CONSTRUCTIONS

DETAIL B
ALTERNATE CONSTRUCTIONS

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20mm FROM TERMINAL TIP.

DIM	MILLIMETERS MIN	MAX
A	0.35	0.45
A1	0.00	0.05
A3	0.13 REF	
b	0.20	0.30
D	1.50 BSC	
E	1.50 BSC	
e	0.50 BSC	
L	0.40	0.60
L1	---	0.15
L2	0.50	0.70

BOTTOM VIEW

GENERIC MARKING DIAGRAM*

XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

RECOMMENDED MOUNTING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	XDFN6, 1.5 X 1.5, 0.5 P	PAGE 1 OF 1

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