NCV8665

Linear Regulator - Low Dropout, Very Low Iq, Reset, Delay Reset

150 mA

The NCV8665 is a precision 5.0 V fixed output, low dropout integrated voltage regulator with an output current capability of 150 mA. Careful management of light load current consumption, combined with a low leakage process, achieve a typical quiescent ground current of 30 μA.

NCV8665 is pin for pin compatible with the NCV8675 and the NCV4275 and it could replace this part when lower output current, and very low quiescent current is required.

The output voltage is accurate within ±2.0%, and maximum dropout voltage is 600 mV at full rated load current.

It is internally protected against 45 V input transients, input supply reversal, output overcurrent faults, and excess die temperature. No external components are required to enable these features.

Features

- 5 V Fixed Output (3.3 V and 2.5 V Versions are Also Available)
- ±2.0% Output Accuracy, Over Full Temperature Range
- 40 μA Maximum Quiescent Current at I_{OUT} = 100 μA
- 600 mV Maximum Dropout Voltage at 150 mA Load Current
- Wide Input Voltage Operating Range of 5.5 V to 45 V
- Internal Fault Protection
  - −42 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- These are Pb−Free Devices

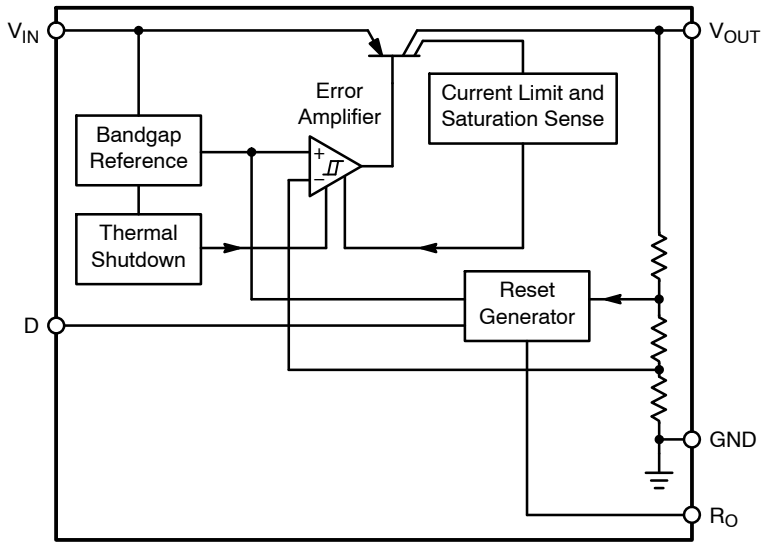
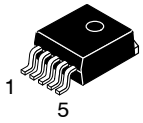


Figure 1. Block Diagram

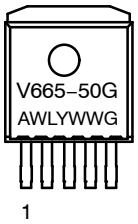
ON Semiconductor®

http://onsemi.com

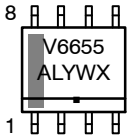
MARKING DIAGRAMS



D²PAK 5−PIN DS SUFFIX CASE 936A



SOIC−8 D SUFFIX CASE 751



A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G or ▪	= Lead Free Indicator

PIN CONNECTIONS

	D²PAK		SOIC−8
Pin	1. V_{IN}	Pin	1. V_{IN}
	2. RO		2. RO
Tab,	3. GND*		3. D
	4. D		4. V_{OUT}
	5. V_{OUT}		5−8. GND

* Tab is connected to Pin 3

ORDERING INFORMATION

See detailed ordering and shipping information in the dimensions section on page 9 of this data sheet.

PIN DESCRIPTIONS

Symbol	Function
V_{IN}	Unregulated input voltage; 5.5 V to 45 V; Battery Input Voltage. Bypass to GND with a 0.1 μF ceramic capacitor.
R_O	Reset Output; open collector active Reset (Accurate when V_{OUT} > 1.0 V)
GND	Ground; Pin 3 internally connected to Tab
D	Reset Delay; timing capacitor to GND for Reset Delay function
V_{OUT}	Output; ±2.0%, 150 mA. 10 μF, ESR < 16 Ω

ABSOLUTE MAXIMUM RATINGS

Pin Symbol, Parameter	Symbol	Min	Max	Unit
V_{IN}, DC Input Voltage	V_{IN}	−42	+45	V
V_{OUT}, DC Voltage	V_{OUT}	−0.3	+16	V
Reset Output Voltage	V_{RO}	−0.3	25	V
Reset Output Current	I_{RO}	−5.0	5.0	mA
Reset Delay Voltage	V_D	−0.3	7.0	V
Reset Delay Current	I_D	−2.0	2.0	mA
Storage Temperature	T_{STG}	−55	+150	°C
ESD Capability, Human body Model (Note 1)	V_{ESDHB}	4000		V
ESD Capability, Machine Model (Note 1)	V_{ESDMM}	200		V
Moisture Sensitivity Level	MSL	1		–

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model (HBM) tested per AEC−Q100−002 (EIA/JESD22−A 114C)
   ESD Machine Model (MM) tested per AEC−Q100−003 (EIA/JESD22−A 115C)
2. Latchup Current Maximum Rating: ≤ 100 mA per JEDEC standard: JESD78.

OPERATING RANGE

Pin Symbol, Parameter	Symbol	Min	Max	Unit
Input Voltage Operating Range	V_{IN}	5.5	45	V
Junction Temperature	T_J	−40	150	°C

THERMAL RESISTANCE

Parameter		Symbol	Min	Max	Unit
Junction to Ambient (Note 3)	D^2PAK	$R_{\theta JA}$	–	85.4	°C/W
Junction to Case (Note 3)	D^2PAK	$R_{\theta JC}$	–	6.8	
Junction to Ambient (Note 4)	SOIC−8	$R_{\theta JA}$	–	138	
Junction to Lead 6 (Note 4)	SOIC−8	$\Psi_{\theta JL6}$	–	21	

3. As mounted on a 35x35x1mm FR4 PCB with a single layer of 100 mm^2 of 1 oz copper heat spreading area.
4. As mounted on a 35x35x1mm FR4 PCB with a single layer of 100 mm^2 of 1 oz copper heat spreading area including traces directly connected to the leads.

Pb SOLDERING TEMPERATURE AND MSL

Parameter	Symbol	Min	Max	Unit
Lead Temperature Soldering Reflow (SMD styles only), Pb−Free (Note 5)	T_{sld}	–	265 pk	°C
MSL, 8−Lead EP, LS Temperature 260°C	MSL	1		–

5. This device series incorporates ESD protection and exceeds the following ratings:
   Human Body Model (HBM) ≤ 2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) ≤ 200 V per JEDEC standard: JESD22−A115.

ELECTRICAL CHARACTERISTICS V_{IN} = 13.5 V, T_J = −40°C to +150°C, unless otherwise specified

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
OUTPUT						
Output Voltage	V_{OUT}	0.1 mA ≤ I_{OUT} ≤ 150 mA (Note 6) 6 V ≤ V_{IN} ≤ 28 V	4.900	5.000	5.100	V
Output Voltage	V_{OUT}	0 mA ≤ I_{OUT} ≤ 150 mA 5.5 V ≤ V_{IN} ≤ 28 V −40°C ≤ T_J ≤ 125°C	4.900	5.000	5.100	V
Line Regulation	ΔV_{OUT} versus V_{IN}	I_{OUT} = 5 mA 8 V ≤ V_{IN} ≤ 32 V	−25	5	+25	mV
Load Regulation	ΔV_{OUT} Vs. I_{OUT}	1 mA ≤ I_{OUT} ≤ 150 mA (Note 6)	−35	5	+35	mV
Dropout Voltage	$V_{IN} - V_{OUT}$	I_{OUT} = 100 mA (Notes 6 and 7) I_{OUT} = 150 mA (Notes 6 and 7)		200 250	500 600	mV
Quiescent Current	I_q	I_{OUT} = 100μA T_J = 25°C T_J = −40°C to +85°C		 30 30	 34 40	μA
Active Ground Current	$I_{G(ON)}$	I_{OUT} = 50 mA (Note 6) I_{OUT} = 150 mA (Note 6)		1.8 12	3.5 19	mA
Power Supply Rejection	PSRR	V_{RIPPLE} = 0.5 V_{PP}, F = 100 Hz		69		%/V
Output Capacitor for Stability	C_{OUT} ESR	I_{OUT} = 0.1 mA to 150 mA	10		 16	μF Ω
RESET TIMING D AND OUTPUT RO						
Reset Switching Threshold	$V_{OUT,rt}$	–	4.50	4.65	4.80	V
Reset Output Low Voltage	V_{ROL}	R_{Ext} > 5.0 k, V_{OUT} > 1.0 V	–	0.20	0.40	V
Reset Output Leakage Current	I_{ROH}	V_{ROH} = 5.0 V	–	0	10	μA
Reset Charging Current	$I_{D,C}$	V_D = 1.0 V	2.0	4.0	6.5	μA
Upper Timing Threshold	V_{DU}	–	1.2	1.3	1.4	V
Reset Delay Time	t_{rd}	C_D = 47 nF	10	16	22	ms
Reset Reaction Time	t_{rr}	C_D = 47 nF		1.5	4.0	μs
PROTECTION						
Current Limit	$I_{OUT(LIM)}$	V_{OUT} = 4.5 V (Note 6)	150		500	mA
Short Circuit Current Limit	$I_{OUT(SC)}$	V_{OUT} = 0 V (Note 6)	100		500	mA
Thermal shutdown threshold	T_{TSD}	(Note 8)	150		200	°C

6. Use pulse loading to limit power dissipation.
7. Dropout voltage = ($V_{IN} - V_{OUT}$), measured when the output voltage has dropped 100 mV relative to the nominal value obtained with V_{IN} = 13.5 V.
8. Not tested in production. Limits are guaranteed by design.

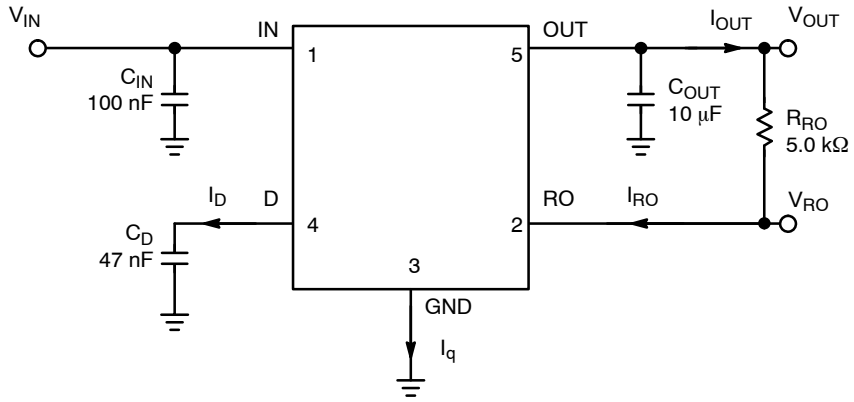


Figure 2. Application Circuit

TYPICAL CHARACTERISTIC CURVES

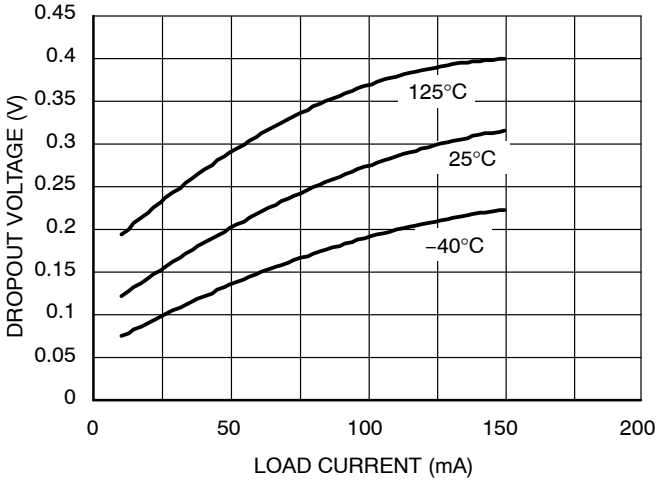


Figure 3. NCV8665 Dropout Voltage vs. Load Current

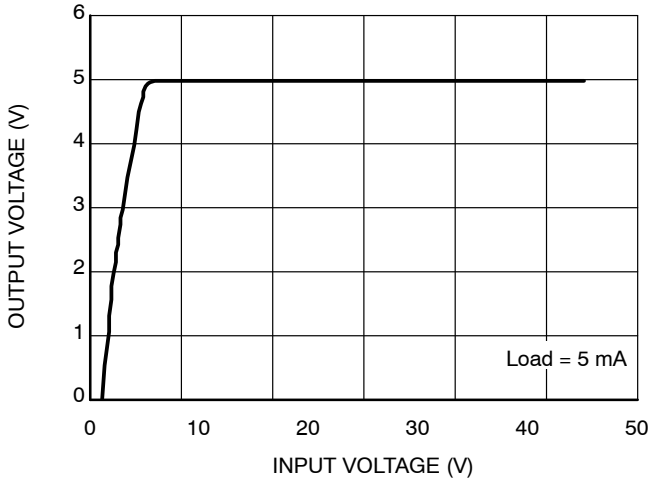


Figure 4. NCV8665 Input Voltage vs. Output Voltage (Full Range)

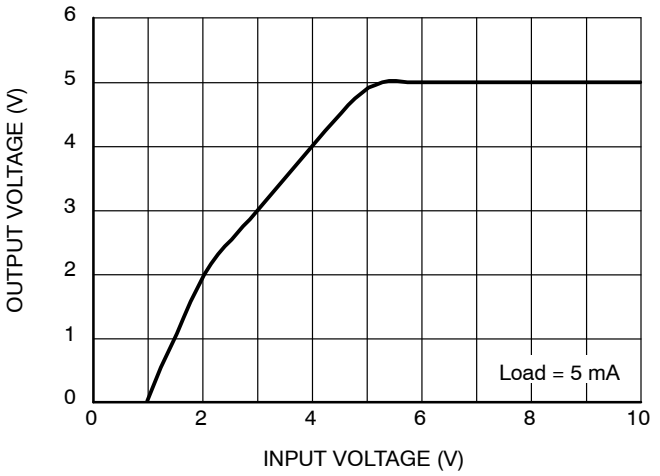


Figure 5. NCV8665 Input Voltage vs. Output Voltage (Low Voltage)

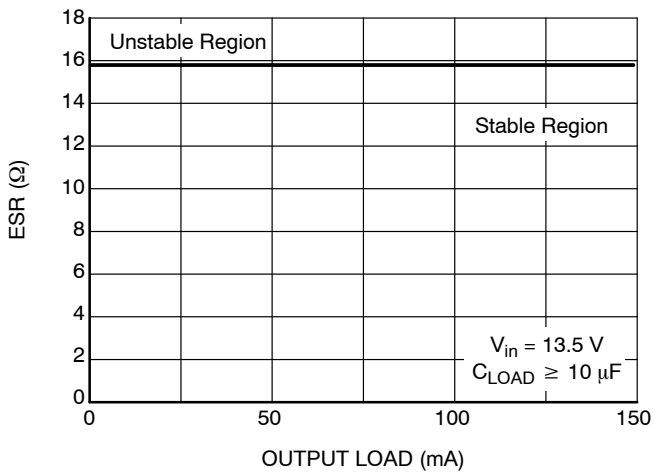


Figure 6. NCV8665 Stability Curve

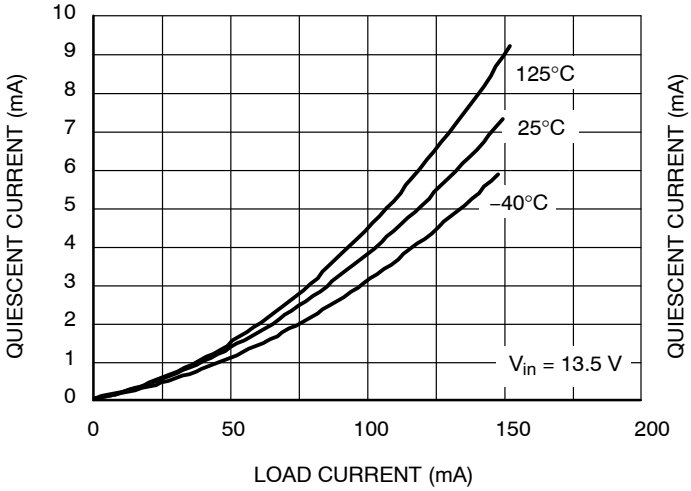


Figure 7. NCV8665 Quiescent Current vs. Load Current (Full Range)

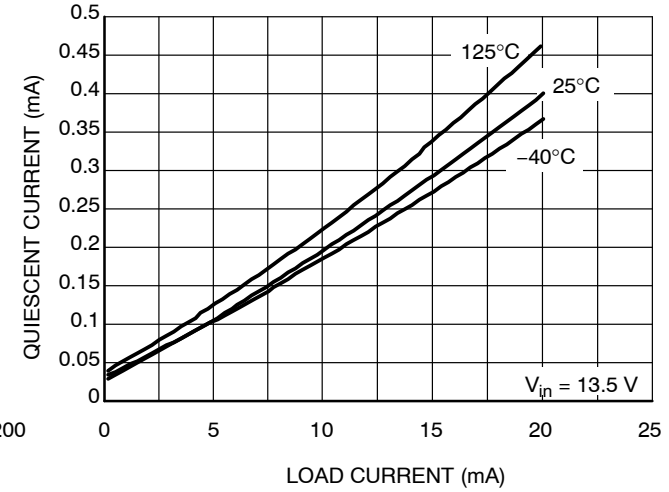


Figure 8. NCV8665 Quiescent Current vs. Load Current (Light Load)

TYPICAL CHARACTERISTIC CURVES

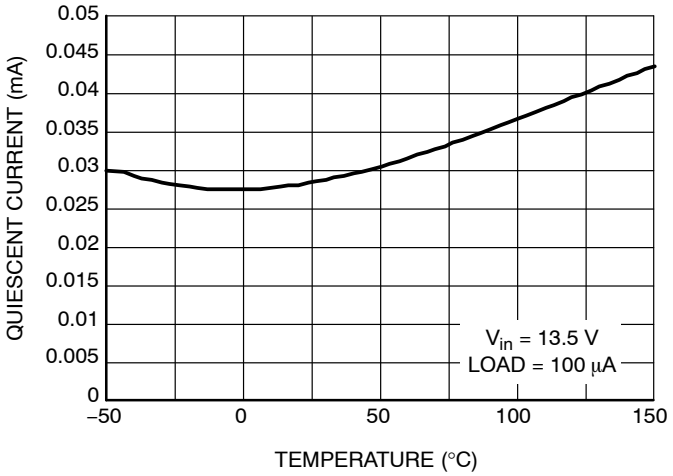


Figure 9. NCV8665 Quiescent Current vs. Temperature

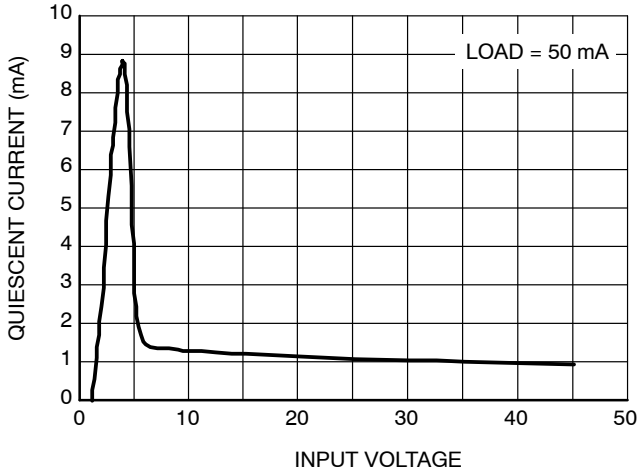


Figure 10. NCV8665 Quiescent Current vs. Input Voltage

Circuit Description

The NCV8665 is an integrated low dropout regulator that provides 5.0 V, 150 mA protected output and a signal for power on reset. The regulation is provided by a PNP pass transistor controlled by an error amplifier with a bandgap reference, which gives it the lowest possible drop out voltage and best possible temperature stability. The output current capability is 150 mA, and the base drive quiescent current is controlled to prevent over saturation when the input voltage is low or when the output is overloaded. The regulator is protected by both current limit and thermal shutdown. Thermal shutdown occurs above 150°C to protect the IC during overloads and extreme ambient temperatures. The delay time for the reset output is adjustable by selection of the timing capacitor. See Figure 2, Application Circuit, for circuit element nomenclature illustration.

Regulator

The error amplifier compares the reference voltage to a sample of the output voltage (V_{OUT}) and drives the base of a PNP series pass transistor by a buffer. The reference is a bandgap design to give it a temperature−stable output. Saturation control of the PNP is a function of the load current and input voltage. Oversaturation of the output power device is prevented, and quiescent current in the ground pin is minimized.

Regulator Stability Considerations

The input capacitor (C_{IN}) is necessary to stabilize the input impedance to avoid voltage line influences. The output capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability. The capacitor value and type should be based on cost, availability, size and temperature constraints. Tantalum, aluminum electrolytic, film, or ceramic capacitors are all acceptable solutions, however attention must be paid to ESR constraints. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the capacitance and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information. The value for the output capacitor C_{OUT} shown in Figure 2, Application Circuit, should work for most applications; however, it is not necessarily the optimized solution.

Reset Output

The reset output is used as the power on indicator to the microcontroller. This signal indicates when the output voltage is suitable for reliable operation of the controller. It pulls low when the output is not considered to be ready. RO is pulled up to V_{OUT} by an external resistor, typically 5.0 kΩ in value. The input and output conditions that control the Reset Output and the relative timing are illustrated in Figure 11, Reset Timing. Output voltage regulation must be maintained for the delay time before the reset output signals a valid condition. The delay for the reset output is defined as the amount of time it takes the timing capacitor on the delay pin to charge from a residual voltage of 0 V to the upper timing threshold voltage V_{DU} of 1.8 V. The charging current for this is I_D of 5.5 μA. By using typical IC parameters with a 47 nF capacitor on the D Pin, the following time delay is derived:

$t_{RD} = C_D * V_{DU} / I_D$

t_{RD} = 47 nF * (1.8 V) / 5.5 μA = 15.4 ms

Other time delays can be obtained by changing the C_D capacitor value.

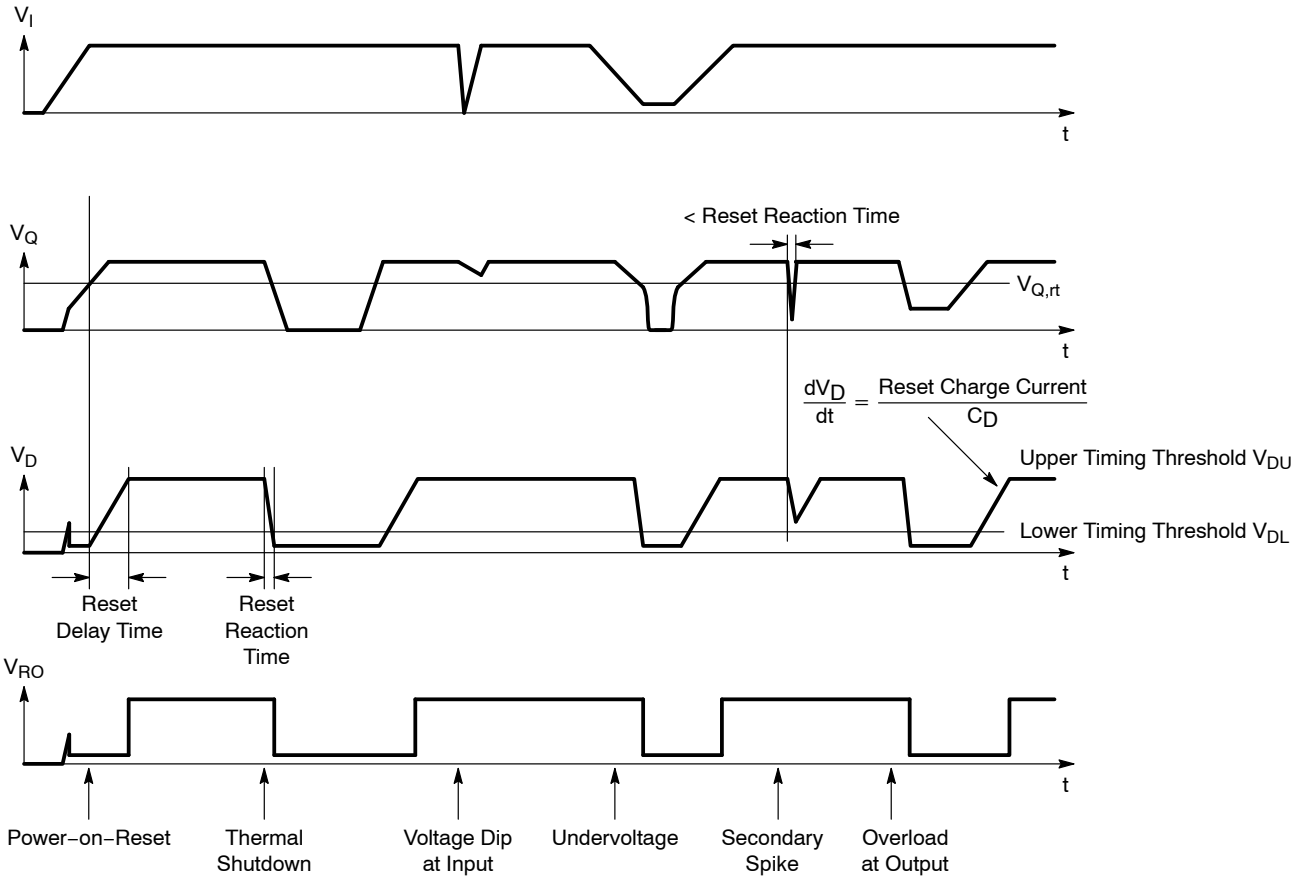


Figure 11. Reset Timing

Calculating Power Dissipation in a Single Output Linear Regulator

The maximum power dissipation for a single output regulator (Figure 12) is:

$$P_{D(max)} = [V_{I(max)} - V_{Q(min)}]I_{Q(max)} + V_{I(max)}I_q \quad (1)$$

where

$V_{I(max)}$ is the maximum input voltage,

$V_{Q(min)}$ is the minimum output voltage,

$I_{Q(max)}$ is the maximum output current for the application,

I_q is the quiescent current the regulator consumes at $I_{Q(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in Equation NO TAG will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

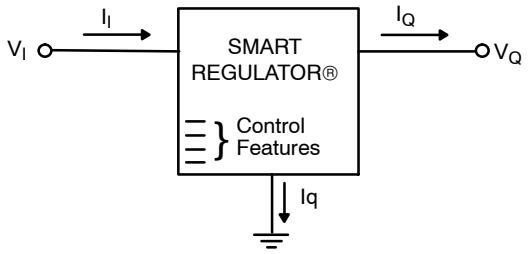


Figure 12. Single Output Regulator with Key Performance Parameters Labeled

Heatsinks

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where

$R_{\theta JC}$ is the junction−to−case thermal resistance,
$R_{\theta CS}$ is the case−to−heatsink thermal resistance,
$R_{\theta SA}$ is the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heatsink manufacturers.

Thermal, mounting, and heatsinking considerations are discussed in the ON Semiconductor application note AN1040/D.

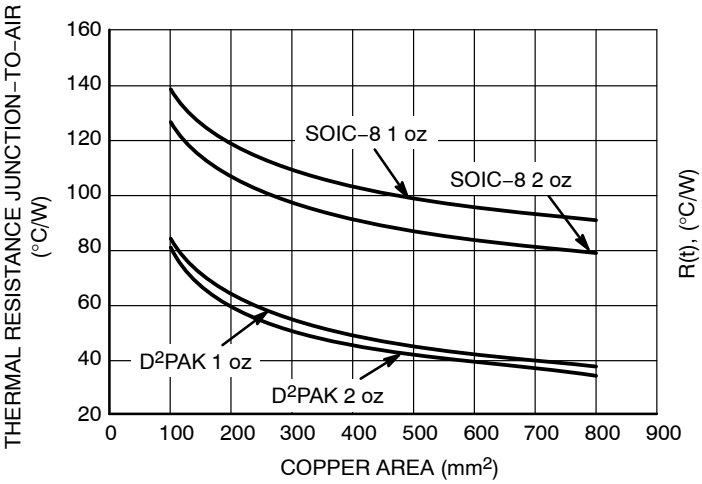


Figure 13. Thermal Resistance vs. PCB Area

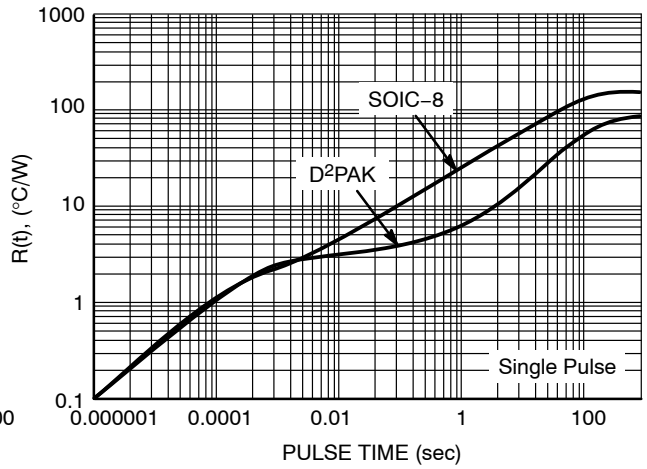


Figure 14. NCV8675 @ PCB Cu Area 100 mm² PCB Cu thk 1 oz

ORDERING INFORMATION

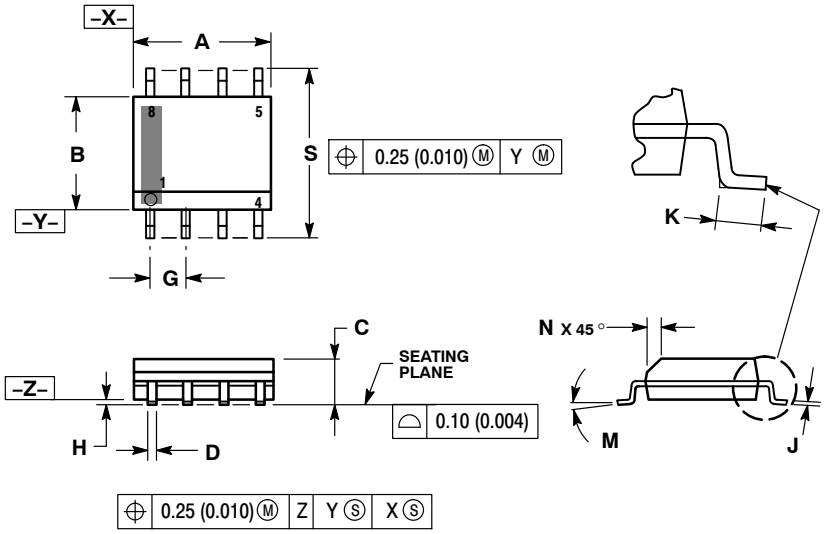
Device	Package	Shipping†
NCV8665DS50G	D2PAK (Pb−Free)	50 Units / Rail
NCV8665DS50R4G	D2PAK (Pb−Free)	800 / Tape & Reel
NCV8665D50G	SOIC−8 (Pb−Free)	98 Units / Rail
NCV8665D50R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

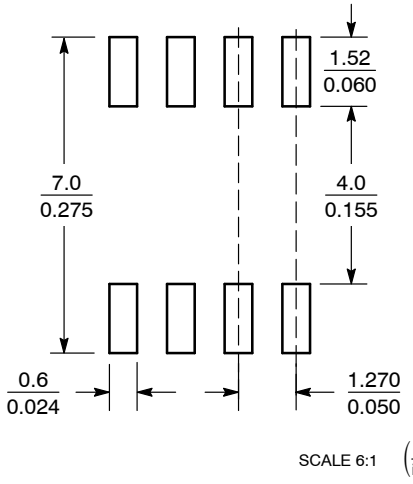
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

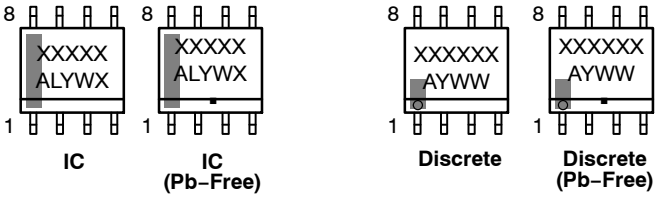
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 1 OF 2**

SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

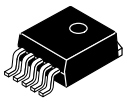
STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

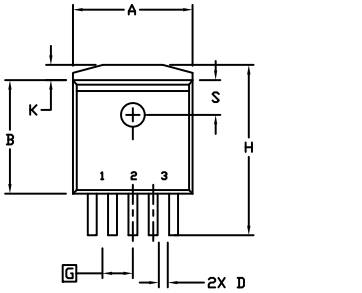
DOCUMENT NUMBER:	**98ASB42564B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−8 NB**		**PAGE 2 OF 2**



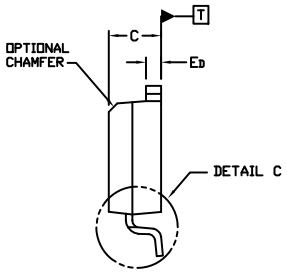
D²PAK 5–LEAD
CASE 936A–02
ISSUE E

DATE 28 JUL 2021

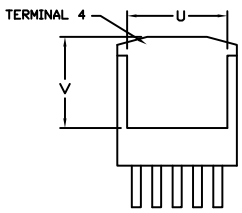
SCALE 1:1



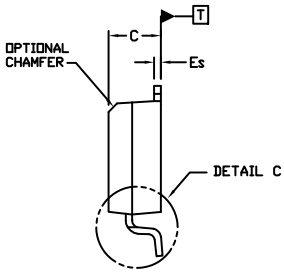
TOP VIEW



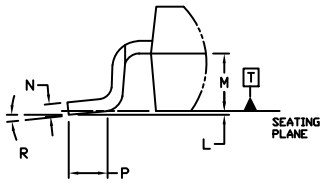
SIDE VIEW
DUAL GUAGE CONSTRUCTION



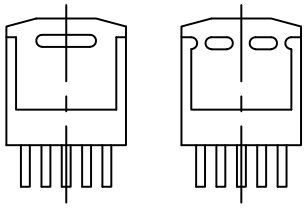
BOTTOM VIEW



SIDE VIEW
SINGLE GUAGE CONSTRUCTION



DETAIL C
TIP LEADFORM
ROTATED 90° CW



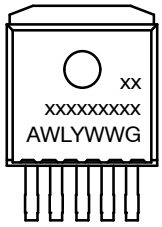
BOTTOM VIEW
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCHES
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 4.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

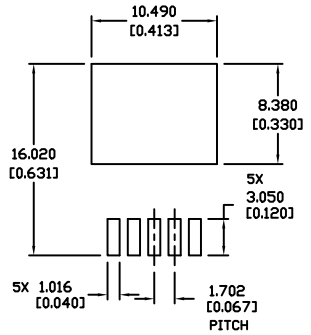
	INCHES		MILLIMETERS	
DIM	MIN.	MAX.	MIN.	MAX.
A	0.396	0.403	9.804	10.236
B	0.356	0.368	9.042	9.347
C	0.170	0.180	4.318	4.572
D	0.026	0.036	0.660	0.914
ED	0.045	0.055	1.143	1.397
ES	0.018	0.026	0.457	0.660
G	0.067 BSC		1.702 BSC	
H	0.539	0.579	13.691	14.707
K	0.050 REF		1.270 REF	
L	0.000	0.010	0.000	0.254
M	0.088	0.102	2.235	2.591
N	0.018	0.026	0.457	0.660
P	0.058	0.078	1.473	1.981
R	0°	8°	0°	8°
S	0.116 REF		2.946 REF	
U	0.200 MIN		5.080 MIN	
V	0.250 MIN		6.350 MIN	

GENERIC MARKING DIAGRAM*



XXXXXX	= Device Code
A	= Assembly Location
WL	= Wafer Lot
Y	= Year
WW	= Work Week
G	= Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	**98ASH01006A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**D2PAK 5–LEAD**		**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales