

# 500 mA, Very Low Dropout Bias Rail CMOS Voltage Regulator

## NCV8135

The NCV8135 is a 500 mA VLDO equipped with NMOS pass transistor and a separate bias supply voltage ( $V_{BIAS}$ ). The device provides very stable, accurate output voltage with low noise suitable for space constrained, noise sensitive applications. In order to optimize performance for battery operated portable applications, the NCV8135 features low  $I_Q$  consumption. The NCV8135 is offered in WDFN6 2 mm x 2 mm package, wettable flanks option available for Enhanced Optical Inspection.

### Features

- Input Voltage Range: 0.4 V to 5.5 V
- Bias Voltage Range: 2.5 V to 5.5 V
- Fixed Output Voltage Versions Available
- $\pm 1\%$  Accuracy over Temperature,  $0.5\% V_{OUT}$  @  $25^\circ\text{C}$
- Ultra-Low Dropout: Typ. 53 mV at 500 mA
- Very Low Bias Input Current of Typ.  $35 \mu\text{A}$
- Logic Level Enable Input for ON/OFF Control
- Output Active Discharge Option Available
- Stable with a  $10 \mu\text{F}$  Ceramic Capacitor
- NCV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- Automotive, Consumer and Industrial Equipment Point of Load Regulation
- Battery-powered Equipment
- Smartphones, Tablets
- Cameras, DVRs, STB and Camcorders

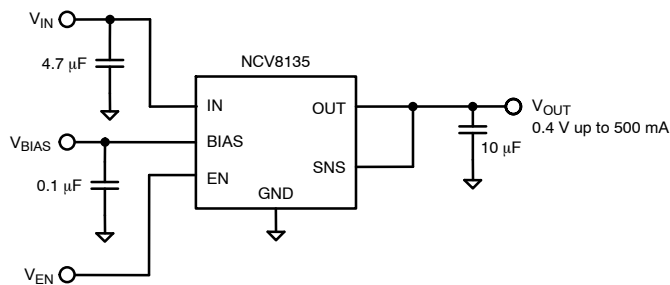
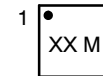


Figure 1. Typical Application Schematic



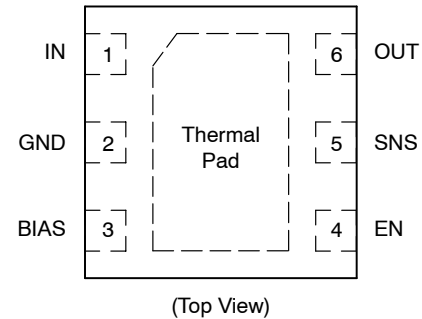
WDFN6  
CASE 511BR

### MARKING DIAGRAM



XX = Specific Device Code  
M = Date Code

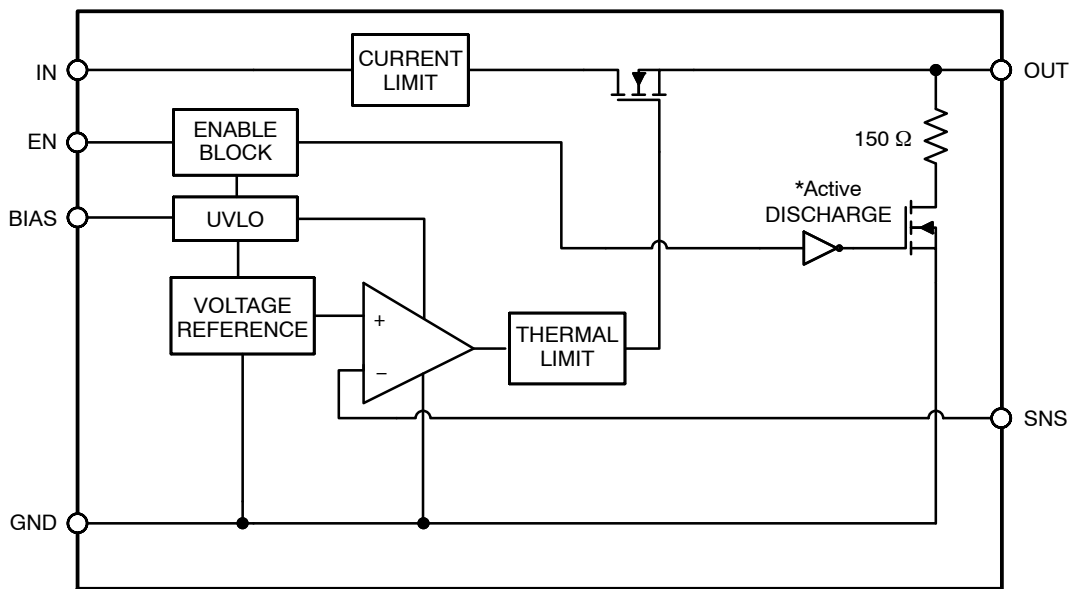
### PIN CONNECTIONS



### ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 9 of this data sheet.

# NCV8135



\*Active output discharge function is present only in NCV8135A option devices.

**Figure 2. Simplified Schematic Block Diagram**

# NCV8135

## PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	VIN	Input Voltage Supply pin
2	GND	Ground pin
3	VBIAS	Bias voltage supply for internal control circuits. This pin is monitored by internal Under-Voltage Lockout Circuit.
4	EN	Enable pin. Driving this pin high enables the regulator. Driving this pin low puts the regulator into shutdown mode.
5	SNS	Output voltage Sensing Input. Connect to Output voltage node on the PCB.
6	VOUT	Regulated Output Voltage pin
Pad	Pad	Should be soldered to the ground plane for increased thermal performance.

## ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	$V_{IN}$	-0.3 to 6	V
Output Voltage	$V_{OUT}$	-0.3 to $(V_{IN}+0.3) \leq 6$	V
Chip Enable, Bias and SNS Input	$V_{EN}, V_{BIAS}, V_{SNS}$	-0.3 to 6	V
Output Short Circuit Duration	$t_{SC}$	unlimited	s
Maximum Junction Temperature	$T_J$	125	°C
Storage Temperature	$T_{STG}$	-55 to 150	°C
ESD Capability, Human Body Model (Note 2)	$ESD_{HBM}$	2000	V
ESD Capability, Machine Model (Note 2)	$ESD_{MM}$	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
- This device series incorporates ESD protection (except OUT pin) and is tested by the following methods:
  - ESD Human Body Model tested per AEC-Q100-002
  - ESD Machine Model tested per AEC-Q100-003
  - Latchup Current Maximum Rating  $\pm 100$  mA per AEC-Q100-004.

## THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, WDFN6 2 mm x 2 mm Thermal Resistance, Junction-to-Air (Note 3)	$R_{\theta JA}$	97	°C/W

- This data was derived by thermal simulations based on the JEDEC JESD51 series standards methodology. Only a single device mounted at the center of a high K (2s2p) 3 in x 3 in multilayer board with 1-ounce internal planes and 1-ounce copper on top and bottom. Top copper layer has a dedicated 25 sq mm copper area.

# NCV8135

**ELECTRICAL CHARACTERISTICS**  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ ;  $V_{\text{BIAS}} = 2.7\text{ V}$  or  $(V_{\text{OUT}} + 1.6\text{ V})$ , whichever is greater,  $V_{\text{IN}} = V_{\text{OUT(NOM)}} + 0.3\text{ V}$ ,  $I_{\text{OUT}} = 1\text{ mA}$ ,  $V_{\text{EN}} = 1\text{ V}$ ,  $C_{\text{IN}} = 4.7\text{ }\mu\text{F}$ ,  $C_{\text{OUT}} = 10\text{ }\mu\text{F}$ ,  $C_{\text{BIAS}} = 1\text{ }\mu\text{F}$ , unless otherwise noted. Typical values are at  $T_J = +25^{\circ}\text{C}$ . Min/Max values are for  $-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$  unless otherwise noted. (Note 4)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
Operating Input Voltage Range		$V_{\text{IN}}$	$V_{\text{OUT}} + V_{\text{DO}}$		5.5	V
Operating Bias Voltage Range		$V_{\text{BIAS}}$	$(V_{\text{OUT}} + 1.50) \geq 2.5$		5.5	V
Undervoltage Lock-out	$V_{\text{BIAS}}$ Rising Hysteresis	UVLO		1.6 0.2		V
Output Voltage Accuracy		$V_{\text{OUT}}$		$\pm 0.5$		%
Output Voltage Accuracy	$-40^{\circ}\text{C} \leq T_J \leq 125^{\circ}\text{C}$ , $V_{\text{OUT(NOM)}} + 0.3\text{ V} \leq V_{\text{IN}} \leq V_{\text{OUT(NOM)}} + 1.0\text{ V}$ , $2.7\text{ V}$ or $(V_{\text{OUT(NOM)}} + 1.6\text{ V})$ , whichever is greater $< V_{\text{BIAS}} < 5.5\text{ V}$ , $1\text{ mA} < I_{\text{OUT}} < 500\text{ mA}$	$V_{\text{OUT}}$	-1.0		+1.0	%
$V_{\text{IN}}$ Line Regulation	$V_{\text{OUT(NOM)}} + 0.3\text{ V} \leq V_{\text{IN}} \leq 5.0\text{ V}$	LineReg		0.01		%/V
$V_{\text{BIAS}}$ Line Regulation	$2.7\text{ V}$ or $(V_{\text{OUT(NOM)}} + 1.6\text{ V})$ , whichever is greater $< V_{\text{BIAS}} < 5.5\text{ V}$	LineReg		0.01		%/V
Load Regulation	$I_{\text{OUT}} = 1\text{ mA}$ to $500\text{ mA}$	LoadReg		0.5		mV
$V_{\text{IN}}$ Dropout Voltage	$I_{\text{OUT}} = 500\text{ mA}$ (Note 5)	$V_{\text{DO}}$		53	100	mV
$V_{\text{BIAS}}$ Dropout Voltage	$I_{\text{OUT}} = 500\text{ mA}$ , $V_{\text{IN}} = V_{\text{BIAS}}$ (Notes 5, 6)	$V_{\text{DO}}$		1.1	1.5	V
Output Current Limit	$V_{\text{OUT}} = 90\% V_{\text{OUT(NOM)}}$	$I_{\text{CL}}$	600	820	1200	mA
SNS Pin Operating Current		$I_{\text{SNS}}$		0.01	0.5	$\mu\text{A}$
Bias Pin Quiescent Current	$V_{\text{BIAS}} = 2.7\text{ V}$ , $I_{\text{OUT}} = 0\text{ mA}$	$I_{\text{BIASQ}}$		35	55	$\mu\text{A}$
Bias Pin Disable Current	$V_{\text{EN}} \leq 0.4\text{ V}$	$I_{\text{BIAS(DIS)}}$		0.2	1	$\mu\text{A}$
Vinput Pin Disable Current	$V_{\text{EN}} \leq 0.4\text{ V}$	$I_{\text{VIN(DIS)}}$		0.01	1	$\mu\text{A}$
EN Pin Threshold Voltage	EN Input Voltage "H"	$V_{\text{EN(H)}}$	0.9			V
	EN Input Voltage "L"	$V_{\text{EN(L)}}$			0.4	
EN Pull Down Current	$V_{\text{EN}} = 5.5\text{ V}$	$I_{\text{EN}}$		0.3	1	$\mu\text{A}$
Turn-On Time	From assertion of $V_{\text{EN}}$ to $V_{\text{OUT}} = 98\% V_{\text{OUT(NOM)}}$ $V_{\text{OUT(NOM)}} = 0.4\text{ V}$ $V_{\text{OUT(NOM)}} = 1.2\text{ V}$ $V_{\text{OUT(NOM)}} = 0.75\text{ V}$	$t_{\text{ON}}$		150 275 198		$\mu\text{s}$
Power Supply Rejection Ratio	$V_{\text{IN}}$ to $V_{\text{OUT}}$ , $f = 1\text{ kHz}$ , $I_{\text{OUT}} = 10\text{ mA}$ , $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5\text{ V}$ , $V_{\text{OUT(NOM)}} = 0.4\text{ V}$	PSRR( $V_{\text{IN}}$ )		73		dB
	$V_{\text{BIAS}}$ to $V_{\text{OUT}}$ , $f = 1\text{ kHz}$ , $I_{\text{OUT}} = 10\text{ mA}$ , $V_{\text{IN}} \geq V_{\text{OUT}} + 0.5\text{ V}$ , $V_{\text{OUT(NOM)}} = 0.4\text{ V}$	PSRR( $V_{\text{BIAS}}$ )		90		
Output Noise Voltage	$V_{\text{IN}} = V_{\text{OUT}} + 0.5\text{ V}$ , $f = 10\text{ Hz}$ to $100\text{ kHz}$ $V_{\text{OUT(NOM)}} = 0.4\text{ V}$ $V_{\text{OUT(NOM)}} = 1.2\text{ V}$ $V_{\text{OUT(NOM)}} = 0.75\text{ V}$	$V_{\text{N}}$		28.7 40.3 35.3		$\mu\text{VRMS}$
Thermal Shutdown Threshold	Temperature increasing			160		$^{\circ}\text{C}$
	Temperature decreasing			140		
Output Discharge Pull-Down	$V_{\text{EN}} \leq 0.4\text{ V}$ , $V_{\text{OUT}} = 0.5\text{ V}$ , NCV8135A options only	$R_{\text{DISCH}}$		150		$\Omega$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Performance guaranteed over the indicated operating temperature range by design and/or characterization. Production tested at  $T_A = 25^{\circ}\text{C}$ . Low duty cycle pulse techniques are used during the testing to maintain the junction temperature as close to ambient as possible.
5. Dropout voltage is characterized when  $V_{\text{OUT}}$  falls 3% below  $V_{\text{OUT(NOM)}}$ .
6. For output voltages below  $0.9\text{ V}$ ,  $V_{\text{BIAS}}$  dropout voltage does not apply due to a minimum Bias operating voltage of  $2.5\text{ V}$ .

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ ,  $V_{BIAS} = 2.7\text{ V}$ ,  $V_{EN} = 1.0\text{ V}$ ,  $V_{OUT(NOM)} = 0.4\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (effective capacitance value), unless otherwise noted.

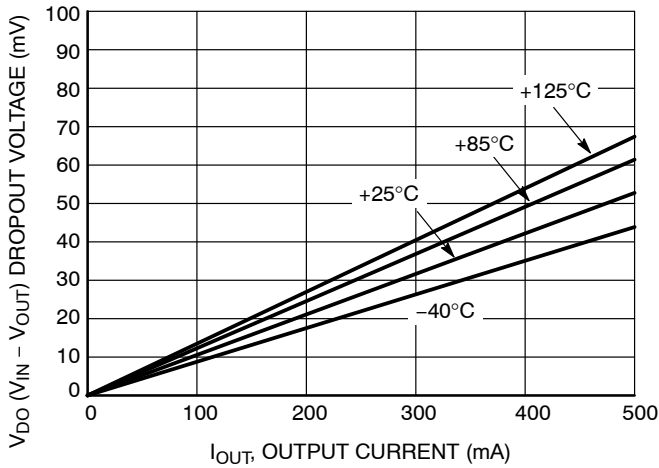


Figure 3.  $V_{IN}$  Dropout Voltage vs.  $I_{OUT}$  and Temperature  $T_J$

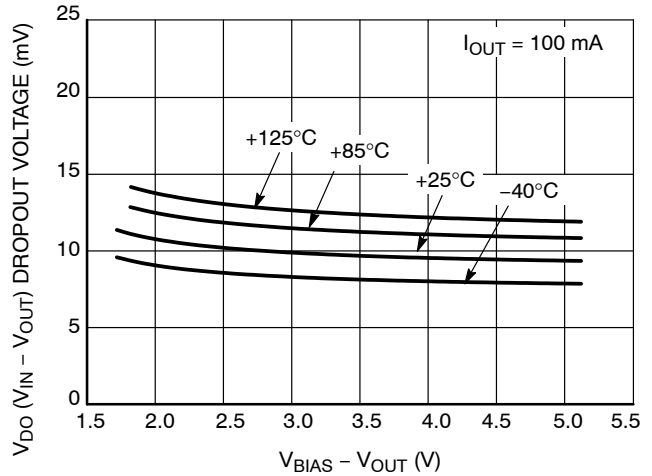


Figure 4.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

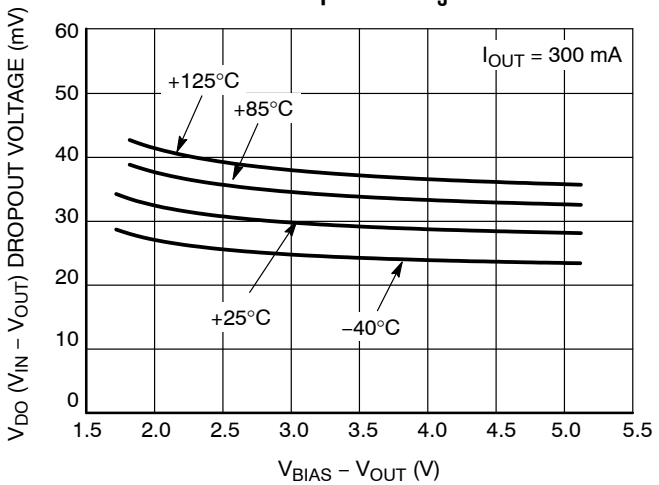


Figure 5.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

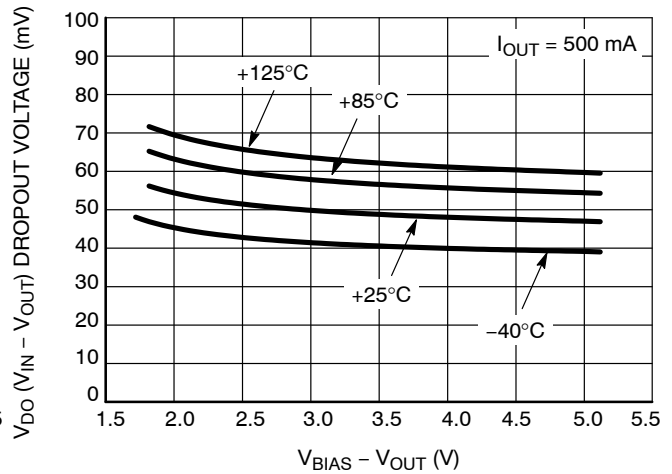


Figure 6.  $V_{IN}$  Dropout Voltage vs.  $(V_{BIAS} - V_{OUT})$  and Temperature  $T_J$

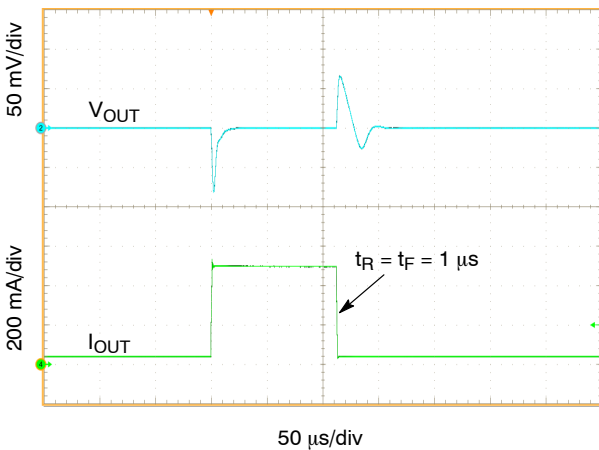


Figure 7. Load Transient Response,  $I_{OUT} = 50\text{ mA}$  to  $500\text{ mA}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$

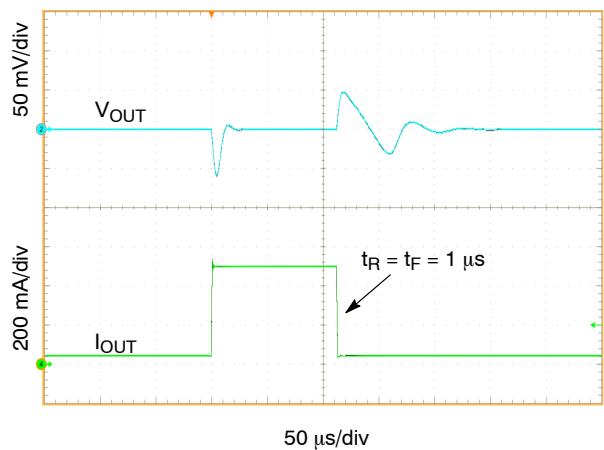


Figure 8. Load Transient Response,  $I_{OUT} = 50\text{ mA}$  to  $500\text{ mA}$ ,  $C_{OUT} = 22\text{ }\mu\text{F}$

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ ,  $V_{BIAS} = 2.7\text{ V}$ ,  $V_{EN} = 1.0\text{ V}$ ,  $V_{OUT(NOM)} = 0.4\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (effective capacitance value), unless otherwise noted.

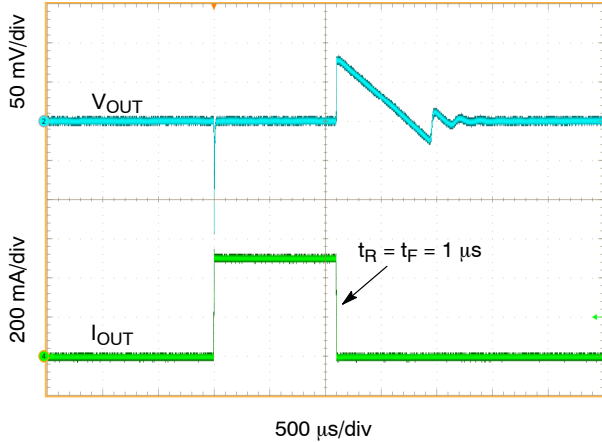


Figure 9. Load Transient Response,  $I_{OUT} = 1\text{ mA}$  to  $500\text{ mA}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$

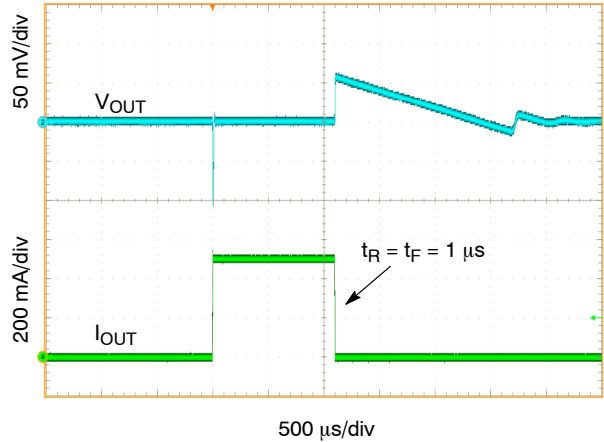


Figure 10. Load Transient Response,  $I_{OUT} = 1\text{ mA}$  to  $500\text{ mA}$ ,  $C_{OUT} = 22\text{ }\mu\text{F}$

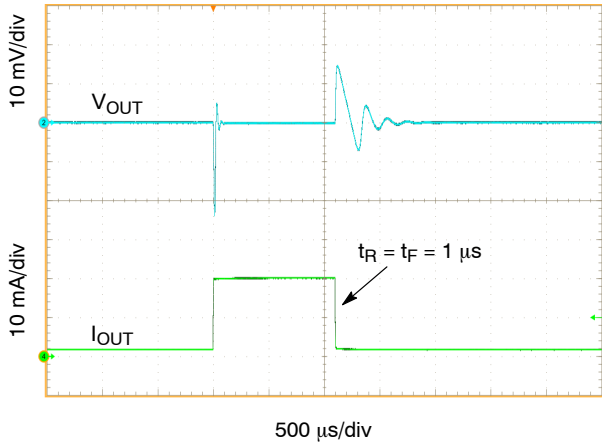


Figure 11. Load Transient Response,  $I_{OUT} = 1\text{ mA}$  to  $20\text{ mA}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$

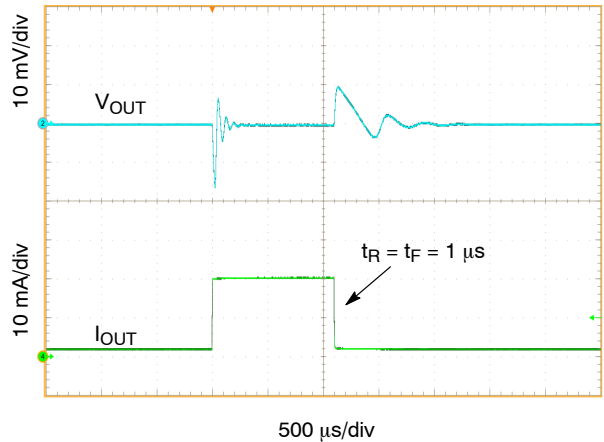


Figure 12. Load Transient Response,  $I_{OUT} = 1\text{ mA}$  to  $20\text{ mA}$ ,  $C_{OUT} = 22\text{ }\mu\text{F}$

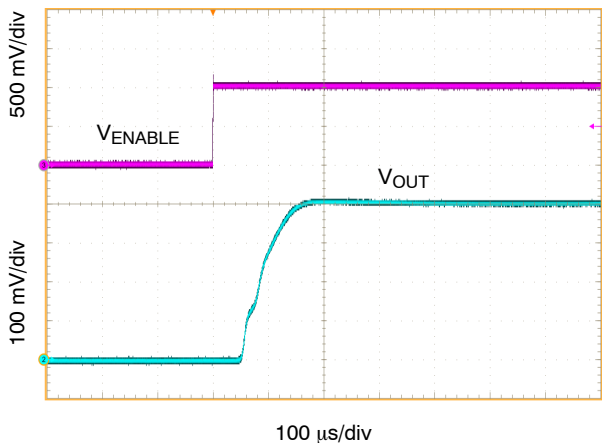


Figure 13. Enable Transient Response,  $I_{OUT} = 0\text{ mA}$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$

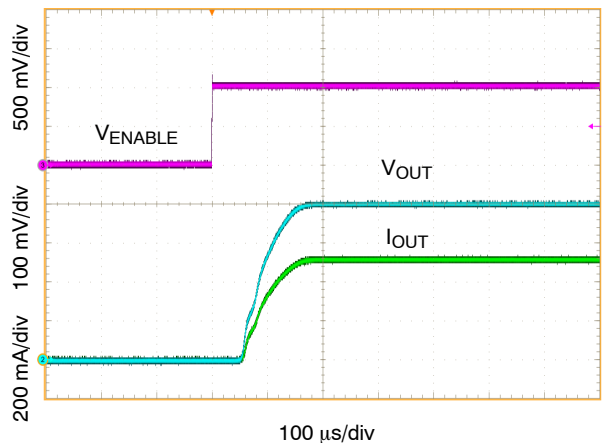


Figure 14. Enable Transient Response, Output Resistive Load  $500\text{ mA}$ ,  $C_{OUT} = 22\text{ }\mu\text{F}$

TYPICAL CHARACTERISTICS

At  $T_J = +25^\circ\text{C}$ ,  $V_{IN} = V_{OUT(NOM)} + 0.3\text{ V}$ ,  $V_{BIAS} = 2.7\text{ V}$ ,  $V_{EN} = 1.0\text{ V}$ ,  $V_{OUT(NOM)} = 0.4\text{ V}$ ,  $I_{OUT} = 500\text{ mA}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{BIAS} = 0.1\text{ }\mu\text{F}$ , and  $C_{OUT} = 10\text{ }\mu\text{F}$  (effective capacitance value), unless otherwise noted.

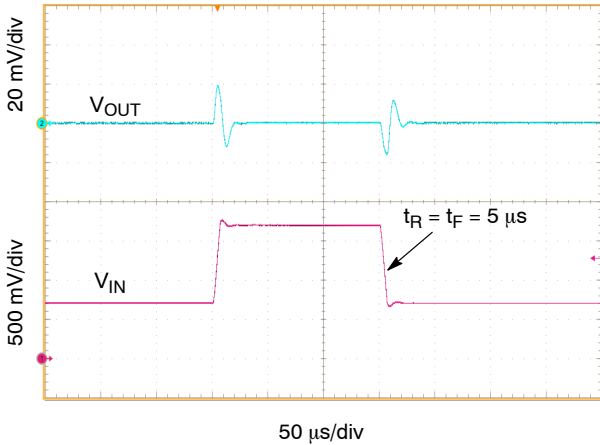


Figure 15.  $V_{IN}$  Line Transient Response,  $V_{IN} = 0.7\text{ V}$  to  $1.7\text{ V}$ ,  $I_{OUT} = 100\text{ mA}$ ,  $C_{IN} = 0$ ,  $C_{OUT} = 10\text{ }\mu\text{F}$

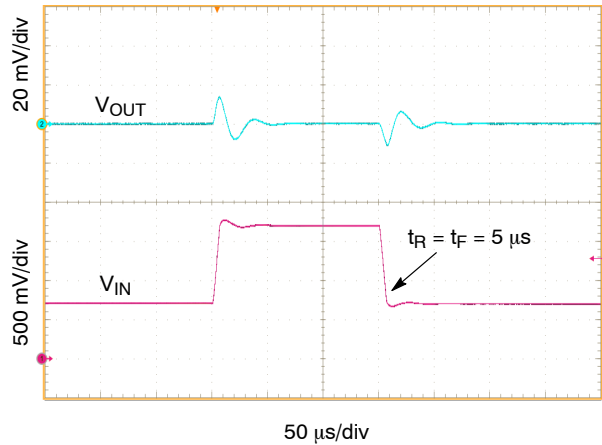


Figure 16.  $V_{IN}$  Line Transient Response,  $V_{IN} = 0.7\text{ V}$  to  $1.7\text{ V}$ ,  $I_{OUT} = 100\text{ mA}$ ,  $C_{IN} = 0$ ,  $C_{OUT} = 22\text{ }\mu\text{F}$

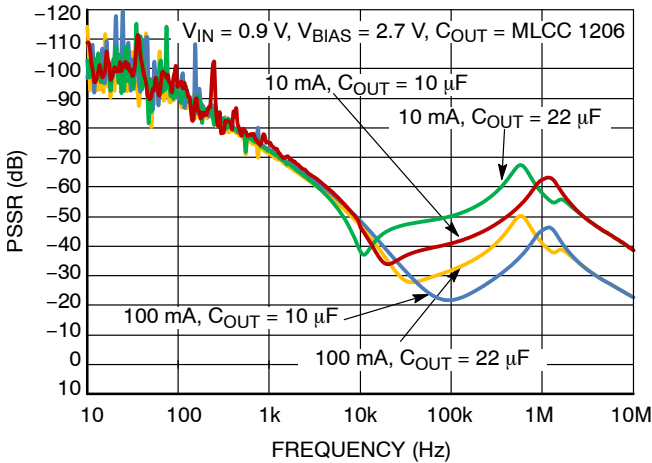


Figure 17.  $V_{IN}$  Power Supply Rejection Ratio vs. Frequency

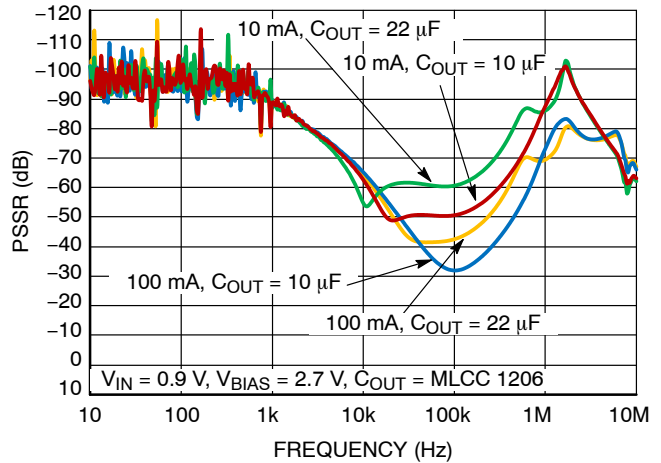


Figure 18.  $V_{BIAS}$  Power Supply Rejection Ratio vs. Frequency

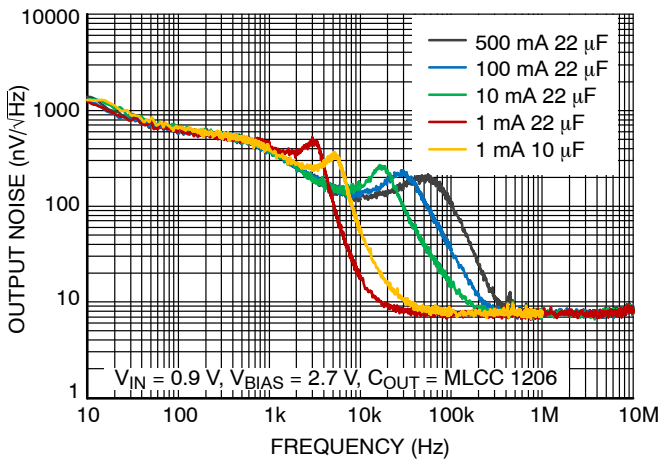
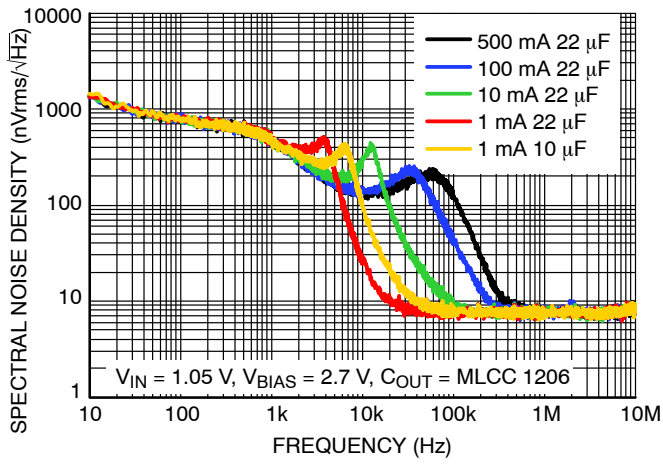


Figure 19. Output Voltage Noise Spectral Density at NCV8135AMT040TBG

		RMS Output Noise Voltage ( $\mu\text{V}$ )	
$I_{OUT}$	$C_{OUT}$	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	10 $\mu\text{F}$	28.67	27.54
1 mA	22 $\mu\text{F}$	28.19	27.28
10 mA	22 $\mu\text{F}$	36.23	35.49
100 mA	22 $\mu\text{F}$	45.44	44.87
500 mA	22 $\mu\text{F}$	54.54	54.04

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**Figure 20. Output Voltage Noise Spectral Density at NCV8135AMTW075TBG**

		RMS Output Noise Voltage ( $\mu\text{V}$ )	
$I_{OUT}$	$C_{OUT}$	10 Hz – 100 kHz	100 Hz – 100 kHz
1 mA	10 $\mu\text{F}$	35.34	34.22
1 mA	22 $\mu\text{F}$	33.39	32.22
10 mA	22 $\mu\text{F}$	41.85	40.91
100 mA	22 $\mu\text{F}$	51.70	50.98
500 mA	22 $\mu\text{F}$	59.78	59.16



APPLICATIONS INFORMATION

The NCV8135 dual-rail very low dropout voltage regulator is using NMOS pass transistor for output voltage regulation from  $V_{IN}$  voltage. All the low current internal control circuitry is powered from the  $V_{BIAS}$  voltage.

The use of an NMOS pass transistor offers several advantages in applications. Unlike PMOS topology devices, the output capacitor has reduced impact on loop stability.  $V_{in}$  to  $V_{out}$  operating voltage difference can be very low compared with standard PMOS regulators in very low  $V_{in}$  applications.

When enabled from Enable (EN) input, the NCV8135 offers smooth monotonic start-up. The controlled voltage rising limits the inrush current.

The Enable (EN) input is equipped with internal hysteresis.

**Dropout Voltage**

Because of two power supply inputs  $V_{IN}$  and  $V_{BIAS}$  and one  $V_{OUT}$  regulator output, there are two Dropout voltages specified.

The first, the  $V_{IN}$  Dropout voltage is the voltage difference ( $V_{IN} - V_{OUT}$ ) when  $V_{OUT}$  starts to decrease by percent specified in the Electrical Characteristics table.  $V_{BIAS}$  is high enough; specific value is published in the Electrical Characteristics table.

The second,  $V_{BIAS}$  dropout voltage is the voltage difference ( $V_{BIAS} - V_{OUT}$ ) when  $V_{IN}$  and  $V_{BIAS}$  pins are joined together and  $V_{OUT}$  starts to decrease.

**Input and Output Capacitors**

The device is designed to be stable for ceramic output capacitors with Effective capacitance in the range from 10  $\mu$ F to 22  $\mu$ F. The device is also stable with multiple capacitors in parallel, having the total effective capacitance in the specified range.

In applications where no low input supplies impedance available (PCB inductance in  $V_{IN}$  and/or  $V_{BIAS}$  inputs as example), the recommended  $C_{IN} = 1 \mu$ F and  $C_{BIAS} = 0.1 \mu$ F or greater. Ceramic capacitors are recommended. For the best performance all the capacitors should be connected to

the NCV8135 respective pins directly in the device PCB copper layer, not through vias having not negligible impedance.

When using small ceramic capacitor, their capacitance is not constant but varies with applied DC biasing voltage, temperature and tolerance. The effective capacitance can be much lower than their nominal capacitance value, most importantly in negative temperatures and higher LDO output voltages. That is why the recommended Output capacitor capacitance value is specified as Effective value in the specific application conditions.

**Enable Operation**

The enable pin will turn the regulator on or off. The threshold limits are covered in the electrical characteristics table in this data sheet. To get the full functionality of soft-start, it is recommended to turn on the  $V_{IN}$  and  $V_{BIAS}$  supply voltages first and activate the Enable pin no sooner than when  $V_{IN}$  and  $V_{BIAS}$  are on their nominal levels. If the enable function is not to be used then the pin should be connected to  $V_{IN}$  or  $V_{BIAS}$ .

**Current Limitation**

The internal Current Limitation circuitry allows the device to supply the full nominal current and surges but protects the device against Current Overload or Short.

**Thermal Protection**

Internal thermal shutdown (TSD) circuitry is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When TSD activated, the regulator output turns off. When cooling down under the low temperature threshold, device output is activated again. This TSD feature is provided to prevent failures from accidental overheating.

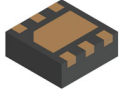
Activation of the thermal protection circuit indicates excessive power dissipation or inadequate heatsinking. For reliable operation, junction temperature should be limited to +125°C maximum.

**ORDERING INFORMATION**

Device	Marking	Voltage	Option	Package	Shipping†
NCV8135AMT040TBG	KA	0.4 V	Output Active Discharge	WDFN6 (Non-Wettable Flank) (Pb-Free)	3000 / Tape & Reel
NCV8135BMT040TBG	KC	0.4 V	Non-Active Discharge		
NCV8135AMT120TBG	KE	1.2 V	Output Active Discharge		
NCV8135AMTW040TBG	K2	0.4 V	Output Active Discharge	WDFN6 (Wettable Flank) (Pb-Free)	
NCV8135BMTW040TBG	K3	0.4 V	Non-Active Discharge		
NCV8135AMTW120TBG	K4	1.2 V	Output Active Discharge		
NCV8135AMTW075TBG	KL	0.75 V	Output Active Discharge		

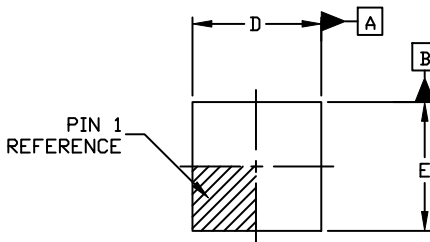
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

To order other package and voltage variants, please contact your ON Semiconductor sales representative

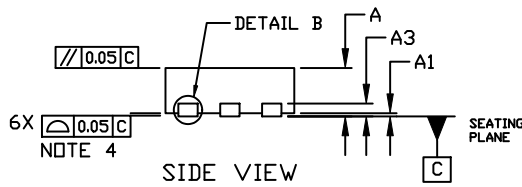


**WDFN6 2x2, 0.65P  
CASE 511BR  
ISSUE C**

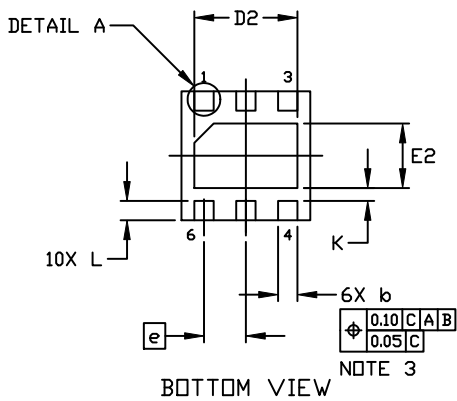
DATE 01 DEC 2021



TOP VIEW



SIDE VIEW



BOTTOM VIEW

**GENERIC  
MARKING DIAGRAM\***

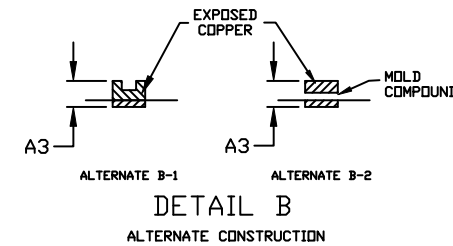


XX = Specific Device Code  
M = Date Code

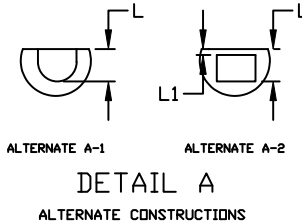
\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

NOTES:

1. DIMENSION AND TOLERANCING PER ASME Y14.5, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

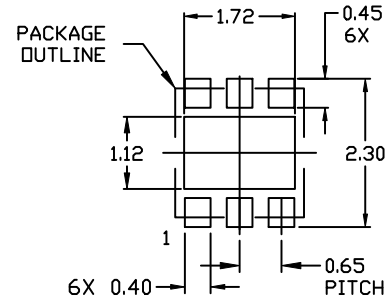


DETAIL B  
ALTERNATE CONSTRUCTION



DETAIL A  
ALTERNATE CONSTRUCTIONS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	---	0.05
A3	0.20 REF		
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
E	1.90	2.00	2.10
E2	0.90	1.00	1.10
e	0.65 BSC		
K	0.20 REF		
L	0.20	0.30	0.40
L1	---	---	0.15



RECOMMENDED  
MOUNTING FOOTPRINT

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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<b>DESCRIPTION:</b>	<b>WDFN6 2X2, 0.65P</b>	<b>PAGE 1 OF 1</b>

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