NCS6433

Wideband Quad 2:1 Video Switch

The NCS6433 is a wide bandwidth, bidirectional, Quad 2:1, NMOS−based video switch suitable for dealing with video signals such as RGB, composite, S−Video, and component video (YPbPr).

The NCS6433 is controlled by a single switch−enabled ($\overline{OE}$) input. When $\overline{OE}$ is low the switch is enabled and the A port is connected to the B port. When $\overline{OE}$ is high the switch is disabled and the high−impedance state exists between the A and B ports. The line select (SEL) input controls the data path of the multiplexer/demultiplexer.

The NCS6433 has a wide bandwidth, low crosstalk, low on resistance, and fast switching times making it suitable for high−frequency video applications in high definition LCD TV's.

Features

- Very Wide Frequency Bandwidth: 570 MHz
- Low Switch Serial Resistance $R_{DS(on)}$, 4 Ω Typical
- Power Supply Voltage, 5 V
- Less Than 0.25 ns Bidirectional Maximum Propagation Delay Through Switch
- Low Quiescent Current: 3 μA Maximum
- Very Low Crosstalk, −80 dB Typical at 10 MHz
- Control Inputs are TTL/CMOS Compatible
- Ideal for High Definition Video Applications
- ESD HBM Protection 8 kV
- Fast Switching − Better Than 10 ns
- Capable of Driving a High Current at the Output (>100 mA)
- Available in SOIC−16 or TSSOP−16 Package
- This is a Pb−Free Device

Typical Applications

- Flat Panel Displays including LCDTV
- CRT Displays
- DVD Reader/Writer
- Set−Top Boxes

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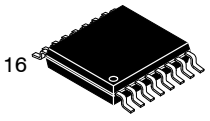
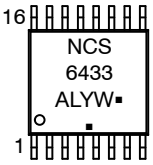
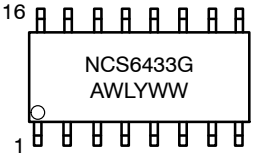


TSSOP−16
DTB SUFFIX
CASE 948F

SOIC−16
D SUFFIX
CASE 751B

MARKING DIAGRAMS

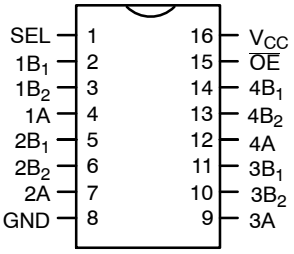




A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



TRUTH TABLE

SEL	$\overline{OE}$	Function
X	H	Open
L	L	A = B_1
H	L	A = B_2

PIN NAMES

Pin	Description
$\overline{OE}$	Bus Switch Enables
SEL	Select Inputs
A	Bus A
B_1, B_2	Bus B

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

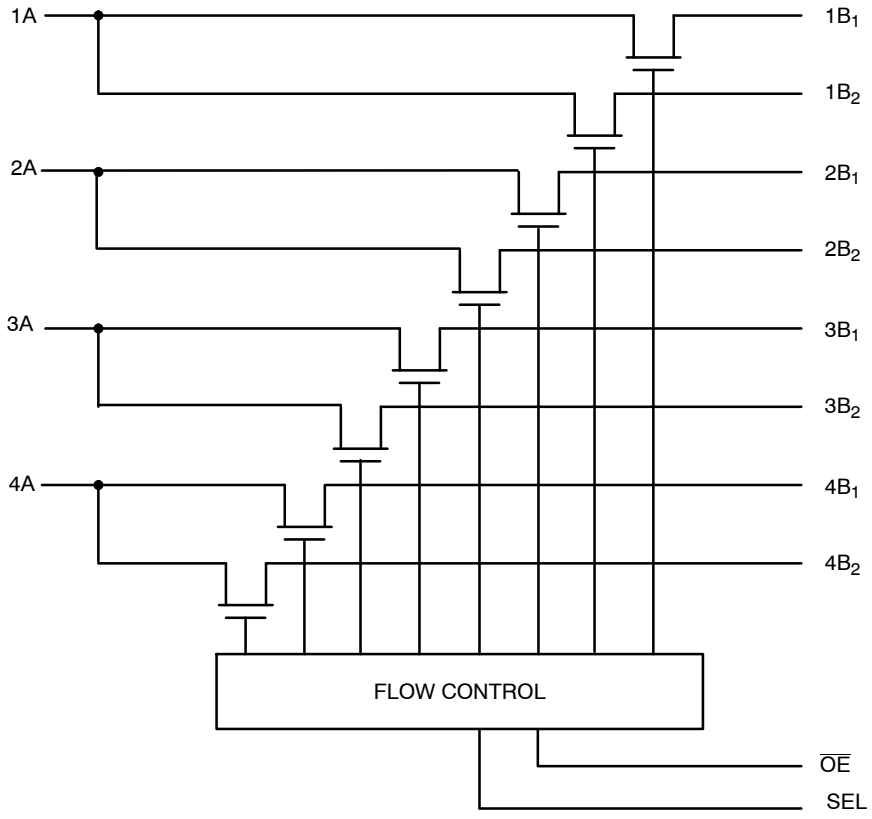


Figure 1. NCS6433 Block Diagram

ORDERING INFORMATION

Device Order Number	Package	Shipping†
NCS6433DR2G	SOIC−16 (Pb−Free)	2500 / Tape & Reel
NCS6433DTBR2G	TSSOP−16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ATTRIBUTES

Characteristics		Value
ESD Protection Human Body Model, R = 1000 Ω, C = 100 pF (Note 1) Machine Model	I/O Pins 2–7, 9–14 All Pins All Pins	8 kV 2 kV 100 V
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V–0 @ 0.125 in.
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latch–up Test		

1. Meets or exceeds JEDEC spec JESD22–A114–B.
2. For additional information, see Application Note AND8003/D

MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
DC Supply Voltage		V_{CC}	–0.5 to +5.5	V
DC Input Voltage		V_I	–0.5 to +5.5	V
DC Output Voltage		V_O	–0.5 to +5.5	V
DC Input Diode Current		I_{IK}	−50	mA
DC Output Diode Current		I_{OK}	−50	mA
DC Output Sink Current		I_O	128	mA
DC Supply Current per Supply Pin		I_{CC}	±100	mA
DC Ground Current per Ground Pin		I_{GND}	±100	mA
Storage Temperature Range		T_{STG}	–65 to +150	°C
Lead Temperature, 1 mm from Case for 10 Seconds		T_L	260	°C
Junction Temperature Under Bias (Note 3)		T_J	+150	°C
Thermal Resistance	SOIC–16 TSSOP–16	θ_{JA}	125 170	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = +25°C.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage	Operating, Data Retention Only	4.75	5.25	V
V_I	Input Voltage	(Note 4)	0	5.25	V
V_O	Output Voltage	(HIGH or LOW State)	0	5.25	V
T_A	Operating Free–Air Temperature		–40	+85	°C
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate Switch I/O	Switch Control Input V_{CC} = 5.0 V ± 0.5 V	 0	DC 5	ns/V

4. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

DC ELECTRICAL CHARACTERISTICS (T_A = −40°C to +85°C for Min and Max values, T_A = 25°C for Typ values)

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Typ*	Max	Unit
V_{IK}	Clamp Diode Voltage	I_{IN} = −18 mA	4.5	−1.2	−0.8		V
V_{IH}	High−Level Input Voltage		4.0 to 5.5	2.0			V
V_{IL}	Low−Level Input Voltage		4.0 to 5.5			0.8	V
I_{LI}	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V	5.5			±1.0	μA
I_{OZ}	Off−State Leakage Current	0 ≤ A, B ≤ V_{CC}	5.5			±1.0	μA
R_{ON}	Switch On Resistance (Note 5)	V_{IN} = 1 V, I_{ON} = 13 mA, R_L = 75 Ω	4.5		4.0	7.0	Ω
		V_{IN} = 2 V, I_{ON} = 26 mA, R_L = 75 Ω	4.5		7.0	10	
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND, I_{OUT} = 0	5.5			3.0	μA
ΔI_{CC}	Increase In I_{CC} per Input	One input at 3.4 V, Other inputs at V_{CC} or GND	5.5			2.5	mA

*Typical values are at V_{CC} = 5.0 V and T_A = 25°C.

5. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

AC ELECTRICAL CHARACTERISTICS (T_A = −40°C to +85°C, C_L = 20 pF, RU = RD = 75 Ω unless otherwise specified) (Note 6)

Symbol	Parameter	Conditions	V_{CC} = 4.5–5.5 V			Unit
			Min	Typ	Max	
t_{ON}	Turn On Time	R_L = 75 Ω, C_L = 20 pF, see Figure 7		2.8	5.0	ns
t_{OFF}	Turn Off Time	R_L = 75 Ω, C_L = 20 pF, see Figure 7		1.4	5.0	ns
BW	−3 dB Bandwidth	R_L = 150 Ω, T_A = 25°C			570	MHz
X_{talk}	Crosstalk Adjacent Non−Adjacent	10 MHz, C_L = 0 pF, R_L = 150 Ω		−47 −80		dB
Off_{ISO}	Off Isolation	10 MHz, C_L = 0 pF, R_L = 150 Ω		−48		dB

6. T_A = +25°C, parameters characterized but not tested.

CAPACITANCES (Note 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{IN}	Control Pin Input Capacitance	V_{CC} = 5.0 V		2.0		pF
$C_{I/OA}$	A Port Input/Output Capacitance	V_{CC} = $\overline{OE}$ = 5.0 V		5.0		pF
$C_{I/OB}$	B Port Input/Output Capacitance	V_{CC} = $\overline{OE}$ = 5.0 V		5.0		pF

7. T_A = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

TYPICAL CHARACTERISTICS

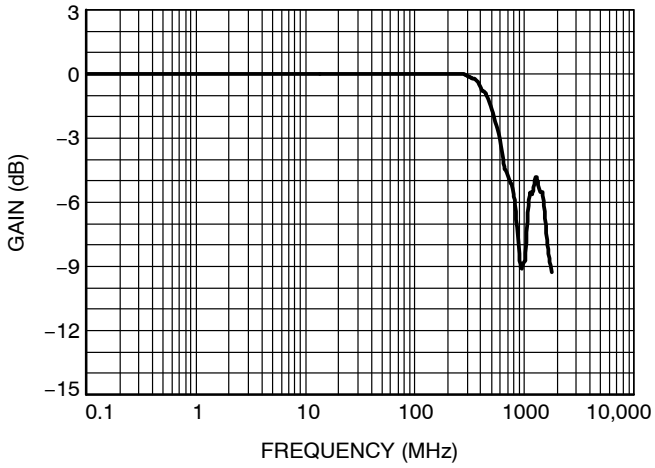


Figure 2. Gain vs. Frequency

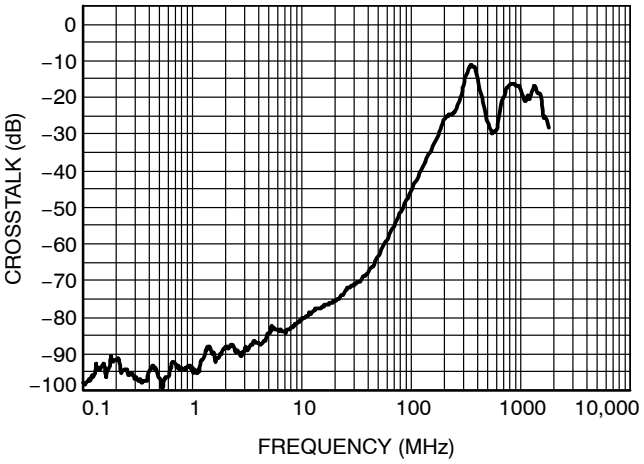


Figure 3. Crosstalk vs. Frequency (Non−Adjacent Channels)

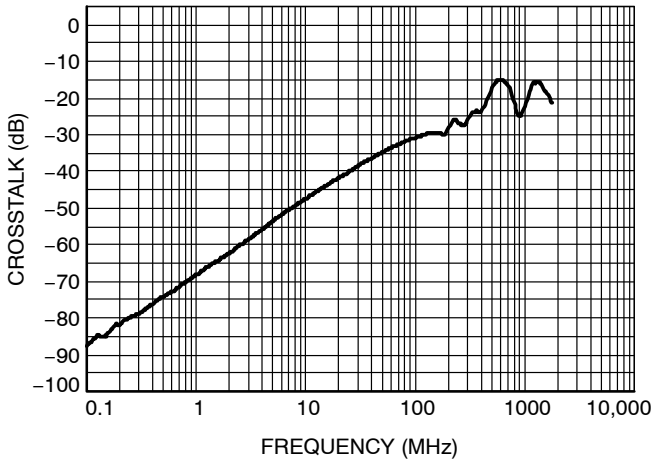


Figure 4. Crosstalk vs. Frequency (Adjacent Channels)

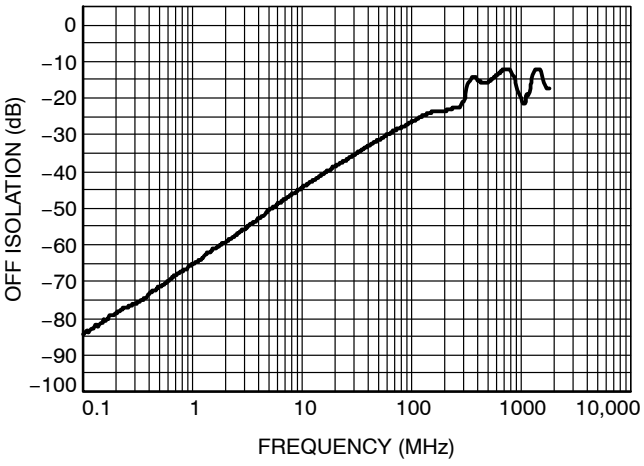


Figure 5. Off Isolation vs. Frequency

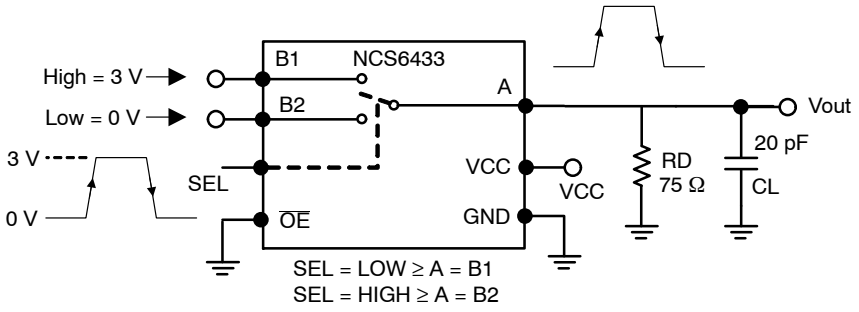


Figure 6. AC Test Circuit for Turn−on and Turn−off Times

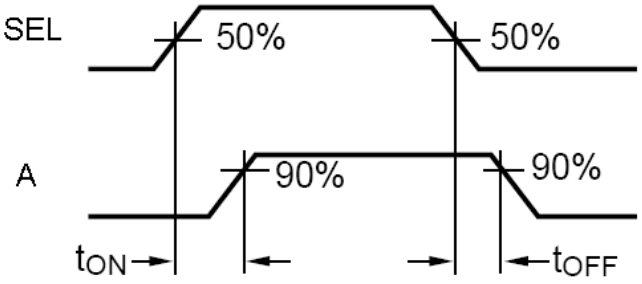


Figure 7. Turn−on and Turn−off Times

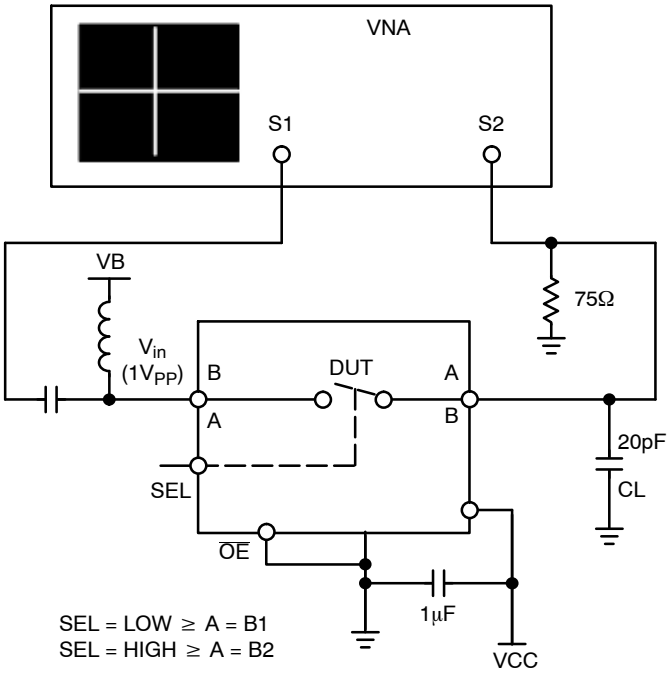


Figure 8. Gain, Crosstalk, Off−Isolation

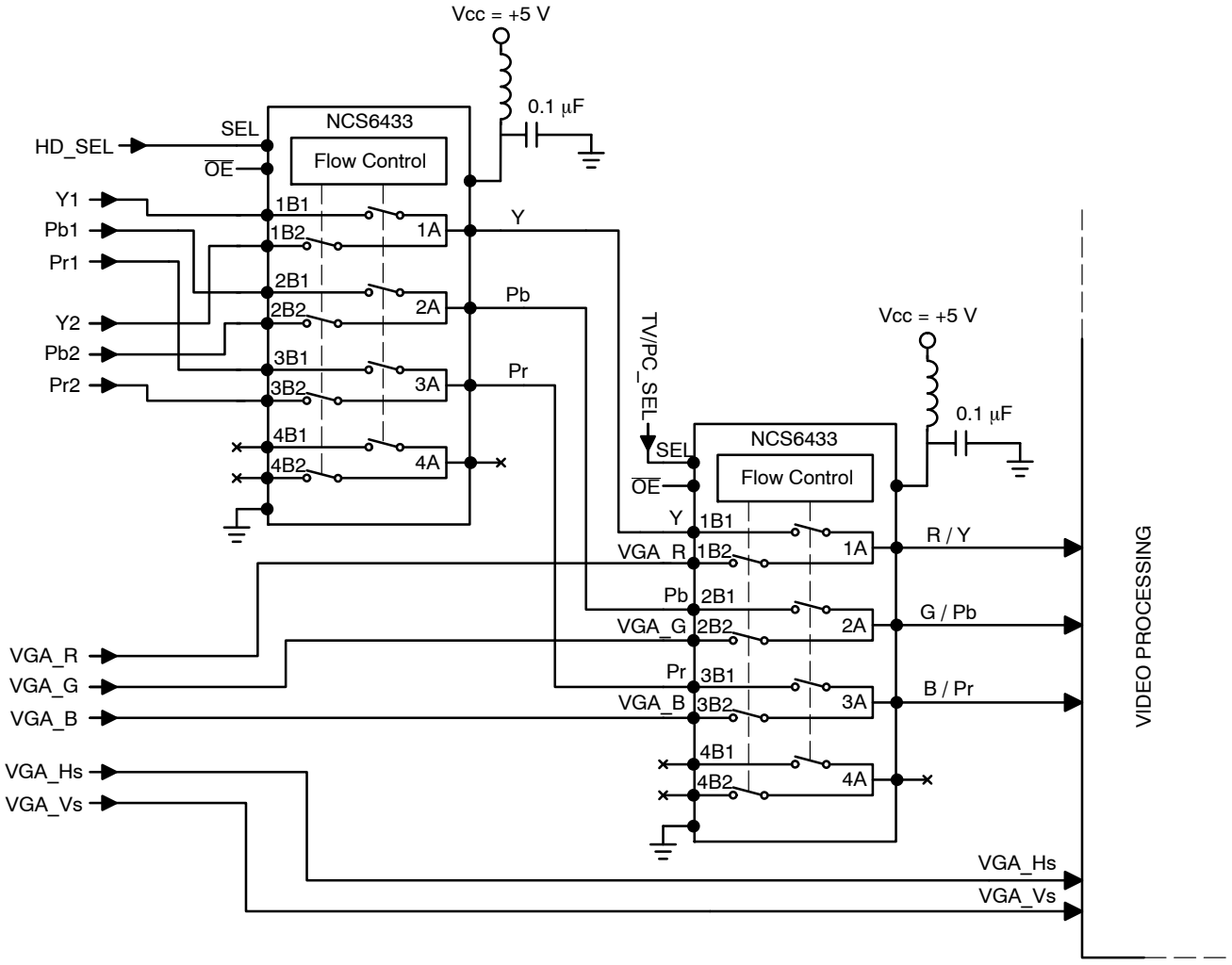
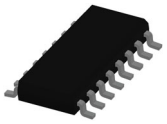


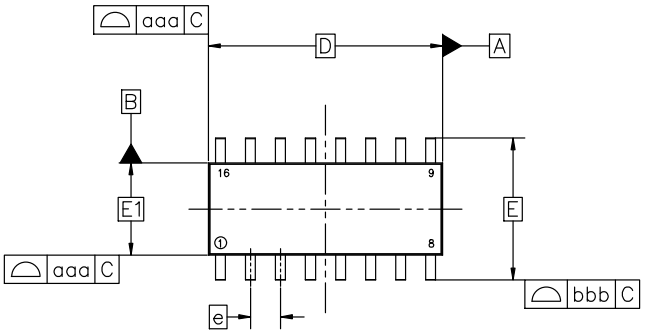
Figure 9. Example of LCDTV Application Using the Video Switch NCS6433



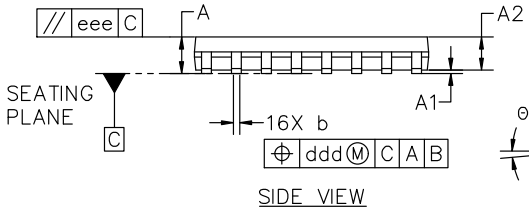
SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

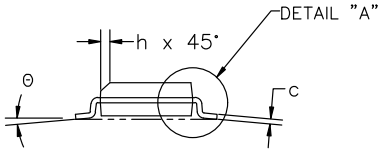
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



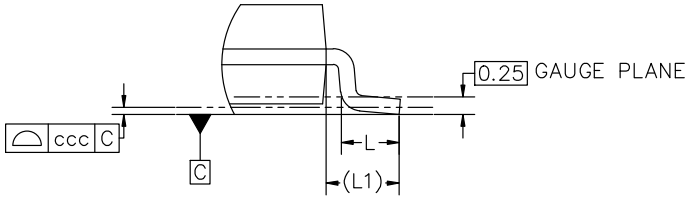
TOP VIEW



SIDE VIEW

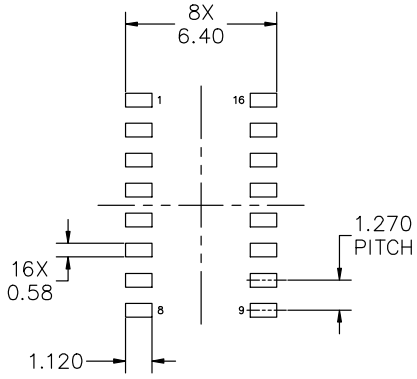


END VIEW



DETAIL "A"
Scale 3:1

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
Θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



RECOMMENDED MOUNTING FOOTPRINT

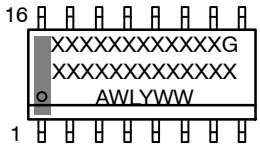
*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	**98ASB42566B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.	
DESCRIPTION:	**SOIC−16 9.90X3.90X1.37 1.27P**		**PAGE 1 OF 2**

SOIC−16 9.90x3.90x1.37 1.27P
CASE 751B
ISSUE M

DATE 18 OCT 2024

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:

PIN	
1.	COLLECTOR
2.	BASE
3.	EMITTER
4.	NO CONNECTION
5.	EMITTER
6.	BASE
7.	COLLECTOR
8.	COLLECTOR
9.	BASE
10.	EMITTER
11.	NO CONNECTION
12.	EMITTER
13.	BASE
14.	COLLECTOR
15.	EMITTER
16.	COLLECTOR

STYLE 2:

PIN	
1.	CATHODE
2.	ANODE
3.	NO CONNECTION
4.	CATHODE
5.	CATHODE
6.	NO CONNECTION
7.	ANODE
8.	CATHODE
9.	CATHODE
10.	ANODE
11.	NO CONNECTION
12.	CATHODE
13.	CATHODE
14.	NO CONNECTION
15.	ANODE
16.	CATHODE

STYLE 3:

PIN	
1.	COLLECTOR, DYE #1
2.	BASE, #1
3.	EMITTER, #1
4.	COLLECTOR, #1
5.	COLLECTOR, #2
6.	BASE, #2
7.	EMITTER, #2
8.	COLLECTOR, #2
9.	COLLECTOR, #3
10.	BASE, #3
11.	EMITTER, #3
12.	COLLECTOR, #3
13.	COLLECTOR, #4
14.	BASE, #4
15.	EMITTER, #4
16.	COLLECTOR, #4

STYLE 4:

PIN	
1.	COLLECTOR, DYE #1
2.	COLLECTOR, #1
3.	COLLECTOR, #2
4.	COLLECTOR, #2
5.	COLLECTOR, #3
6.	COLLECTOR, #3
7.	COLLECTOR, #4
8.	COLLECTOR, #4
9.	BASE, #4
10.	EMITTER, #4
11.	BASE, #3
12.	EMITTER, #3
13.	BASE, #2
14.	EMITTER, #2
15.	BASE, #1
16.	EMITTER, #1

STYLE 5:

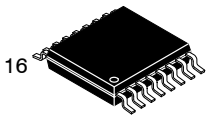
PIN	
1.	DRAIN, DYE #1
2.	DRAIN, #1
3.	DRAIN, #2
4.	DRAIN, #2
5.	DRAIN, #3
6.	DRAIN, #3
7.	DRAIN, #4
8.	DRAIN, #4
9.	GATE, #4
10.	SOURCE, #4
11.	GATE, #3
12.	SOURCE, #3
13.	GATE, #2
14.	SOURCE, #2
15.	GATE, #1
16.	SOURCE, #1

STYLE 6:

PIN	
1.	CATHODE
2.	CATHODE
3.	CATHODE
4.	CATHODE
5.	CATHODE
6.	CATHODE
7.	CATHODE
8.	CATHODE
9.	ANODE
10.	ANODE
11.	ANODE
12.	ANODE
13.	ANODE
14.	ANODE
15.	ANODE
16.	ANODE

STYLE 7:

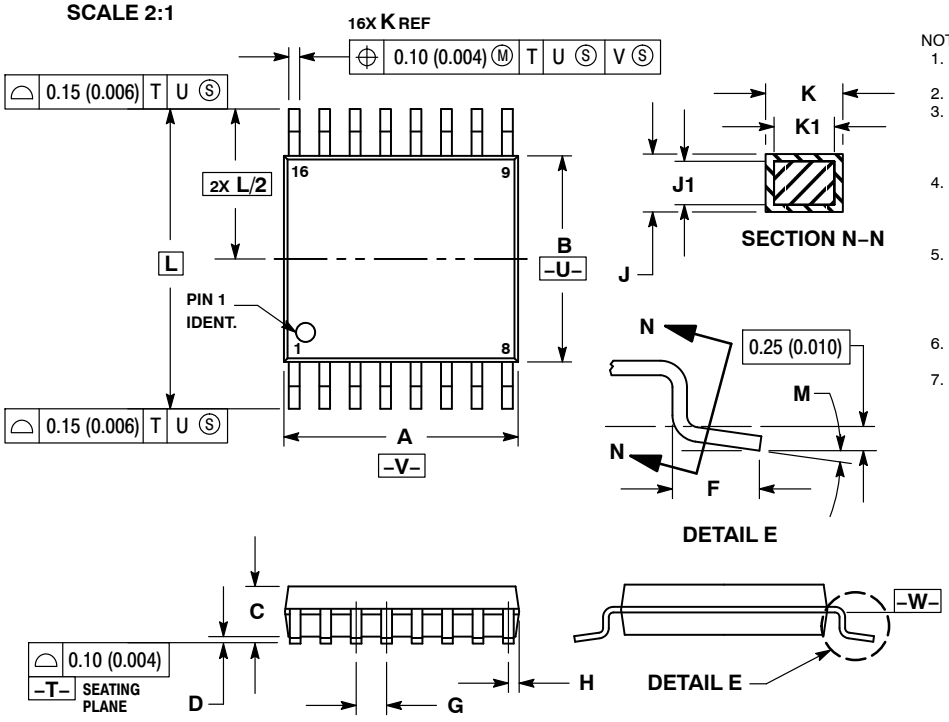
PIN	
1.	SOURCE N-CH
2.	COMMON DRAIN (OUTPUT)
3.	COMMON DRAIN (OUTPUT)
4.	GATE P-CH
5.	COMMON DRAIN (OUTPUT)
6.	COMMON DRAIN (OUTPUT)
7.	COMMON DRAIN (OUTPUT)
8.	SOURCE P-CH
9.	SOURCE P-CH
10.	COMMON DRAIN (OUTPUT)
11.	COMMON DRAIN (OUTPUT)
12.	COMMON DRAIN (OUTPUT)
13.	GATE N-CH
14.	COMMON DRAIN (OUTPUT)
15.	COMMON DRAIN (OUTPUT)
16.	SOURCE N-CH



SCALE 2:1

TSSOP−16 WB
CASE 948F
ISSUE B

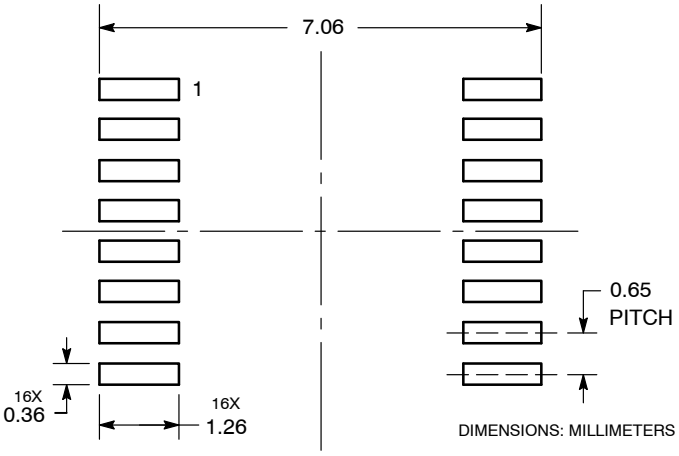
DATE 19 OCT 2006



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

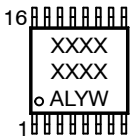
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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