3 A Ultra-Small Controlled Load Switch with Auto-Discharge Path and Reverse Current Control

NCP339

The NCP339 is a very low Ron MOSFET controlled by external logic pin, allowing optimization of battery life, and portable device autonomy.

Indeed, due to a current consumption optimization with PMOS structure, leakage currents are eliminated by isolating connected IC on the battery when not used.

Reverse blocking control is automatically engage if OUT pin voltage is higher than IN pin voltage, eliminate leakages current from OUT to IN.

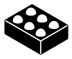
Proposed in a wide input voltage range from 1.2 V to 5.5 V, in a small 1 x 1.5 mm WLCSP6, pitch 0.5 mm.

Features

- 1.2 V – 5.5 V Operating Range
- 19 mΩ P MOSFET at 4.5 V
- DC Current up to 3 A
- Soft Start Control
- Low Quiescent Current
- Reverse Blocking
- Active High EN pin
- WLCSP6 1 x 1.5 mm
- This is a Pb−Free Device

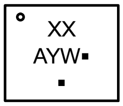
Typical Applications

- Mobile Phones
- Tablets
- Digital Cameras
- GPS
- Portable Devices
- Computers



WLCSP6, 1.00x1.50
CASE 567FH

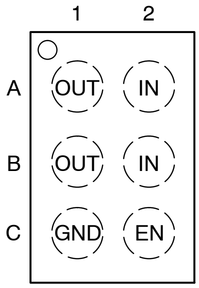
MARKING DIAGRAM



XX = NP or DP
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PACKAGE PINOUT DIAGRAM



(Top View)

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 9 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 9.

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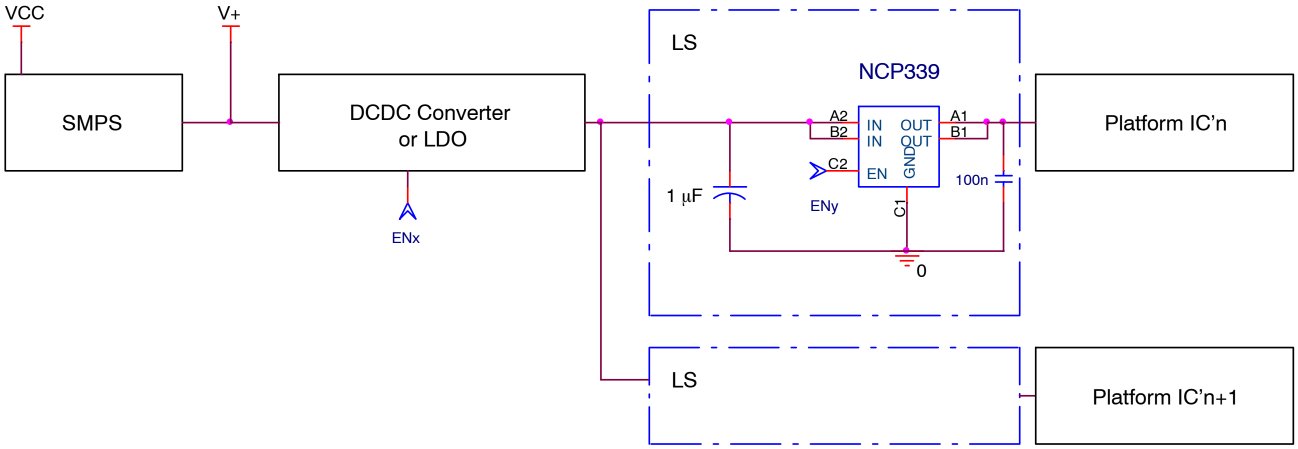


Figure 1. Typical Application Circuit

Table 1. PIN FUNCTION DESCRIPTION

Pin Name	Pin Number	Type	Description
IN	A2, B2	POWER	Load-switch input voltage; connect a 1 µF or greater ceramic capacitor from IN to GND as close as possible to the IC.
GND	C1	POWER	Ground connection.
EN	C2	INPUT	Enable input, logic high turns on power switch.
OUT	A1, B1	OUTPUT	Load-switch output; connect a 100 nF ceramic capacitor from OUT to GND as close as possible to the IC is recommended.

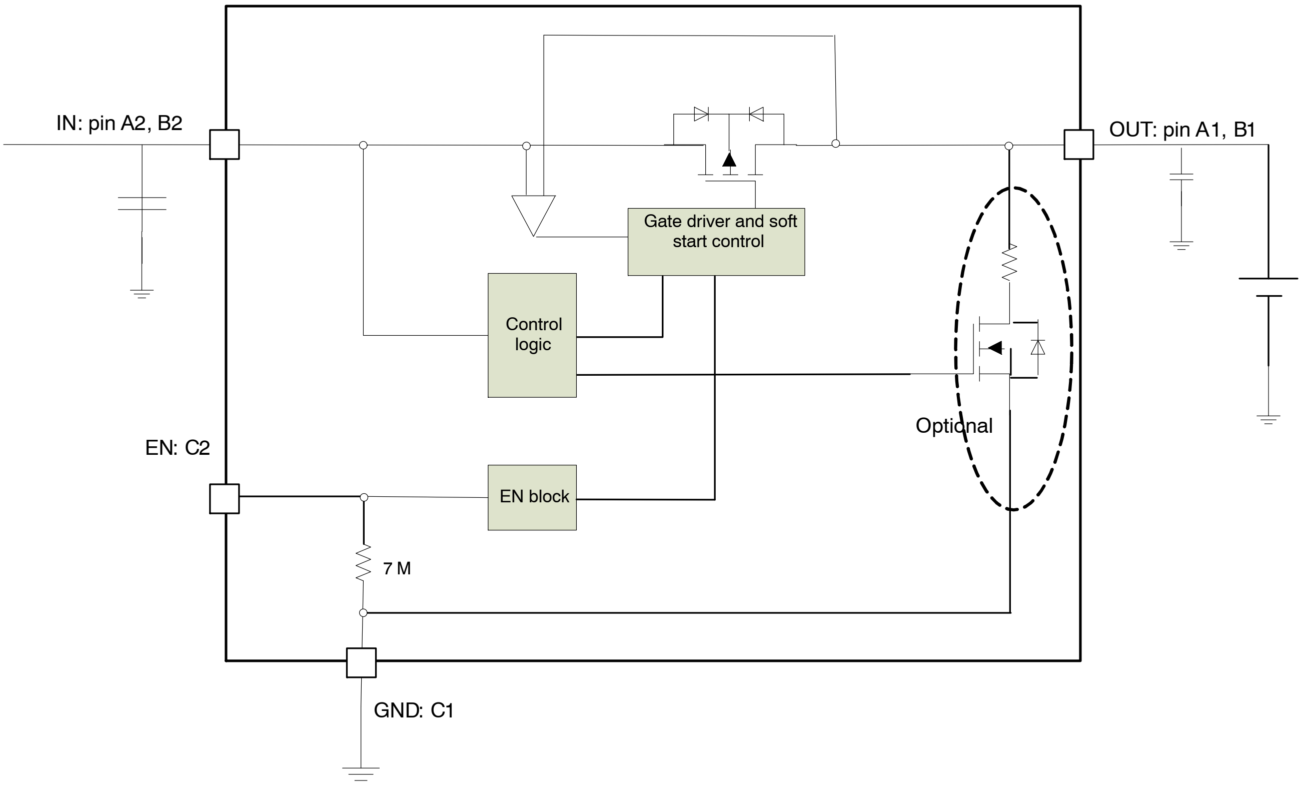


Figure 2. Block Diagram

Table 2. MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IN, OUT, EN, Pins: (Note 1)	V_{EN}, V_{IN}, V_{OUT}	-0.3 to +7.0	V
From IN to OUT Pins: Input/Output (Note 1)	V_{IN}, V_{OUT}	-7.0 to +7.0	V
Human Body Model (HBM) ESD Rating are (Note 1 and 2)	ESD HBM	4000	V
Machine Model (MM) ESD Rating are (Note 1 and 2)	ESD MM	250	V
Latch-up protection (Note 3) – Pins IN, OUT, EN	LU	100	mA
Maximum Junction Temperature	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-55 to +150	°C
Moisture Sensitivity (Note 4)	MSL	Level 1	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 3. OPERATING CONDITIONS

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IN}	Operational Power Supply			1.2		5.5	V
V_{EN}	Enable Voltage			0		5.5	
T_A	Ambient Temperature Range			-40	25	+85	°C
T_J	Junction Temperature Range			-40	25	+125	°C
C_{IN}	Decoupling input capacitor			1			μF
C_{OUT}	Decoupling output capacitor			100			nF
$R_{\theta JA}$	Thermal Resistance Junction to Air	WLCSP package (Note 3)			100		°C/W
I_{OUT}	Maximum DC current					3	A
P_D	Power Dissipation Rating (Note 4)	$T_A \le 25$ °C	WLCSP package		1		W
		$T_A = 85$ °C	WLCSP package		0.4		W

1. According to JEDEC standard JESD22-A108.
2. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J-STD-020.
3. The $R_{\theta JA}$ is dependent of the PCB heat dissipation and thermal via.
4. The maximum power dissipation ($_{PD}$) is given by the following formula:

$$P_D = \frac{T_{JMAX} - T_A}{R_{\theta JA}}$$

Table 4. ELECTRICAL CHARACTERISTICS

Min & Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.2 V to 5.5 V (Unless otherwise noted).
Typical values are referenced to T_A = +25°C and V_{IN} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
POWER SWITCH							
R_{DSON}	Static drain-source on-state resistance	Vin = 5.5 V	Iout = 200 mA, T_A = 25°C		18		mΩ
		Vin = 5.5 V	Tj = 125°C			30	
		Vin = 4.5 V	Iout = 200 mA, T_A = 25°C		19		
			Tj = 125°C			30	
		Vin = 3.3 V	Iout = 200 mA, T_A = 25°C		22		
			Tj = 125°C			30	
		Vin = 2.5 V	Iout = 200 mA, T_A = 25°C		27		
			Tj = 125°C			40	
		Vin = 1.8 V	Iout = 200 mA, T_A = 25°C		37		
			Tj = 125°C			60	
		Vin = 1.5 V	Iout = 200 mA, T_A = 25°C		48		
			Tj = 125°C			110	
Rdis	Output discharge path	EN = low	Discharge path option		70	90	Ω
V_{IH}	High-level input voltage			1.2			V
V_{IL}	Low-level input voltage					0.8	
R_{pd}	EN pull down resistor			5.5	7.1	9.5	MΩ
REVERSE CURRENT BLOCKING							
V_{rev_thr}	Reverse threshold	Vout-Vin			40		mV
V_{rev_hyst}	Reverse threshold hysteresis				60		mV
T_{rev}	Reverse comparator response time	Vout-Vin > V_{rev_thr}			2.5		µs
QUIESCENT CURRENT							
Istd	Standby current	Vin = 4.2 V	EN = low, No load, GND current		0.35	0.6	µA
I_{in_leak}	Mos leakage current	Vin = 4.2 V	EN = low, Vout = GND, Vout current		9	200	nA
Iq	Quiescent current	Vin = 4.2 V	EN = high, No load, GND current		1.0	1.5	µA
I_{out_leak}	Output leakage current	Vout = 4.2 V	Vin = GND		16	200	nA
TIMINGS							
T_{EN}	Enable time	Vin = 4.2 V (Note 6)	R_L = 5 Ω, Cout = 100 µF		1.7		ms
T_R	Output rise time				2.7		
T_{ON}	ON time (T_{EN} + T_R)				4.4		
T_F	Output fall time				1.5		
T_{EN}	Enable time	Vin = 4.2 V (Note 6)	R_L = 25 Ω, Cout = 1 µF	0.5	1.0	2.5	ms
T_R	Output rise time			0.4	1.5	2.3	
T_{ON}	ON time (T_{EN} + T_R)			0.9	2.5	4.8	
T_F	Output fall time				0.06	0.1	

5. Guaranteed by design and characterization.
6. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground.

Table 4. ELECTRICAL CHARACTERISTICS
Min & Max Limits apply for T_A between −40°C to +85°C for V_{IN} between 1.2 V to 5.5 V (Unless otherwise noted).
Typical values are referenced to T_A = +25°C and V_{IN} = 5 V (Unless otherwise noted).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
T_{EN}	Enable time	Vin = 4.2 V (Note 6)	R_L = 150 Ω, Cout = 100 µF		1.7		ms
T_R	Output rise time				1.5		
T_{ON}	ON time (T_{EN} + T_R)				3.2		
T_{DIS}	Disable time				1.8		
T_F	Fall time				4		
T_{OFF}	Output fall time (T_F + T_{DIS})				42		

5. Guaranteed by design and characterization.
6. Parameters are guaranteed for C_{LOAD} and R_{LOAD} connected to the OUT pin with respect to the ground.

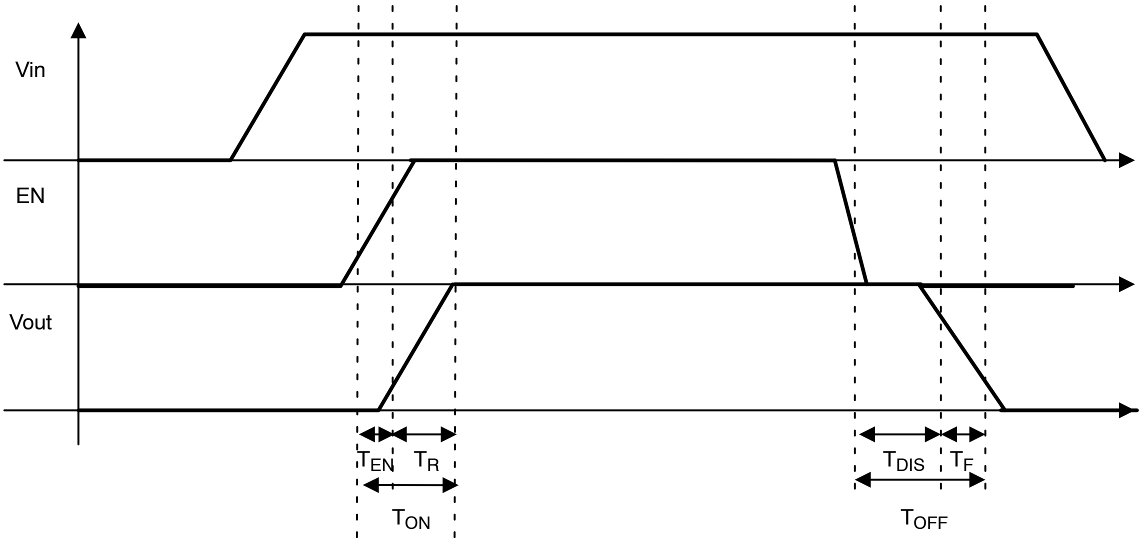


Figure 3. Timings

TYPICAL CHARACTERISTICS

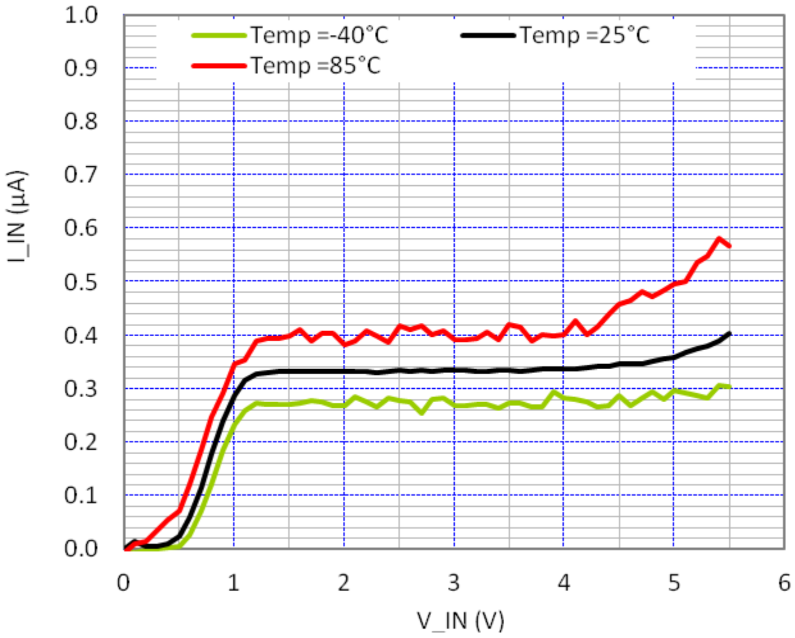


Figure 4. Standby Current (µA) versus Vin (V)

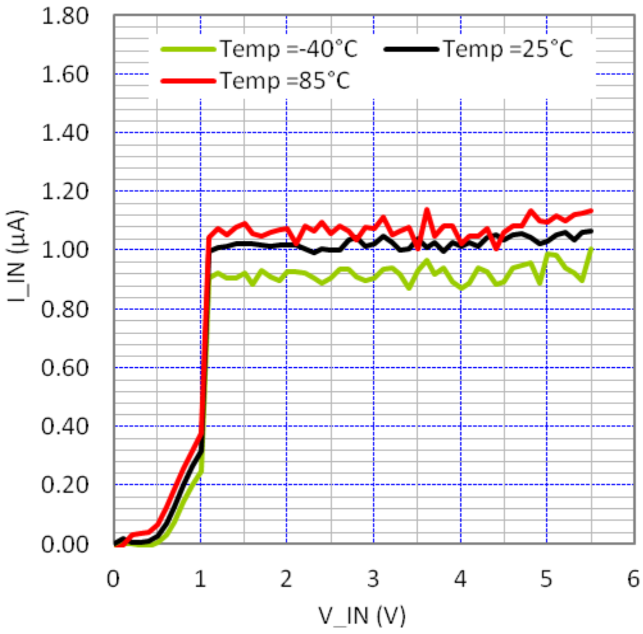


Figure 5. Quiescent Current (µA) versus Vin (V)

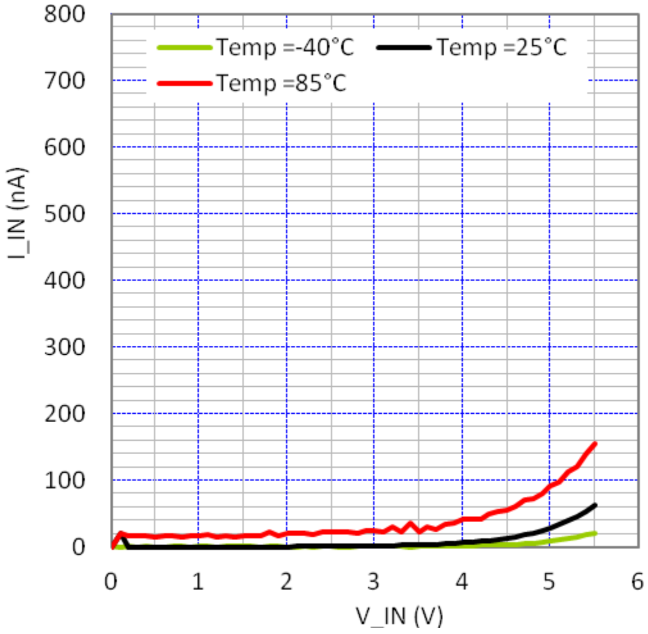


Figure 6. Reverse Current (nA) versus Vin (V)

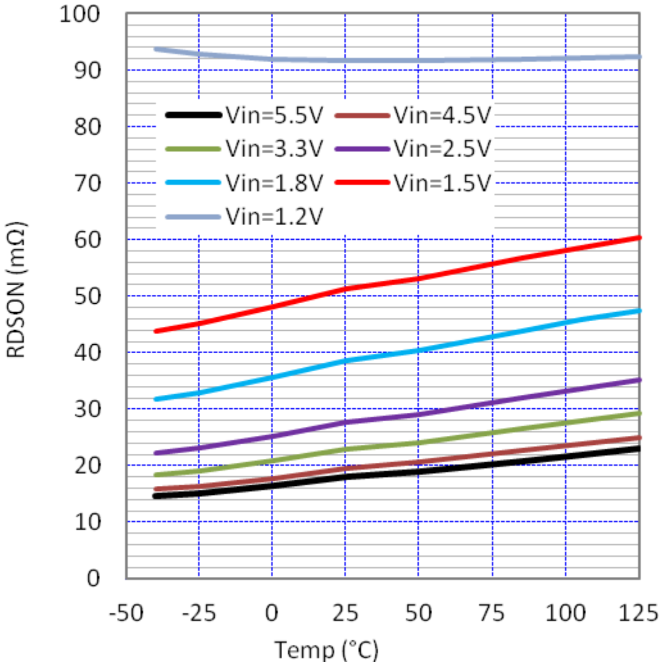


Figure 7. R_{DSON} (mΩ) versus Temperature (I_{LOAD} = 100 mA)

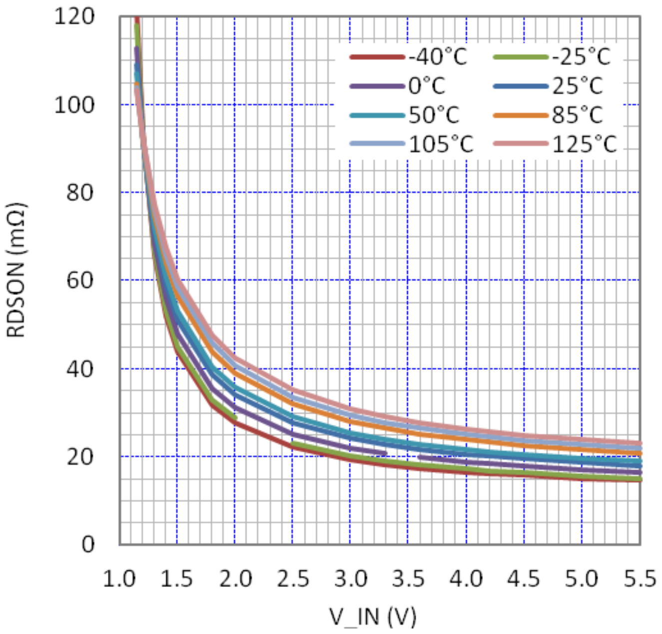


Figure 8. R_{DSON} (mΩ) versus Vin (V)

FUNCTIONAL DESCRIPTION

Overview

The NCP339 is a high side P channel MOSFET power distribution switch designed to isolate ICs connected on the battery in order to save energy. The part can be turned on, with a wide range of battery from 1.2 V to 5.5 V. Reverse blocking from output to input control is embedded in the IC to eliminate leakage current if Vout voltage exceed front end power supply.

Enable Input

Enable pin is an active high. The path is opened when EN pin is tied low (disable), forcing P MOS switch off.

The IN/OUT path is activated with a minimum of Vin of 1.2 V and EN forced to high level.

Blocking Control

The reverse blocking feature allows to avoid reverse current, through the PMOS fet if a voltage is applied on Vout pin, and V_{rev_thr} above the Vin pin. This function is available, whatever the EN logic pin state (High or low). To retrieve normal state, Vin-Vout must be higher to hysteresis of the reverse blocking comparator (V_{rev_hyst}). The reverse blocking comparator response time is set to T_{rev}.

Table 5. CONTROL LOGIC

V_{IN}	V_{OUT}	EN
Present	Mos OFF	Low
Present	Mos ON	High
Mos OFF	$V_{OUT} > V_{IN}$	x

Auto Discharge (Optional)

NMOS FET is placed between the output pin and GND, in order to discharge the application capacitor connected on OUT pin.

The auto-discharge is activated when EN pin is set to low level (disable state).

The discharge path (Pull down NMOS) stays activated as long as EN pin is set at low level and Vin > 1.2 V.

In order to limit the current across the internal discharge Nmosfet, the typical value is set at 70 Ω.

Cin and Cout Capacitors

Cin 1 μF and Cout 100 nF , at least, capacitors must be placed as close as possible the part to for stability improvement.

For inrush effects at start up, it’s recommended to respect Cin > Cout size.

APPLICATION INFORMATION

Power Dissipation

Main contributor in term of junction temperature is the power dissipation of the power MOSFET. Assuming this, the power dissipation and the junction temperature in normal mode can be calculated with the following equations:

- $P_D = R_{DS(on)} \times (I_{OUT})^2$

P_D = Power dissipation (W)
$R_{DS(on)}$ = Power MOSFET on resistance (Ω)
I_{OUT} = Output current (A)

- $T_J = P_D \times R_{\theta JA} + T_A$

T_J = Junction temperature (°C)
$R_{\theta JA}$ = Package thermal resistance (°C/W)
T_A = Ambient temperature (°C)

PCB Recommendations

The NCP339 integrates an up to 3 A rated PMOS FET, and the PCB design rules must be respected to properly

evacuate the heat out of the silicon. By increasing PCB area, especially around IN and OUT pins, the $R_{\theta JA}$ of the package can be decreased, allowing higher power dissipation.

Routing example: 2 oz, 4 layers with vias across 2 internal inners.

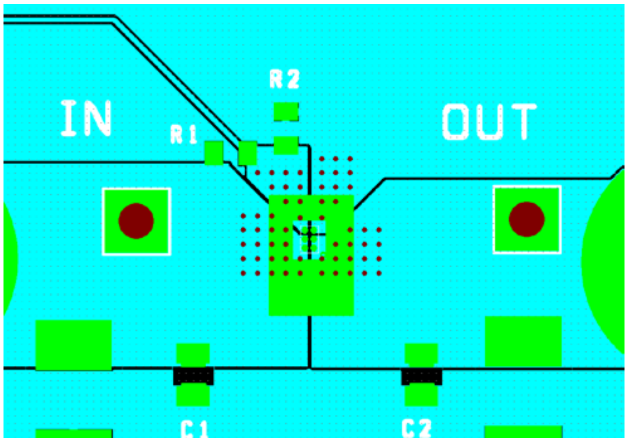


Figure 9.

Example of application definition.

$T_J - T_A = R_{\theta JA} \times P_D = R_{\theta JA} \times R_{DSON} \times I^2$

T_J: junction temperature.
T_A: ambient temperature.
R_θ = Thermal resistance between IC and air, through PCB.
R_{DSON}: intrinsic resistance of the IC Mosfet.
I: load DC current.

Taking into account of R_θ obtain with:

- 1 oz, 2 layers: 100°C/W.

At 3 A, 25°C ambient temperature, R_{DSON} 20 mΩ @ Vin 5 V, the junction temperature will be:

$T_J = T_A + R_\theta \times P_D = 25 + (0.02 \times 3^2) \times 100 = 43°C$

Taking into account of R_θ obtain with:

- 2 oz, 4 layers: 60°C/W.

At 3 A, 65°C ambient temperature, R_{DSON} 24 mΩ @ Vin 5 V, the junction temperature will be:

$T_J = T_A + R_\theta \times P_D = 65 + (0.024 \times 3^2) \times 60 = 78°C$

ORDERING INFORMATION

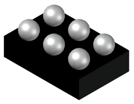
Device	Marking	Option	Package	Shipping†
NCP339BFCT2G	DP	With Auto−discharge	WLCSP6, 1 x 1.5 mm (Pb−Free)	3000 / Tape & Reel

DISCONTINUED (Note 7)

NCP339AFCT2G	NP	Without Auto−discharge	WLCSP6, 1 x 1.5 mm (Pb−Free)	3000 / Tape & Reel

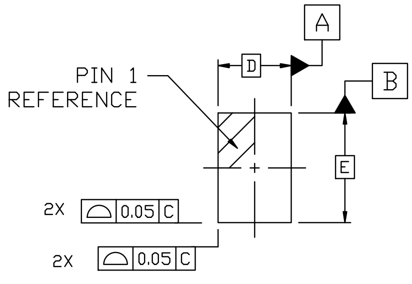
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

7. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.



WLCSP6 1.0x1.5x0.609
CASE 567FH
ISSUE A

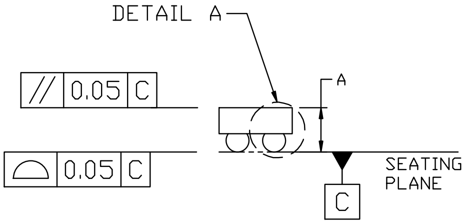
DATE 21 JUN 2022



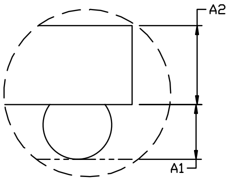
TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.

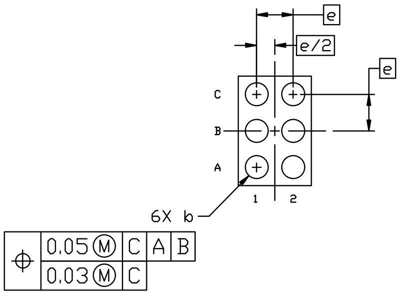


SIDE VIEW

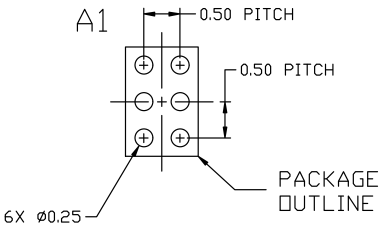


DETAIL A
SCALE 1:3

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.554	0.609	0.664
A1	0.219	0.249	0.279
A2	0.335	0.360	0.385
b	0.282	0.312	0.342
D	1.00 BSC		
E	1.50 BSC		
e	0.50 BSC		



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*

XXX
AYW
▪

XXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WLCSP6 1.0x1.5x0.609**	**PAGE 1 OF 1**

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