Enhanced, High-Efficiency Power Factor Controller

The 6-pin PFC controller NCP1602 is designed to drive PFC boost stages. It is based on an innovative Valley Synchronized Frequency Fold-back (VSFF) method. In this mode, the circuit classically operates in Critical conduction Mode (CrM) when \( V_{\text{control}} \) voltage exceeds a programmable value \( V_{\text{ctrl,FF}} \). When \( V_{\text{control}} \) is below this preset level \( V_{\text{ctrl,FF}} \), the NCP1602 (versions [B**] and [D**]) linearly decays the frequency down to about 30 kHz until \( V_{\text{control}} \) reaches the SKIP mode threshold. VSFF maximizes the efficiency at both nominal and light load. In particular, the stand–by losses are reduced to a minimum. Like in FCCrM controllers, internal circuitry allows near–unity power factor even when the switching frequency is reduced. Housed in a TSOP6 package, the circuit also incorporates the features necessary for robust and compact PFC stages, with few external components.

**General Features**
- Near–Unity Power Factor
- Two–Level Boost Follower Line Level Dependent (disabled by default)
- Critical Conduction Mode (CrM)
- Valley Synchronized Frequency Fold–back (VSFF): Low Frequency Operation is Forced at Low Current Levels
- Works With or Without a Transformer w/ ZCD Winding (simple inductor)
- On–time Modulation to Maintain a Proper Current Shaping in VSFF Mode
- Skip Mode at Very Low Load Current (versions [B**] and [D**])
- Fast Line / Load Transient Compensation (Dynamic Response Enhancer)
- Valley Turn–on
- High Drive Capability: −500 mA / +800 mA
- \( V_{\text{CC}} \) Range: from 9.5 V to 30 V
- Low Start–up Consumption for:
  - [**C] & [**D] Versions: Low \( V_{\text{cc}} \) Start–up level (10.5 V)
  - [**A] & [**B] Versions: High \( V_{\text{cc}} \) Start–up level (17.0 V)
- Line Range Detection for Reduced Crossover Frequency Spread
- This is a Pb–Free Device

**Safety Features**
- Thermal Shutdown
- Non–latching, Over–Voltage Protection
- Second Over–Voltage Protection
- Brown–Out Detection
- Over Current Limitation
- Disable Protection if the Feedback Pin is Not Connected
- Low Duty–Cycle Operation if the Bypass Diode is Shorted
- Open Ground Pin Fault Monitoring

**Typical Applications**
- PC Power Supplies
- Lighting Ballasts (LED, Fluorescent)
- Flat TV
- All Off Line Appliances Requiring Power Factor Correction
**DEVICE ORDERING INFORMATION**

<table>
<thead>
<tr>
<th>Operating Part Number (OPN)</th>
<th>L1, L2, L3 Option</th>
<th>Marking</th>
<th>Package Type</th>
<th>Shipping</th>
</tr>
</thead>
<tbody>
<tr>
<td>NCP1602ABASNT1G</td>
<td>ABA</td>
<td>ABA</td>
<td>TSOP–6 (Pb–Free)</td>
<td>3000 / Tape &amp; Reel</td>
</tr>
<tr>
<td>NCP1602ACCSNT1G</td>
<td>ACC</td>
<td>A6C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1602AEASNT1G</td>
<td>AEA</td>
<td>AEA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1602AFCSNT1G</td>
<td>AFC</td>
<td>AFC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1602BEASNT1G</td>
<td>BEA</td>
<td>2EA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1602DCCSNT1G</td>
<td>DCC</td>
<td>DCC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>NCP1602DFCSNT1G</td>
<td>DFC</td>
<td>DFC</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTE: Other L1, L2, L3 combinations are available upon request.
Product versions are coded with three letters (L1,L2,L3).

<table>
<thead>
<tr>
<th>Table 1. NCP1602 1st LETTER CODING OF PRODUCT VERSIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
</tr>
<tr>
<td>----</td>
</tr>
<tr>
<td>A</td>
</tr>
<tr>
<td>B</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>D</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 2. NCP1602 2nd LETTER CODING OF PRODUCT VERSIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>L2</td>
</tr>
<tr>
<td>----</td>
</tr>
<tr>
<td>B</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>E</td>
</tr>
<tr>
<td>F</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 3. NCP1602 3rd LETTER CODING OF PRODUCT VERSIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td>L3</td>
</tr>
<tr>
<td>----</td>
</tr>
<tr>
<td>A</td>
</tr>
<tr>
<td>B</td>
</tr>
<tr>
<td>C</td>
</tr>
<tr>
<td>D</td>
</tr>
</tbody>
</table>
Figure 1. NCP1602 Application Schematic

Table 4. DETAILED PIN DESCRIPTION

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Name</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VCTRL</td>
<td>The error amplifier output is available on this pin. The network connected between this pin and ground adjusts the regulation loop bandwidth that is typically set below 20 Hz to achieve high Power Factor ratios. VCTRL pin is internally pulled down when the circuit is off so that when it starts operation, the power increases slowly to provide a soft−start function. VCTRL pin must not be controlled or pulled down externally.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>Connect this pin to the PFC stage ground.</td>
</tr>
<tr>
<td>3</td>
<td>CS / ZCD</td>
<td>This pin monitors the MOSFET current to limit its maximum current. This pin is the output of a resistor bridge connected between the drain and the source of the power MOSFET. Internal circuitry takes care of extracting $V_{in}$, $V_{out}$, $I_{ind}$ and ZCD.</td>
</tr>
<tr>
<td>4</td>
<td>DRV</td>
<td>The high−current capability of the totem pole gate drive (−0.5/+0.8A) makes it suitable to effectively drive high gate charge power MOSFETs.</td>
</tr>
<tr>
<td>5</td>
<td>VCC</td>
<td>This pin is the positive supply of the IC. The circuit starts to operate when VCC exceeds 17.0 V ([<strong>A</strong>] &amp; [<strong>B</strong>] Versions) or 10.5 V ([<strong>C</strong>] &amp; [<strong>D</strong>] Versions) and turns off when VCC goes below 9.0 V (typical values). After start−up, the operating range is 9.5 V up to 30 V.</td>
</tr>
<tr>
<td>6</td>
<td>FB</td>
<td>This pin receives a portion of the PFC output voltage for the regulation and the Dynamic Response Enhancer (DRE) that drastically speeds−up the loop response when the output voltage drops below 95.5% of the desired output level. FB pin voltage $V_{FB}$ is also the input signal for the (non−latching) Over−Voltage (OVP) and Under−Voltage (UVP) comparators. The UVP comparator prevents operation as long as FB pin voltage is lower than $V_{UVPH}$ internal voltage reference. A SOFTOVP comparator gradually reduces the duty−ratio when FB pin voltage exceeds 105% of $V_{REF}$. If the output voltage still increases, the driver is immediately disabled if the output voltage exceeds 107% of the desired level (fast OVP). A 250−nA sink current is built−in to trigger the UVP protection and disable the part if the feedback pin is accidently open.</td>
</tr>
</tbody>
</table>
### Table 5. MAXIMUM RATINGS TABLE

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Pin</th>
<th>Rating</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCTRL</td>
<td>1</td>
<td>VCONTROL pin</td>
<td>−0.3, V_{ctrl,max}(*)</td>
<td>V</td>
</tr>
<tr>
<td>CS/ZCD</td>
<td>3</td>
<td>CS/ZCD Pin</td>
<td>−0.3, +9</td>
<td>V</td>
</tr>
<tr>
<td>DRV</td>
<td>4</td>
<td>Driver Voltage</td>
<td>−0.3, V_{DRV} (*)</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Driver Current</td>
<td>−500, +800</td>
<td>mA</td>
</tr>
<tr>
<td>VCC</td>
<td>5</td>
<td>Power Supply Input</td>
<td>−0.3, + 30</td>
<td>V</td>
</tr>
<tr>
<td>FB</td>
<td>6</td>
<td>Feedback Pin</td>
<td>TBD upon test engineer</td>
<td>V/s</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>measurements</td>
<td></td>
</tr>
<tr>
<td>P_{D}</td>
<td></td>
<td>Power Dissipation and Thermal Characteristics</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{JA}</td>
<td></td>
<td>Maximum Power Dissipation at T_{A}=70°C</td>
<td>550, 145</td>
<td>mW/°C</td>
</tr>
<tr>
<td>T_{J}</td>
<td></td>
<td>Operating Junction Temperature Range</td>
<td>−40 to +125</td>
<td>°C</td>
</tr>
<tr>
<td>T_{J,max}</td>
<td></td>
<td>Maximum Junction Temperature</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>T_{S,max}</td>
<td></td>
<td>Storage Temperature Range</td>
<td>−65 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>T_{L,max}</td>
<td></td>
<td>Lead Temperature (Soldering, 10 s)</td>
<td>300</td>
<td>°C</td>
</tr>
<tr>
<td>MSL</td>
<td></td>
<td>Moisture Sensitivity Level</td>
<td>1</td>
<td>–</td>
</tr>
<tr>
<td>ESD Capability, HBM model (Note 1)</td>
<td></td>
<td></td>
<td>&gt; 2000</td>
<td>V</td>
</tr>
<tr>
<td>ESD Capability, Charged Device Model (Note 1)</td>
<td></td>
<td></td>
<td>&gt; 1500</td>
<td>V</td>
</tr>
</tbody>
</table>

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**“V_{ctrl,max}”** is the VCTRL pin clamp voltage. **“V_{DRV}”** is the DRV clamp voltage (V_{DRVhigh}) if V_{CC} is higher than (V_{DRVhigh}). **“V_{DRV}”** is V_{CC} otherwise.

1. This device(s) contains ESD protection and exceeds the following tests:
   - Human Body Model 2000 V per JEDEC Standard JESD22–A114E
   - Charged Device Model Method 1500 V per JEDEC Standard JESD22–C101E.
2. This device contains latch–up protection and exceeds 100 mA per JEDEC Standard JESD78.
Table 6. TYPICAL ELECTRICAL CHARACTERISTICS
(Conditions: \( V_{CC} = 18 \) V, \( T_J \) from \(-40^\circ C \) to \(+125^\circ C \), unless otherwise specified) (Note 3)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CC,on} )</td>
<td>Start-Up Threshold, ( V_{CC} ) increasing:</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>[**C] &amp; [**D] Versions [**A] &amp; [**B] Versions</td>
<td>9.75</td>
<td>15.80</td>
<td>11.25</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CC,off} )</td>
<td>Minimum Operating Voltage, ( V_{CC} ) falling</td>
<td>8.50</td>
<td>9.00</td>
<td>9.50</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CC,hyst} )</td>
<td>Hysteresis ( (V_{CC,on} - V_{CC,off}) )[**C] &amp; [**D] Versions [**A] &amp; [**B] Versions</td>
<td>0.75</td>
<td>1.50</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6.00</td>
<td>8.00</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>( I_{CC,start} )</td>
<td>Maximum Start-Up Current, for ( V_{CC} ) lower than 9.4 V, below startup voltage</td>
<td>–</td>
<td>–</td>
<td>480</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{CC,op1} )</td>
<td>Operating Consumption, no switching.</td>
<td>–</td>
<td>0.5</td>
<td>1.00</td>
<td>mA</td>
</tr>
<tr>
<td>( I_{CC,op2} )</td>
<td>Operating Consumption, 50–kHz switching, no load on DRV pin</td>
<td>–</td>
<td>2.00</td>
<td>3.00</td>
<td>mA</td>
</tr>
<tr>
<td>( t_{DT,B,1} )</td>
<td>Dead–Time, ( V_{ctrl} ) = 0.65 V w/ B config</td>
<td>5.73</td>
<td>7.64</td>
<td>9.55</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{DT,B,2} )</td>
<td>Dead–Time, ( V_{ctrl} ) = 0.75 V w/ B config</td>
<td>2.91</td>
<td>3.88</td>
<td>4.85</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{DT,C,1} )</td>
<td>Dead–Time, ( V_{ctrl} ) = 0.65 V w/ C config</td>
<td>8.90</td>
<td>11.90</td>
<td>14.84</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{DT,C,2} )</td>
<td>Dead–Time, ( V_{ctrl} ) = 0.75 V w/ C config</td>
<td>5.69</td>
<td>7.50</td>
<td>9.48</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{DT,E,1} )</td>
<td>Dead–Time, ( V_{ctrl} ) = 0.65 V w/ E config</td>
<td>9.96</td>
<td>13.28</td>
<td>16.60</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{DT,E,2} )</td>
<td>Dead–Time, ( V_{ctrl} ) = 0.75 V w/ E config</td>
<td>6.70</td>
<td>8.93</td>
<td>10.80</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{DT,F,1} )</td>
<td>Dead–Time, ( V_{ctrl} ) = 0.65 V w/ F config</td>
<td>13.00</td>
<td>17.30</td>
<td>21.66</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( t_{DT,F,2} )</td>
<td>Dead–Time, ( V_{ctrl} ) = 0.75 V w/ F config</td>
<td>9.97</td>
<td>13.10</td>
<td>16.61</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( V_{CrM,th,B} )</td>
<td>( V_{ctrl} ) threshold CrM to DCM mode w/ B config</td>
<td>0.923</td>
<td>1.026</td>
<td>1.129</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CrM,th,C} )</td>
<td>( V_{ctrl} ) threshold CrM to DCM mode w/ C config</td>
<td>1.16</td>
<td>1.29</td>
<td>1.43</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CrM,th,E} )</td>
<td>( V_{ctrl} ) threshold CrM to DCM mode w/ E config</td>
<td>1.398</td>
<td>1.553</td>
<td>1.708</td>
<td>V</td>
</tr>
<tr>
<td>( V_{CrM,th,F} )</td>
<td>( V_{ctrl} ) threshold CrM to DCM mode w/ F config</td>
<td>1.865</td>
<td>2.08</td>
<td>2.29</td>
<td>V</td>
</tr>
<tr>
<td>( V_{SKIP-H} )</td>
<td>( V_{ctrl} ) pin SKIP Level, ( V_{control} ) rising</td>
<td>555</td>
<td>617</td>
<td>678</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{SKIP-L} )</td>
<td>( V_{ctrl} ) pin SKIP Level, ( V_{control} ) falling</td>
<td>516</td>
<td>593</td>
<td>665</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{SKIP-Hyst} )</td>
<td>( V_{ctrl} ) pin SKIP Hysteresis</td>
<td>–</td>
<td>30</td>
<td>–</td>
<td>mV</td>
</tr>
<tr>
<td>( t_R )</td>
<td>Output voltage rise–time @ ( C_L = 1 ) nF, 10–90% of output signal</td>
<td>–</td>
<td>30</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>( t_F )</td>
<td>Output voltage fall–time @ ( C_L = 1 ) nF, 10–90% of output signal</td>
<td>–</td>
<td>20</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>( R_{OH} )</td>
<td>Source resistance @ 200 mV under High VCC</td>
<td>–</td>
<td>10</td>
<td>–</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( R_{OL} )</td>
<td>Sink resistance @200 mV above Low VCC</td>
<td>–</td>
<td>7</td>
<td>–</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>( V_{DRV,low} )</td>
<td>DRV pin level for ( V_{CC} = V_{CC,off} +200 ) mV (10–k( \Omega ) resistor between DRV and GND)</td>
<td>8.0</td>
<td>–</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>( V_{DRV,high} )</td>
<td>DRV pin level at ( V_{CC} = 30 ) V (( R_L = 33 ) k( \Omega ) &amp; ( C_L = 1 ) nF)</td>
<td>10</td>
<td>12</td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td>( V_{REF} )</td>
<td>Feedback Voltage Reference</td>
<td>2.44</td>
<td>2.50</td>
<td>2.56</td>
<td>V</td>
</tr>
<tr>
<td>( V_{REF2,HL} )</td>
<td>Feedback Voltage Reference #2 @ High Line</td>
<td>2.44</td>
<td>2.50</td>
<td>2.56</td>
<td>V</td>
</tr>
<tr>
<td>( V_{REF2,LL} )</td>
<td>Feedback Voltage Reference #2 @ Low Line</td>
<td>1.56</td>
<td>1.60</td>
<td>1.64</td>
<td>V</td>
</tr>
<tr>
<td>( I_{EA} )</td>
<td>Error Amplifier Current Capability, Sinking and Sourcing</td>
<td>15</td>
<td>20</td>
<td>26</td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

3. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.
### Table 6. TYPICAL ELECTRICAL CHARACTERISTICS

(Conditions: \( V_{CC} = 18 \) V, \( T_J \) from \(-40^\circ C \) to \(+125^\circ C \), unless otherwise specified) (Note 3)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>REGULATION BLOCK</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( G_{EA} )</td>
<td>Error Amplifier Gain</td>
<td>110</td>
<td>200</td>
<td>290</td>
<td>( \mu S )</td>
</tr>
<tr>
<td>( V_{ctrl} )</td>
<td>VCTRL pin Voltage (( V_{ctrl} )):</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{ctrl,min} ) @ ( V_FB = 2 ) V (OTA is sourcing 20 ( \mu A ))</td>
<td>–</td>
<td>4.5</td>
<td>–</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{ctrl,max} ) @ ( V_FB = 3 ) V (OTA is sinking 20 ( \mu A ))</td>
<td>–</td>
<td>0.5</td>
<td>–</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{out,L} / V_{REF2} ) Ratio (( V_{out} ) Low Detect Threshold / ( V_{REF} ))</td>
<td>–</td>
<td>95.5</td>
<td>–</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( H_{out,L} / V_{REF2} ) Ratio (( V_{out} ) Low Detect Hysteresis / ( V_{REF} ))</td>
<td>–</td>
<td>0.35</td>
<td>–</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>( I_{BOOST} )</td>
<td>VCTRL pin Source Current when (( V_{OUT} ) Low Detect) is activated</td>
<td>147</td>
<td>220</td>
<td>277</td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>CURRENT SENSE AND ZERO CURRENT DETECTION BLOCKS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{CS,(R)} )</td>
<td>Current Sense Voltage Reference</td>
<td>450</td>
<td>500</td>
<td>550</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{CS,OVS,(R)} )</td>
<td>Current Sense Overstress Voltage Reference</td>
<td>675</td>
<td>750</td>
<td>825</td>
<td>mV</td>
</tr>
<tr>
<td>( I_{LEB,OVS} )</td>
<td>“Overstress” Leading edge Blanking Time (guaranteed by design)</td>
<td>–</td>
<td>250</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>( I_{LEB,OCP} )</td>
<td>“Over−Current Protection” Leading edge Blanking Time (guaranteed by design)</td>
<td>–</td>
<td>400</td>
<td>–</td>
<td>ns</td>
</tr>
<tr>
<td>( I_{OCP} )</td>
<td>Over−Current Protection Delay from ( V_{CS,ZCD} &gt; V_{CS,(R)} ) to DRV low (( V_{CS,ZCD} / \frac{dI}{dt} = 10 ) ( V/\mu A ))</td>
<td>–</td>
<td>40</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>( V_{ZCD,(H)} )</td>
<td>Zero Current Detection, ( V_{CS,ZCD} ) rising</td>
<td>8</td>
<td>35</td>
<td>62</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{ZCD,(L)} )</td>
<td>Zero Current Detection, ( V_{CS,ZCD} ) falling</td>
<td>–68</td>
<td>–46</td>
<td>–25</td>
<td>mV</td>
</tr>
<tr>
<td>( V_{ZCD,(hyst)} )</td>
<td>Hysteresis of the Zero Current Detection Comparator</td>
<td>46</td>
<td>84</td>
<td>–</td>
<td>mV</td>
</tr>
</tbody>
</table>

To discuss versus what esd protection will be used

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CL,(pos)} )</td>
<td>CS/ZCD Positive Clamp @ ( I_{CS,ZCD} = 5 ) mA (guaranteed by design)</td>
<td>–</td>
<td>9.5</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>( I_{ZCD} )</td>
<td>(( V_{CS,ZCD} &lt; V_{ZCD,(H)} )) to (DRV high)</td>
<td>–</td>
<td>60</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>( I_{SYNC} )</td>
<td>Minimum ZCD Pulse Width</td>
<td>–</td>
<td>110</td>
<td>200</td>
<td>ns</td>
</tr>
<tr>
<td>( I_{WDG} )</td>
<td>Watch Dog Timer</td>
<td>80</td>
<td>200</td>
<td>320</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{WDG(OS)} )</td>
<td>Watch Dog Timer in “OverStress” Situation</td>
<td>400</td>
<td>800</td>
<td>1200</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{ZCD,(neg)} )</td>
<td>Source Current for CS/ZCD pin impedance Testing</td>
<td>–</td>
<td>50</td>
<td>–</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{ZCD,(VCC)} )</td>
<td>Pull−up current source referenced to ( V_{CC} ) for open pin detection</td>
<td>–</td>
<td>200</td>
<td>–</td>
<td>nA</td>
</tr>
</tbody>
</table>

**STATIC OVP**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( D_{MIN} )</td>
<td>Duty Cycle, ( V_FB = 3 ) V (When low clamp of ( V_{ctrl} ) is reached)</td>
<td>–</td>
<td>–</td>
<td>0</td>
<td>%</td>
</tr>
</tbody>
</table>

**ON−TIME CONTROL (Options [*E*], [*B*], [*F*], [*C*] for maximum \( I_{ON} \) value)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{ON,LL,B} )</td>
<td>Maximum On Time, avg(( V_{GC} )) = 0.9 V and ( V_{ctrl} ) maximum (CrM)</td>
<td>22</td>
<td>25</td>
<td>28</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{ON,HL,B} )</td>
<td>Maximum On Time, avg(( V_{GC} )) = 2.8 V and ( V_{ctrl} ) maximum (CrM)</td>
<td>7.49</td>
<td>8.33</td>
<td>9.16</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{ON,LL,C} )</td>
<td>Maximum On Time, avg(( V_{GC} )) = 0.9 V and ( V_{ctrl} ) maximum (CrM)</td>
<td>22</td>
<td>25</td>
<td>28</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{ON,HL,C} )</td>
<td>Maximum On Time, avg(( V_{GC} )) = 2.8 V and ( V_{ctrl} ) maximum (CrM)</td>
<td>7.49</td>
<td>8.40</td>
<td>9.16</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{ON,LL,E} )</td>
<td>Maximum On Time, avg(( V_{GC} )) = 0.9 V and ( V_{ctrl} ) maximum (CrM)</td>
<td>11.4</td>
<td>12.5</td>
<td>13.6</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{ON,HL,E} )</td>
<td>Maximum On Time, avg(( V_{GC} )) = 2.8 V and ( V_{ctrl} ) maximum (CrM)</td>
<td>3.75</td>
<td>4.17</td>
<td>4.59</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{ON,LL,F} )</td>
<td>Maximum On Time, avg(( V_{GC} )) = 0.9 V and ( V_{ctrl} ) maximum (CrM)</td>
<td>11.4</td>
<td>12.5</td>
<td>13.6</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( I_{ON,HL,F} )</td>
<td>Maximum On Time, avg(( V_{GC} )) = 2.8 V and ( V_{ctrl} ) maximum (CrM)</td>
<td>3.75</td>
<td>4.20</td>
<td>4.59</td>
<td>( \mu s )</td>
</tr>
<tr>
<td>( K_{I_{ON,LL−HL}} )</td>
<td>( I_{ON} ) @LL over ( I_{ON} ) @HL ratio (all ( I_{ON} ) versions)</td>
<td>–</td>
<td>3</td>
<td>–</td>
<td>w/o</td>
</tr>
</tbody>
</table>

Specifying max \( I_{ON,\text{min}} \) means \( I_{ON,\text{min}} \) can go down to zero

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{ON,LL,min} )</td>
<td>Minimum On Time, avg(( V_{GC} )) = 0.9 V (not tested, guaranteed by design)</td>
<td>–</td>
<td>300</td>
<td>–</td>
<td>ns</td>
</tr>
</tbody>
</table>

3. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.
Table 6. TYPICAL ELECTRICAL CHARACTERISTICS
(Conditions: \( V_{CC} = 18 \) V, \( T_J \) from −40°C to +125°C, unless otherwise specified) (Note 3)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{on,HL,min} )</td>
<td>Minimum On Time, ( \text{avg}(V_{cs}) = 2.8 ) V (not tested, guaranteed by design)</td>
</tr>
</tbody>
</table>

**FEED-BACK OVER AND UNDER-VOLTAGE PROTECTIONS (OVP and UVP)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{softOVP} )</td>
<td>Ratio (Soft OVP Threshold, ( V_{FB} ) rising) over ( V_{REF} ) (or ( V_{REF2} )) (guaranteed by design)</td>
</tr>
<tr>
<td>( R_{softOVP(HYST)} )</td>
<td>Ratio (Soft OVP Hysteresis) over ( V_{REF} ) (or ( V_{REF2} )) (guaranteed by design)</td>
</tr>
<tr>
<td>( R_{fastOVP} )</td>
<td>Ratio (Fast OVP Threshold, ( V_{FB} ) rising) over ( V_{REF} ) (or ( V_{REF2} )) (guaranteed by design)</td>
</tr>
<tr>
<td>( R_{fastOVP(HYST)} )</td>
<td>Ratio (Fast OVP Hysteresis) over ( V_{REF} ) (or ( V_{REF2} )) (guaranteed by design)</td>
</tr>
<tr>
<td>( V_{UVPH} )</td>
<td>UVP Threshold, ( V_{FB} ) increasing</td>
</tr>
<tr>
<td>( V_{UVPL} )</td>
<td>UVP Threshold, ( V_{FB} ) decreasing</td>
</tr>
<tr>
<td>( I_{FB} )</td>
<td>FB pin Bias Current @ ( V_{FB} = V_{OVP} ) and ( V_{FB} = V_{UV} )</td>
</tr>
</tbody>
</table>

**BROWN-OUT PROTECTION AND FEED-FORWARD (Vsns is an internal pin that replaces Vsense)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{BOH} )</td>
<td>Brown-Out Threshold ( V_{main} ) increasing, ( V_{FB} ) based ([C**] and [D**] versions)</td>
</tr>
<tr>
<td>( V_{BOL} )</td>
<td>Brown-Out Threshold, ( V_{main} ) decreasing, avg(( V_{CS} )) based ([C**] and [D**] versions)</td>
</tr>
<tr>
<td>( V_{BO(HYST)} )</td>
<td>Brown-Out Comparator Hysteresis ([C**] and [D**] versions)</td>
</tr>
<tr>
<td>( t_{BO(blank)} )</td>
<td>Brown-Out Blanking Time ([C**] and [D**] versions)</td>
</tr>
<tr>
<td>( I_{VCTRL(BO)} )</td>
<td>VCTRL pin sink current during BO condition</td>
</tr>
<tr>
<td>( V_{HL} )</td>
<td>Comparator Threshold for Line Range Detection, avg(( V_{CS} )) rising</td>
</tr>
<tr>
<td>( V_{LL} )</td>
<td>Comparator Threshold for Line Range Detection, avg(( V_{CS} )) falling</td>
</tr>
<tr>
<td>( V_{HL(hyst)} )</td>
<td>Comparator Hysteresis for Line Range Detection</td>
</tr>
<tr>
<td>( t_{HL(blank)} )</td>
<td>Blanking Time for Line Range Detection</td>
</tr>
</tbody>
</table>

**THERMAL SHUTDOWN**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>( T_{LIMIT} )</td>
<td>Thermal Shutdown Threshold</td>
</tr>
<tr>
<td>( H_{TEMP} )</td>
<td>Thermal Shutdown Hysteresis</td>
</tr>
</tbody>
</table>

**SECOND OVERVOLTAGE PROTECTION (OVP2)**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{OVP2_HL} )</td>
<td>OVP2 Threshold, ( V_{CS} ) rising, ( K_{CS} = 138 ), @ ( V_{REF2} = 2.5 ) V</td>
</tr>
<tr>
<td>( V_{OVP2_LL} )</td>
<td>OVP2 Threshold, ( V_{CS} ) falling, ( K_{CS} = 138 ), @ ( V_{REF2} = 2.5 ) V</td>
</tr>
<tr>
<td>( V_{OVP2(HYST)_HL} )</td>
<td>OVP2 Comparator Hysteresis, ( K_{CS} = 138 ), @ ( V_{REF2} = 2.5 ) V</td>
</tr>
<tr>
<td>( V_{OVP2(LL)} )</td>
<td>OVP2 Threshold, ( V_{CS} ) rising, ( K_{CS} = 138 ), @ ( V_{REF2} = 1.6 ) V</td>
</tr>
<tr>
<td>( V_{OVP2(LL)} )</td>
<td>OVP2 Threshold, ( V_{CS} ) falling, ( K_{CS} = 138 ), @ ( V_{REF2} = 1.6 ) V</td>
</tr>
<tr>
<td>( V_{OVP2(HYST)_LL} )</td>
<td>OVP2 Comparator Hysteresis, ( K_{CS} = 138 ), @ ( V_{REF2} = 1.6 ) V</td>
</tr>
<tr>
<td>( I_{LEB,OVP2} )</td>
<td>OVP2 Leading Edge Blanking Time, ( V_{CS} ) rising (guaranteed by design)</td>
</tr>
<tr>
<td>( t_{RST(OVP2)} )</td>
<td>Reset Timer for OVP2 latch</td>
</tr>
</tbody>
</table>

3. The above specification gives the targeted values of the parameters. The final specification will be available once the complete circuit characterization has been performed.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
Figure 2. NCP1602 Block Diagram
NCP1602

TYPICAL CHARACTERISTICS

Figure 3. Start-Up Threshold, \( V_{CC} \) Increasing (\( V_{CC,\text{on}} \) vs. Junction Temperature (versions [**C] & [**D]))

Figure 4. Start-Up Threshold, \( V_{CC} \) Increasing (\( V_{CC,\text{on}} \) vs. Junction Temperature (versions [**A] & [**B]))

Figure 5. Minimum Operating Voltage, \( V_{CC} \) Falling (\( V_{CC,\text{off}} \) vs. Junction Temperature)

Figure 6. Hysteresis (\( V_{CC,\text{on}} \) – \( V_{CC,\text{off}} \) vs. Junction Temperature (versions [**C] & [**D]))

Figure 7. Hysteresis (\( V_{CC,\text{on}} \) – \( V_{CC,\text{off}} \) vs. Junction Temperature (versions [**A] & [**B]))

Figure 8. Dead-Time, \( V_{ctrl} = 0.65 \) V w/ E Config (\( t_{DT,E,1} \) vs. Junction Temperature)
TYPICAL CHARACTERISTICS

Figure 9. Dead-Time, $V_{\text{ctrl}} = 0.75\ V$ w/ E Config ($t_{\text{DT,E,2}}$) vs. Junction Temperature

Figure 10. $V_{\text{ctrl}}$ Threshold CrM to DCM Mode w/ E Config ($V_{\text{ctrl,th,E}}$) vs. Junction Temperature

Figure 11. $V_{\text{ctrl}}$ Pin SKIP Level, $V_{\text{ctrl}}$ Rising ($V_{\text{SKIP-H}}$) vs. Junction Temperature

Figure 12. $V_{\text{ctrl}}$ Pin SKIP Level, $V_{\text{ctrl}}$ Falling ($V_{\text{SKIP-L}}$) vs. Junction Temperature

Figure 13. DRV Pin Level for $V_{\text{CC}} = V_{\text{CC,off}} + 200\ mV$ (10–kΩ Resistor between DRV and GND) ($V_{\text{DRV,low}}$) vs. Junction Temperature

Figure 14. DRV Pin Level @ $V_{\text{CC}} = 30\ V$ ($R_L = 33\ k\Omega$ & $C_L = 1\ nF$) ($V_{\text{DRV,high}}$) vs. Junction Temperature
TYPICAL CHARACTERISTICS

Figure 15. Feedback Voltage Reference ($V_{REF}$) vs. Junction Temperature

Figure 16. Error Amplifier Current Capability, Sourcing ($I_{EA1}$) vs. Junction Temperature

Figure 17. Error Amplifier Current Capability, Sinking ($I_{EA2}$) vs. Junction Temperature

Figure 18. Error Amplifier Transconductance ($G_{EA}$) vs. Junction Temperature

Figure 19. Watch Dog Timer Duration ($t_{WDG}$) vs. Junction Temperature

Figure 20. Watch Dog Timer Duration in “OverStress” Situation ($t_{WDG(OS)}$) vs. Junction Temperature
TYPICAL CHARACTERISTICS

Figure 21. Maximum On Time, $\text{avg}(V_{CS}) = 0.9 \text{ V}$ & $V_{\text{ctrl}}$ Maximum (CrM) & Low Line for E Version ($t_{\text{on,LL,E}}$) vs. Junction Temperature

Figure 22. Maximum On Time, $\text{avg}(V_{CS}) = 2.8 \text{ V}$ & $V_{\text{ctrl}}$ Maximum (CrM) & High Line for E Version ($t_{\text{on,HL,E}}$) vs. Junction Temperature

Figure 23. UVP Threshold, $V_{\text{FB}}$ Increasing ($V_{\text{UVPH}}$) vs. Junction Temperature

Figure 24. UVP Threshold, $V_{\text{FB}}$ Decreasing ($V_{\text{UVPL}}$) vs. Junction Temperature

Figure 25. UVP Threshold Hysteresis ($V_{\text{UVPL(HYST)}}$) vs. Junction Temperature

Figure 26. Comparator Threshold for Line Range Detection, $\text{avg}(V_{CS})$ Rising, ($V_{\text{HL}}$) vs. Junction Temperature
TYPICAL CHARACTERISTICS

Figure 27. Comparator Threshold for Line Range Detection, avg(V_{CS}) Falling, (V_{LL}) vs. Junction Temperature

Figure 28. Comparator Hysteresis for Line Range Detection, (V_{HL(hyst)}) vs. Junction Temperature
NCP1602

Detailed Operating Description

Introduction
NCP1602 is designed to optimize the efficiency of your PFC stage throughout the load range. In addition, it incorporates protection features for rugged operation. More generally, NCP1602 is ideal in systems where cost-effectiveness, reliability, low stand-by power and high efficiency are key requirements:

- **Valley Synchronized Frequency Fold-back:** NCP1602 is designed to drive PFC boost stages in so-called Valley Synchronized Frequency Fold-back (VSFF). In this mode, the circuit classically operates in Critical conduction Mode (CrM) when Vctrl exceeds a programmable value. When the Vctrl is below this preset level, NCP1602 linearly reduces the frequency down to about 33 kHz before reaching the SKIP threshold voltage (SKIP Mode versions [B**] and [D**]). VSFF maximizes the efficiency at both nominal and light load. In particular, stand-by losses are reduced to a minimum. Similarly to FCCrM controllers, an internal circuitry allows near-unity power factor even when the switching frequency is reduced.

- **SKIP Mode (Versions [B**] and [D**]):** To further optimize the efficiency, the circuit skips cycles at low load current when Vctrl reaches the SKIP threshold voltage. This is to avoid circuit operation when the power transfer is particularly inefficient at the cost of current distortion. This SKIP function is not present on versions [A**] and [C**]).

- **Low Start-up Current** and large VCC range ([**A**] & [**B**] versions): The start-up consumption of the circuit is minimized to allow the use of high-impedance start-up resistors to pre-charge the VCC capacitor. Also, the minimum value of the UVLO hysteresis is 6 V to avoid the need for large VCC capacitors and help shorten the start-up time without the need for too dissipative start-up elements. The [**C**] & [**D**] version is preferred in applications where the circuit is fed by an external power source (from an auxiliary power supply or from a downstream converter). Its maximum start-up level (11.25 V) is set low enough so that the circuit can be powered from a 12–V rail. After start-up, the high VCC maximum rating allows a large operating range from 9.5 V up to 30 V.

- **Fast Line / Load Transient Compensation (Dynamic Response Enhancer):** Since PFC stages exhibit low loop bandwidth, abrupt changes in the load or input voltage (e.g. at start-up) may cause excessive over or under-shoot. This circuit limits possible deviations from the regulation level as follows:
  - NCP1602 linearly decays the power delivery to zero when the output voltage exceeds 105% of its desired level (soft OVP). If this soft OVP is too smooth and the output continues to rise, the circuit immediately interrupts the power delivery when the output voltage is 107% above its desired level.
  - NCP1602, dramatically speeds-up the regulation loop when the output voltage goes below 95.5% of its regulation level. This function is enabled only after the PFC stage has started-up to allow normal soft-start operation to occur.

- **Safety Protections:** Permanently monitoring the input and output voltages, the MOSFET current and the die temperature to protect the system from possible over-stress making the PFC stage extremely robust and reliable. In addition to the OVP protection, the following methods of protection are provided:
  - **Maximum Current Limit:** The circuit senses the MOSFET current and turns off the power switch if the set current limit is exceeded. In addition, the circuit enters a low duty-cycle operation mode when the current reaches 150% of the current limit as a result of the inductor saturation or a short of the bypass diode.
  - **Under-Voltage Protection:** This circuit turns off when it detects that the output voltage is below 12% of the voltage reference (typically). This feature protects the PFC stage if the ac line is too low or if there is a failure in the feedback network (e.g., bad connection).
  - **Brown-Out Detection:** The circuit detects low ac line conditions and stops operation thus protecting the PFC stage from excessive stress.
  - **Thermal Shutdown:** An internal thermal circuitry disables the gate drive when the junction temperature exceeds 150°C (typically). The circuit resumes operation once the temperature drops below approximately 100°C (50°C hysteresis).

- **Output Stage Totem Pole:** NCP1602 incorporates a ~0.5 A / +0.8 A gate driver to efficiently drive most TO220 or TO247 power MOSFETs.

NCP1602 Operation Modes
As mentioned, NCP1602 PFC controller implements a Valley Synchronized Frequency Fold-back (VSFF) where:

- The circuit operates in classical Critical conduction Mode (CrM) when Vctrl exceeds a programmable value Vctrl,th,*.

  - When Vctrl is below this Vctrl,th,* the NCP1602 linearly reduces the operating frequency down to about 33 kHz

  - When Vctrl reaches Vctrl minimum value or the Vctrl SKIP mode threshold, the system works in low frequency burst mode.

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Figure 29. Valley Switching Operation in CrM and DCM Modes

As illustrated in Figure 29, under high load conditions, the boost stage is operating in CrM but as the load is reduced, the controller enters controlled frequency discontinuous operation.

Valley Synchronized Frequency Foldback (VSFF) 

To further reduce the losses, the MOSFET turns on is stretched until its drain–source voltage is at its valley. The end of the dead time is synchronized with the drain–source ringing.

Valley Synchronized Frequency Foldback (VSFF) 
a/ Valley Synchronized (VS)

Valley Synchronized is the first half of the VSFF system.

Synchronizing the Turn–on with the drain voltage valley maximizes the efficiency at both nominal and light load conditions. In particular, the stand–by losses are reduced to a minimum. The synchronization of Power MOSFET Turn–on (rising edge of CLK signal) with drain voltage valley is depicted on Figure 30. This method avoids system stalls between valleys. Instead, the circuit acts so that the PFC controller transitions from the n valley to (n+1) valley or vice versa from the n valley to (n−1) cleanly as illustrated by the simulation results of Figure 31. When the Line voltage and inductor current are very low, or when the amplitude of the drain voltage gets too low (in the case of long dead times), the turn–on of the power MOSFET is no longer synchronized with the drain valley but will start exactly at the end of a programmed dead time looks to the ZCD TIMER block.

If no demagnetization is sensed the power MOSFET will be turned–on after a watchdog timing of 200–μs.
**b/ Frequency Foldback (FF)**

Frequency Foldback is the second half of the VSFF system. When $V_{\text{ctrl}}$ falls below an option–programmable $V_{\text{ctrl,th,}}$ threshold, the NCP1602 enters DCM and linearly reduces the operating frequency down to about 33 kHz by adding a dead–time after the end of inductor demagnetization. The end of the dead–time is synchronized with the valley in the drain voltage, hence the name Valley Synchronized (VS). The lower the $V_{\text{ctrl}}$ value, the longer the dead–time.

The Frequency Foldback (FF) system adjusts the on–time versus $t_{\text{DT}}$ (see Figure 32) and the output power in order to ensure that the instantaneous mains current is in phase with the mains instantaneous voltage (creating a PF=1).

**Figure 31. Clean Transition Without Hesitation Between Valleys**

**Figure 32. NCP1602 Clock, Dead Time and $t_{\text{ON}}$ Waveforms**
When the load is at its maximum (the maximum $V_{\text{ctrl}}$ value and inductor peak current limitation is not triggering), the controller runs in CrM mode and the frequency ($@ V_{\text{in}}=V_{\text{in,max}}$) has its minimum value. As we start decreasing the output power, the $V_{\text{ctrl}}$ voltage decreases, the switching frequency ($@ V_{\text{in}}=V_{\text{in,max}}$) increases and the controller stays in CrM mode until $V_{\text{ctrl}}$ reach a threshold voltage named $V_{\text{ctrl,th,}}$. From this point, continuing to reduce the output power makes the controller to continue increase the dead time ($T_{\text{DT}}$) after the end of demagnetization resulting in a DCM conduction mode and a switching frequency decrease (Frequency Foldback).

When the output power is reduced and we enter DCM mode, the switching frequency decreases down to a value given by the following equation, which is valid down to before entering SKIP mode. This minimum DCM frequency value is dominated by the dead time value, $t_{\text{ON}}$ plus $t_{\text{DEMAG}}$ being negligible versus $t_{\text{DT,max}}$ that has reached its maximum value.

$$\frac{F_{\text{SW, DCM, min}}}{f_{\text{Oldback}}} = \frac{1}{t_{\text{DT,max}} + t_{\text{ON}} + t_{\text{DEMAG}}} = \frac{1}{t_{\text{DT,max}}} \quad (\text{eq. 1})$$

In order to have, depending on customer application, a different limitation of the maximum switching frequency ($@ V_{\text{in}}=V_{\text{in,max}}$), as well as different $V_{\text{ctrl}}$ thresholds for CrM to DCM boundary, different product versions are made available (see Table 2).

**CrM–DCM and DCM–CrM Transition Hysteresis**

Hesitation of the system to transition between the modes CrM and DCM may have consequences on inductor current shape and distort the mains current, resulting in a bad PF value when the operating point is at the CrM–DCM boundary.

To avoid such undesired behavior, a 40–mV hysteresis is added on $V_{\text{ctrl}}$ threshold. The $V_{\text{ctrl}}$ threshold for transitioning from CrM to DCM mode is named $V_{\text{ctrl,th,}}$ (see Table 6) and the $V_{\text{ctrl}}$ threshold for transitioning from DCM to CrM mode is $V_{\text{ctrl,th,}} + 40 \text{ mV}$.

**NCP1602 Skip Mode (Active on Versions [B**] and [D**], Disabled on Versions [A**] and [C**])**

The circuit also skips cycles when $V_{\text{ctrl}}$ decreases towards $V_{\text{SKIP,L}}$ threshold. A comparator monitors the $V_{\text{ctrl}}$ voltage and inhibits the drive when $V_{\text{ctrl}}$ is lower than the SKIP Mode threshold $V_{\text{SKIP,L}}$. Switching resumes when $V_{\text{ctrl}}$ exceeds $V_{\text{SKIP,H}}$ threshold. The skip mode capability is disabled whenever the PFC stage is not in nominal operation (as dictated by the PFCOK signal – see PFCOK Operation section).

**NCP1602 On–time Modulation and $V_{\text{TON}}$ Processing Circuit**

Let’s analyze the ac line current absorbed by the PFC boost stage. The initial inductor current at the beginning of each switching cycle is always zero. The coil current ramps up when the MOSFET is on. The slope is $(V_{\text{in}}/L)$ where $L$ is the coil inductance. At the end of the on–time ($t_1$), the inductor starts to demagnetize. The inductor current ramps down until it reaches zero. The duration of this phase is ($t_2$). In some cases, the system enters then the dead–time ($t_3$) that lasts until the next clock is generated.

One can show that the ac line current is given by:

$$I_{\text{in}} = \frac{V_{\text{in}}}{2TL} \frac{t_1}{t_1 + t_2 + t_3} \quad (\text{eq. 2})$$

Where

$$T = t_1 + t_2 + t_3 \quad (\text{eq. 3})$$

is the switching period and $V_{\text{in}}$ is the ac line rectified voltage.

In light of this equation, we immediately note that $I_{\text{in}}$ is proportional to $V_{\text{in}}$ if $[t_1(t_1+t_2)/T]$ is a constant.

---

**Figure 33. PFC Boost Converter and Inductor Current in DCM**
The NCP1602 operates in voltage mode. As portrayed by Figure 33 & Figure 34, the MOSFET on-time $t_1$ is set by a dedicated circuitry monitoring $V_{ctrl}$ and dead-time $t_{DT}$ ensuring $[t_1 (t_1+t_2)/T]$ is constant and as a result making $I_{in}$ proportional to $V_{in}$ (PF=1)

On-time $t_1$ is also called $t_{on}$ and its maximum value $t_{on,max}$ is obtained when $V_{ctrl}$ is at maximum level. The internal circuitry makes $t_{on,max}$ at High Line condition (HLINE) to be 3 times the $t_{on,max}$ at Low Line condition (LLINE) (low-pass filtered internal CS-pin voltage is compared to $V_{HL}$ and $V_{LL}$ for deciding whether we are in HLINE or in LLINE). Two other values of $t_{on,max}$ are offered as options.

The input current is then proportional to the input voltage. Hence, the ac line current is properly shaped.

One can note that this analysis is also valid in the CrM case. This condition is just a particular case of this functioning where $(t_3=0)$, which leads to $(t_1+t_2=T)$ and $(V_{ton}=V_{regul})$. That is why the NCP1602 automatically adapts to the conditions and transitions from DCM and CrM (and vice versa) without power factor degradation and without discontinuity in the power delivery.

The swing of the error amplifier output is limited within an accurate range:
- It is forced above a voltage drop ($V_F$) by some circuitry.
- It is clamped not to exceed 4.0 V + the same $V_F$ voltage drop.

The $V_F$ value is 0.5 V typically.

The regulated output voltage $V_{out}$ uses a reference voltage that has two possible values based on mains voltage level.

For $LLINE = 0$ $V_{REF} = 2.5$ V and for $LLINE = 1$ $V_{REF} = V_{REF2} = 1.6$ V so the output voltage will have for example a 390 V value for Highline ($LLINE = 0$) and a 250 V value for Lowline ($LLINE = 1$).

This feature that can be named “two level boost follower” is not active by default but can be enabled by OTP programming.

Given the low bandwidth of the regulation loop, abrupt variations of the load, may result in excessive over or under-shoot. Over-shoot is limited by the Over-Voltage Protection connected to FB pin (Feedback).

NCP1602 embeds a “Dynamic Response Enhancer” circuitry (DRE) that contains under-shoots. An internal comparator monitors the FB pin voltage ($V_{FB}$) and when $V_{FB}$ is lower than 95.5% of its nominal value, it connects a 200–μA current source to speed-up the charge of the
compensation network. Effectively this appears as a 10x increase in the loop gain.

The circuit also detects overshoot and immediately reduces the power delivery when the output voltage exceeds 105% of its desired level.

The error amplifier OTA and the OVP, UVP and DRE comparators share the same input information. Based on the typical value of their parameters and if \( V_{\text{out,nom}} \) is the output voltage nominal value (e.g., 390 V), we can deduce:

- **Output Regulation Level**: \( V_{\text{out,nom}} \)
- **Output DRE Level**: \( V_{\text{out,dre}} = 95.5\% \times V_{\text{out,nom}} \)
- **Output Soft OVP Level**: \( V_{\text{out,sovp}} = 105\% \times V_{\text{out,nom}} \)
- **Output Fast OVP level**: \( V_{\text{out,fovp}} = 107\% \times V_{\text{out,nom}} \)

**Current Sense and Zero Current Detection**

NCP1602 is designed to monitor the current flowing through the power switch during On−time for detecting over current and overstress and to monitor the power MOSFET drain voltage during demagnetization time and dead time in order to generate the ZCD signal.

Current sense, zero current detection and Vin sense are using the CS/ZCD pin voltage as depicted in the electrical schematic of Figure 35.

**Current Sense**

The power MOSFET current \( I \) is sensed during the \( T_{\text{ON}} \) phase by the resistor \( R_{\text{sense}} \) inserted between the MOSFET source and ground (see Figure 36). During \( T_{\text{ON}} \) phase \( R_{cs1} \) and \( R_{cs2} \) are almost in parallel and the signal \( R_{\text{sense}}.I \) is equal to the voltage on pin CS.
Figure 36. Current Sensing during the $T_{ON}$ Phase
During the On−time and after a 200−ns blanking time, an OCP (Over Current Protection) signal is generated by an OCP comparator, comparing \( V_{CS} = V_{CS2} \) to a 500−mV internal reference.

When \( R_{senseds_{\text{max}}} = V_{CS} = V_{CS2} = 500 \text{ mV} \) we get:

\[
I_{ds_{\text{max}}} = \frac{V_{\text{ocp}}}{R_{\text{sense}}} \quad \text{(eq. 4)}
\]

When \( V_{CS} \) exceeds the 500−mV internal reference threshold, the OCP signal turns high to reset the PWM latch and forces the driver low. The 200−ns blanking time prevents the OCP comparator from tripping because of the switching spikes that occur when the MOSFET turns on.

**Zero Current Detection**

The CS pin is also designed to receive, during tDEMAg and tDT, a scaled down (divided by 138) power MOSFET drain voltage that will be used for Zero Current Detection. It may happen that the MOSFET turns on while a huge current flows through the inductor. As an example such a situation can occur at start−up when large in−rush currents charge the bulk capacitor to the line peak voltage. Traditionally, a bypass diode is generally placed between the input and output high−voltage rails to divert this inrush current. If this diode is accidently shorted, the demagnetization will be impossible and cycle after cycle the inductor current will increase so the MOSFET will also see a high current when it turns on. In both cases, the current can be large enough to trigger the OverStress (OVS) comparator. In this case, the “OverStress” signal goes high and disables the driver for an 800−μs delay. This long delay leads to a very low duty−ratio operation in case of “OverStress” fault in order to limit the risk of overheating.

When no signal is received that triggers the ZCD comparator to indicate the end of inductor demagnetization, an internal 200−μs watchdog timer initiates the next drive pulse. At the end of this delay, the circuit senses the CS/ZCD pin impedance to detect a possible grounding of this pin and prevent operation.

**Brown−Out Detection (Versions [C**] and [D**])**

For an application w/o Vaux (using the Drain) and using Brown−out options ([C**] and [D**]) the Brown−out feature will use the High and Low Brown−out levels.

Brown−out options ([C**] and [D**]) must not be used on an application using Vaux as these options are not designed to work in this case.

By default, the Brown−out flag is set High (BONOK=1), meaning that \( V_{in}, \text{sensed thru CSZCD pin and } V_{\text{sns}} (V_{\text{sns}} \text{ is a low−pass filtered scaled down } V_{\text{in}}) \text{ internal signal (see Figure 1), when higher than internal reference voltage } V_{\text{BOLh}} \text{ will set the brown−out flag to zero } (\text{BONOK}=0) \text{ and allow the controller to start. After BONOK is set to zero, and switching activity starts, the } V_{\text{in}} \text{ continues to be sensed thru CSZCD pin and when } V_{\text{sns}} \text{ falls under Brown−out internal reference voltage } V_{\text{BOL}} \text{ for 50 ms, BONOK flag will be set to 1. After BONOK flag will be set to 1, drive is not disabled, instead, a 30−μA current source is applied to VCTRL pin to gradually reduce } V_{\text{CTRL}}. \text{ As a result, the circuit only stops pulsing when the STATICOVP function is activated (that is when } V_{\text{CTRL}} \text{ reaches the SKIP detection threshold). At that moment, the circuit stops switching. This method limits any risk of false triggering.}

**For an application w/ Vaux (not using the Drain), Brown−out options ([C**] and [D**]) are not be allowed** and the UVP will act like a brown−in. The reason is that before controller starts switching, the \( V_{\text{out}} \) voltage is equal to \( V_{\text{mains, rms}} \) and sensed by FB pin and compared to UVP high internal reference voltage \( V_{\text{UVPH}} \).

The input of the PFC stage has some impedance that leads to some sag of the input voltage when the input current is large. If the PFC stage suddenly stops while a high current is drawn from the mains, the abrupt decay of the current may make the input voltage rise and the circuit detect a correct line level. Instead, the gradual decrease of \( V_{\text{control}} \) avoids a line current discontinuity and limits the risk of false triggering.

\( V_{\text{sns}} \) internal voltage is also used to sense the line for feed−forward. A similar method is used:

- The \( V_{\text{sns}} \) internal pin voltage is compared to a 1.801−V reference.
- If \( V_{\text{sns}} \) exceeds 1.801 V, the circuit detects a high−line condition and the loop gain is divided by three (the internal PWM ramp slope is three times steeper)
- Once this occurs, if \( V_{\text{sns}} \) remains below 1.392 V for 25 ms, the circuit detects a low−line situation (500−mV hysteresis).

At startup, the circuit is in High−line state (“LLINE” Low”) and then \( V_{\text{sns}} \) will be used to determine the High−Line or Low−Line state. The line range detection circuit allows more optimal loop gain control for universal (wide input mains) applications.
Two-Level Boost Follower Line Level Dependent

The Two-Level Boost Follower feature is disabled by default, but it is available on product versions [**B] & [**D].

When the feature is enabled, the controller will regulate its output voltage \( V_{\text{out}} \) to a value dependent on the sensed line level. The regulated output voltage \( V_{\text{out}} \) uses a reference voltage that has two possible values based on mains voltage. For \( \text{LLINE} = 0 \) \( V_{\text{REF}} = 2.5 \text{ V} \) and for \( \text{LLINE} = 1 \) \( V_{\text{REF}} = 1.6 \text{ V} \) so the output voltage will have for example a 390 V value for Highline (LLINE = 0) and a 250 V value for Lowline (LLINE = 1).

In order for the Two-Level Boost Follower Line Level Dependent feature to work OK with the the Brown-in feature at startup, the controller will always start with \( V_{\text{REF}} = 2.5 \text{ V} \) and then, once Brown-in validated and switching started, the sensed line level will determine the \( V_{\text{REF}} \) value to be used and hence the \( V_{\text{out}} \) value.

Thermal Shut-Down (TSD)

An internal thermal circuitry disables the circuit gate drive and keeps the power switch off when the junction temperature exceeds 150\(^\circ\)C. The output stage is then enabled once the temperature drops below about 100\(^\circ\)C (50\(^\circ\)C hysteresis).

The temperature shutdown remains active as long as the circuit is not reset, that is, as long as \( V_{\text{CC}} \) is higher than a reset threshold.

Output Drive Section

The output stage contains a totem pole optimized to minimize the cross conduction current during high frequency operation. Its high current capability (~500 mA / +800 mA) allows it to effectively drive high gate charge power MOSFET.

Second Over-Voltage Protection

On top of the existing overvoltage protection, a second and redundant overvoltage protection named OVP2 has been added. This overvoltage protection, senses, during \( t_{\text{DEMAG}} \) the value of \( V_{\text{out}} \), thru the \( R_{\text{CS1}}, R_{\text{CS2}} \) divider bridge connected to the pin \( \text{CS} \) and compares it to an OVP2 voltage reference \( V_{\text{REF, OVP2}} \). Because it is not possible to adjust the \( V_{\text{REF, OVP2}} \) reference to \( R_{\text{fb1}} \& R_{\text{fb2}} \) that programs the \( V_{\text{out}} \) value, it has been decided to set \( V_{\text{REF, OVP2}} \) and \( R_{\text{CS1}}, R_{\text{CS2}} \) in order to get OVP2 triggering for \( V_{\text{out}} \) voltages much higher than for OVP condition (e.g. OVP2 goes high when \( V_{\text{out}} \) goes higher than 438 V).

For \( V_{\text{out}} = 438 \text{ V} \) for OVP2 and given a \( K_{\text{CS}} \) value equal to 1/138 \( (K_{\text{CS}} = R_{\text{CS2}} / (R_{\text{CS1}} + R_{\text{CS2}}) \), this gives \( V_{\text{REF, OVP2}} = 3.175 \text{ V} \) for the threshold voltage to which is compared the \( V_{\text{CS}} \) voltage during \( t_{\text{off}} \). When \( V_{\text{CS}} \) goes above \( V_{\text{REF, OVP2}} \) threshold of the OVP2 comparator (100 mV hysteresis), and after a 1−\( /C_0109 \)s leading edge blanking time, the OVP2 flag is latched and will stop the switching by resetting the main PWM latch. The OVP2 latch is reset each \( 800 /C_0109 \)s.

Two-level Boost Follower

In order to minimize the voltage between \( V_{\text{in}} \) and \( V_{\text{out}} \) for avoiding the degradation of power efficiency, the internal voltage references can be managed versus the line voltage level condition (LLINE = 0 for High Line or LLINE = 1 for Low Line).

If the “Two-level Boost Follower” feature is activated (by default it is not activated), this will result in a regulated \( V_{\text{out}} \) voltage for Low Line condition being 0.64 times the regulated \( V_{\text{out}} \) voltage for High Line condition.

OFF Mode

As previously mentioned, the circuit turns off when one of the following faults is detected:

- Incorrect feeding of the circuit (“UVLO” high when \( V_{\text{CC}} < V_{\text{CC}(\text{off})} \) and \( V_{\text{CC}(\text{off})} \) equating 9 V typically).
- Excessive die temperature detected by the thermal shutdown
- Under-Voltage Protection
- Brown-Out Fault and STATICOVP (see Figure 2)
Generally speaking, the circuit turns off when the conditions are not proper for desired operation. In this mode, the controller stops operating. The major part of the circuit sleeps and its consumption is minimized.

More specifically, when the circuit is in OFF state:
- The drive output is kept low
- All the blocks are off except:
  - The UVLO circuitry that keeps monitoring the $V_{CC}$ voltage and controlling the start-up current source accordingly.
  - The TSD (thermal shutdown)
  - The Under-Voltage Protection (“UVP”)
  - The brown-out circuitry
- $V_{ctrl}$ is grounded so that when the fault is removed, the device starts-up under the soft start mode (version XB).
- The internal “PFCOK” signal is grounded.
- The output of the “$V_{ton}$ processing block” is grounded

**Failure Detection**

When manufacturing a power supply, elements can be accidentally shorted or improperly soldered. Such failures can also happen later on because of the components fatigue or excessive stress, soldering defaults or external interactions. In particular, adjacent pins of controllers can be shorted; a pin can be grounded or badly connected. Such open/short situations are generally required not to cause fire, smoke nor big noise. NCP1602 integrate functions that ease meet this requirement. Among them, we can list:

- **Floating feedback pin**
  A special internal circuitry detects the floating feedback pin and stops the operation of the IC.

- **Fault of the GND connection**
  If the GND pin is not connected, internal circuitry detects it and if such a fault is detected for 200 $\mu$s, the circuit stops operating.

- **Detection the CS/ZCD pin improper connection**
  If the CS/ZCD pin is floating or shorted to GND it is detected by internal circuitry and the circuit stops operating.

- **Boost or bypass diode short**
  The controller addresses the short situations of the boost and bypass diodes (a bypass diode is generally placed between the input and output high-voltage rails to divert this inrush current). Practically, the overstress protection is implemented to detect such conditions and forces a low duty-cycle operation until the fault is gone.

Refer to application note ANDxxxx for more details.
NCP1602

PACKAGE DIMENSIONS

TSOP−6
CASE 318G−02
ISSUE V

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOLDERING FOOTPRINT*

STYLE 13:
PIN 1. GATE 1
2. SOURCE 2
3. GATE 2
4. DRAIN 2
5. SOURCE 1
6. DRAIN 1

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 PER SIDE. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM
MIN
NOM
MAX

A
0.90
1.00
1.10

A1
0.01
0.06
0.10

B
0.25
0.38
0.50

e
0.10
0.18
0.26

D
2.90
3.00
3.10

E
2.50
2.75
3.00

E1
1.30
1.50
1.70

e
0.85
0.95
1.05

L
0.20
0.40
0.60

L2
0.25 BSC

M
–
–
10c

PITCH

D
2.90
3.00
3.10

E
2.50
2.75
3.00

E1
1.30
1.50
1.70


e
0.85
0.95
1.05

L
0.20
0.40
0.60

L2
0.25 BSC

M
–
–
10c

PITCH

NOTES:
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
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5. PIN ONE INDICATOR MUST BE LOCATED IN THE INDICATED ZONE.

DIM
MIN
NOM
MAX

A
0.90
1.00
1.10

A1
0.01
0.06
0.10

B
0.25
0.38
0.50

e
0.10
0.18
0.26

D
2.90
3.00
3.10

E
2.50
2.75
3.00

E1
1.30
1.50
1.70

e
0.85
0.95
1.05

L
0.20
0.40
0.60

L2
0.25 BSC

M
–
–
10c

PITCH

D
2.90
3.00
3.10

E
2.50
2.75
3.00

E1
1.30
1.50
1.70


e
0.85
0.95
1.05

L
0.20
0.40
0.60

L2
0.25 BSC

M
–
–
10c

PITCH

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