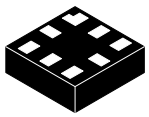
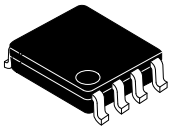
TinyLogic UHS Dual 2-Input Exclusive-OR Gate

NC7WZ86

MARKING DIAGRAMS



UQFN8
1.6X1.6, 0.5P
CASE 523AY



US8
CASE 846AN

N7, WZ86	= Specific Device Code
KK	= 2−Digit Lot Run Traceability Code
XY	= 2−Digit Date Code Format
Z	= Assembly Plant Code
A	= Assembly Site
L	= Wafer Lot Number
YW	= Assembly Start Week

ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

Description

The NC7WZ86 is a dual 2−Input Exclusive−OR Gate from **onsemi**'s Ultra High Speed Series of TinyLogic. The device is fabricated with advanced CMOS technology to achieve ultra high speed with high output drive while maintaining low static power dissipation over a very broad V_{CC} operating range. The device is specified to operate over the 1.65 V to 5.5 V V_{CC} range. The inputs and output are high impedance when V_{CC} is 0 V. Inputs tolerate voltages up to 5.5 V independent of V_{CC} operating voltage.

Features

- Space Saving US8 Surface Mount Package
- MicroPak™ Pb−Free Leadless Package
- Ultra High Speed: t_{PD} 2.9 ns Typ. into 50 pF at 5 V V_{CC}
- High Output Drive: ±24 mA at 3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Matches the Performance of LCX when Operated at 3.3 V V_{CC}
- Power Down High Impedance Inputs / Output
- Overvoltage Tolerant Inputs Facilitate 5 V to 3 V Translation
- Patented Noise / EMI Reduction Circuitry Implemented
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

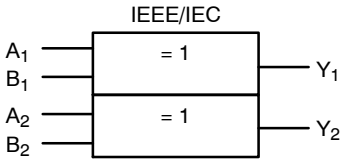


Figure 1. Logic Symbol

Connection Diagrams

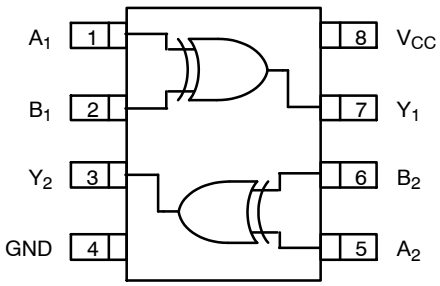


Figure 2. Connection Diagram (Top View)

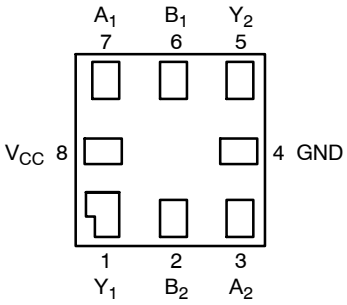
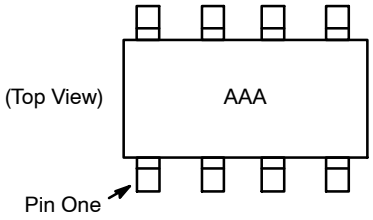


Figure 4. Pad Assignments for MicroPak (Top Thru View)



AAA represents Product Code Top Mark – see ordering code

NOTE: Orientation of Top Mark determines Pin One location. Read the top product code mark left to right, Pin One is the lower left pin (see diagram).

Figure 3. Pin One Orientation Diagram

PIN DESCRIPTIONS

Pin Names	Description
A_n, B_n	Input
Y_n	Output

FUNCTION TABLE ($Y = A \oplus B$)

Inputs		Output
A	**B**	**Y**
L	L	L
L	H	H
H	L	H
H	H	L

H = HIGH Logic Level
L = LOW Logic Level

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.5	V
V_{IN}	DC Input Voltage		−0.5	6.5	V
V_{OUT}	DC Output Voltage		−0.5	6.5	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V	−	−50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V	−	−50	mA
I_{OUT}	DC Output Current		−	±50	mA
I_{CC} / I_{GND}	DC V_{CC} / GND Current		−	±100	mA
T_{STG}	Storage Temperature		−65	+150	°C
T_J	Junction Temperature under Bias		−	150	°C
T_L	Junction Lead Temperature (Soldering, 10 Seconds)		−	260	°C
P_D	Power Dissipation in Still Air	US8 MicroPak−8	− −	500 539	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage Operating		1.65	5.5	V
	Supply Voltage Data Retention		1.5	5.5	
V_{IN}	Input Voltage		0	5.5	V
V_{OUT}	Output Voltage		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 1.8 V ±0.15 V, 2.5 V ±0.2 V	0	20	ns/V
		V_{CC} = 3.3 V ±0.3 V	0	10	
		V_{CC} = 5.0 V ±0.5 V	0	5	
θ_{JA}	Thermal Resistance	US8 MicroPak−8	− −	250 232	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTICAL CHARACTERISTICS

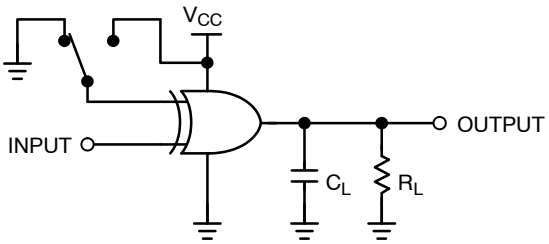
Symbol	Parameter	Conditions		V_{CC} (V)	T_A = +25°C			T_A = −40 to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage			1.65 to 1.95	0.65 V_{CC}	–	–	0.65 V_{CC}	–	V
				2.3 to 5.5	0.7 V_{CC}	–	–	0.7 V_{CC}	–	
V_{IL}	LOW Level Input Voltage			1.65 to 1.95	–	–	0.35 V_{CC}	–	0.35 V_{CC}	V
				2.3 to 5.5	–	–	0.3 V_{CC}	–	0.3 V_{CC}	
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH}, V_{IL}	I_{OH} = −100 μA	1.65	1.55	1.65	–	1.55	–	V
				2.3	2.2	2.3	–	2.2	–	
				3.0	2.9	3.0	–	2.9	–	
				4.5	4.4	4.5	–	4.4	–	
			I_{OH} = −4 mA	1.65	1.29	1.52	–	1.29	–	
			I_{OH} = −8 mA	2.3	1.9	2.15	–	1.9	–	
			I_{OH} = −16 mA	3.0	2.4	2.80	–	2.4	–	
			I_{OH} = −24 mA	3.0	2.3	2.68	–	2.3	–	
			I_{OH} = −32 mA	4.5	3.8	4.20	–	3.8	–	
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 100 μA	1.65	–	0.0	0.1	–	0.1	V
				2.3	–	0.0	0.1	–	0.1	
				3.0	–	0.0	0.1	–	0.1	
				4.5	–	0.0	0.1	–	0.1	
			I_{OL} = 4 mA	1.65	–	0.08	0.24	–	0.24	
			I_{OL} = 8 mA	2.3	–	0.10	0.3	–	0.3	
			I_{OL} = 16 mA	3.0	–	0.15	0.4	–	0.4	
			I_{OL} = 24 mA	3.0	–	0.22	0.55	–	0.55	
			I_{OL} = 32 mA	4.5	–	0.22	0.55	–	0.55	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V, GND		1.65 to 5.5	–	–	±0.1	–	±1	μA
I_{OFF}	Power Off Leakage Current	V_{IN} or V_{OUT} = 5.5 V		0.0	–	–	1	–	10	μA
I_{CC}	Quiescent Supply Current	V_{IN} = 5.5 V, GND		1.65 to 5.5	–	–	1	–	10	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = +25°C			T_A = −40 to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay (Figure 5, 7)	C_L = 15 pF, R_L = 1 MΩ	1.8 ±0.15	–	6.7	12.5	–	13.0	ns
			2.5 ±0.2	–	4.1	7.0	–	7.5	
			3.3 ±0.3	–	3.0	4.8	–	5.2	
			5.0 ±0.5	–	2.2	3.5	–	3.8	
		C_L = 50 pF, R_L = 500 Ω	3.3 ±0.3	–	3.8	5.4	–	5.9	
			5.0 ±0.5	–	2.9	4.2	–	4.6	
C_{IN}	Input Capacitance		0	–	2.5	–	–	–	pF
C_{PD}	Power Dissipation Capacitance (Figure 6)	(Note 2)	3.3	–	15	–	–	–	pF
			5.0	–	19	–	–	–	

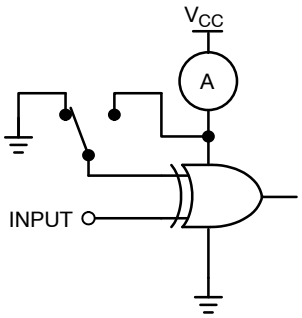
2. C_{PD} is defined as the value of the internal equivalent capacitance which is derived from dynamic operating current consumption (I_{CCD}) at no output loading and operating at 50% duty cycle. (see Figure 6) C_{PD} is related to I_{CCD} dynamic operating current by the expression: $I_{CCD} = (C_{PD})\ (V_{CC})\ (f_{IN}) + (I_{CC}static)$.

AC Loading and Waveforms



C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_W = 500 ns

Figure 5. AC Test Circuit



Input = AC Waveform;t_r = t_f = 1.8 ns;
PRR = 10 MHz; Duty Cycle = 50%

Figure 6. I_{CCD} Test Circuit

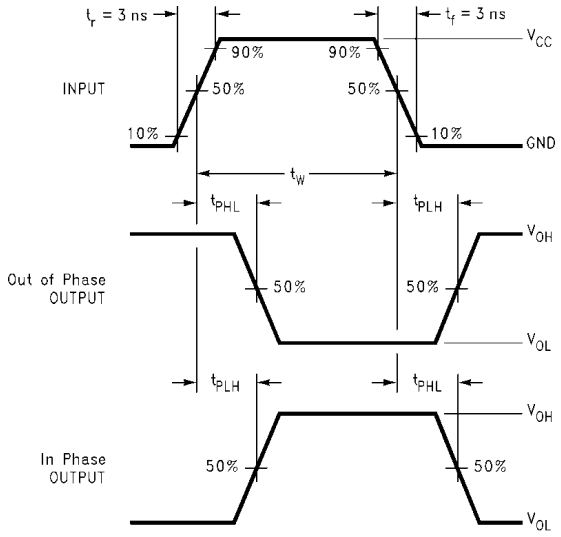


Figure 7. AC Waveforms

ORDERING INFORMATION

Order Number	Top Mark	Package	Shipping†
NC7WZ86K8X	WZ86	8−Lead US8, JEDEC MO−187, Variation CA 3.1 mm Wide	3000 / Tape & Reel
NC7WZ86L8X	N7	8−Lead MicroPak, 1.6 mm Wide (Pb−Free)	5000 / Tape & Reel

DISCONTINUED (Note 4)

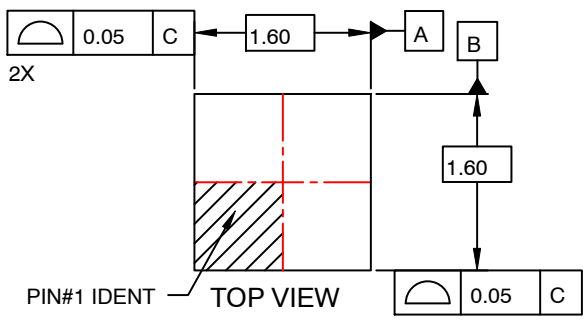
NC7WZ86L8X−L22185	N7	8−Lead MicroPak, 1.6 mm Wide (Pb−Free)	5000 / Tape & Reel

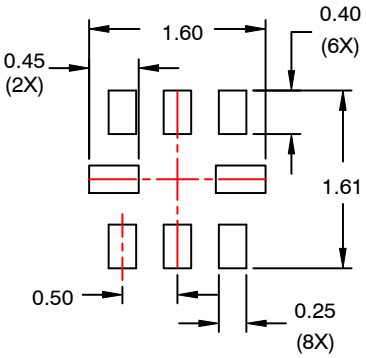
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

3. Pb−Free package per JEDEC J−STD−020B.
4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

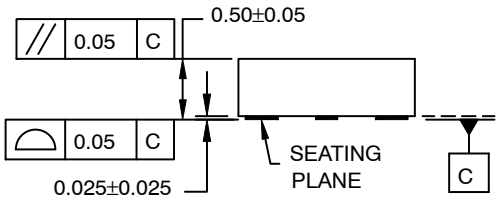
UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

DATE 31 AUG 2016





RECOMMENDED
LAND PATTERN



SIDE VIEW

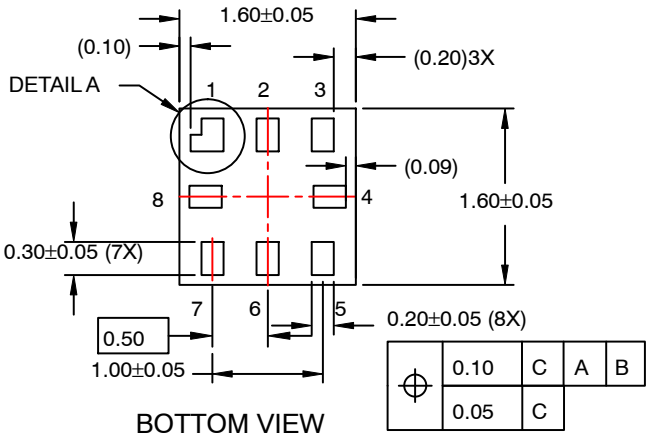
NOTES:

A. PACKAGE CONFORMS TO JEDEC MO−255 VARIATION UAAD.

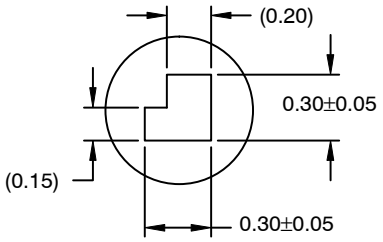
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW



DETAIL A
SCALE : 2X

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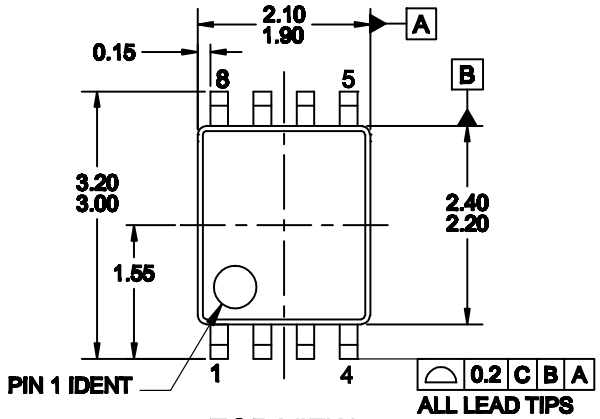
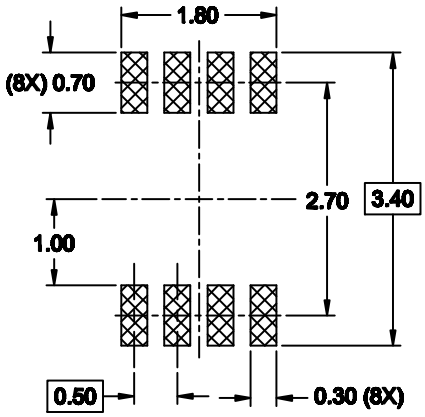
DESCRIPTION:	**UQFN8 1.6X1.6, 0.5P**	**PAGE 1 OF 1**

US8
CASE 846AN
ISSUE O

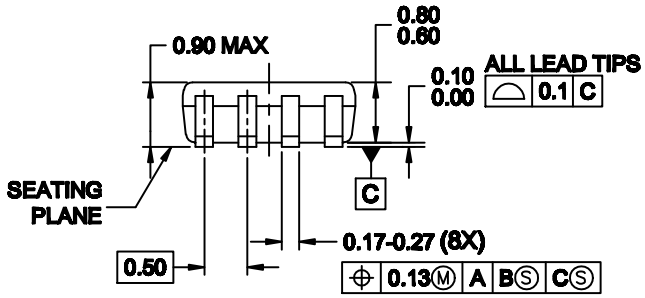
DATE 31 DEC 2016



TOP VIEW



RECOMMENDED LAND PATTERN



SIDE VIEW

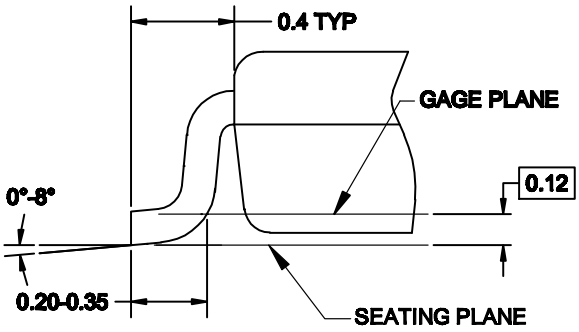
NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-187

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1994.



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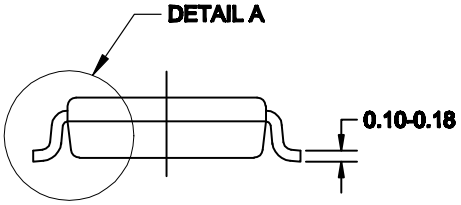

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