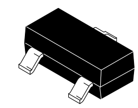
Amplifier Transistor

NPN Silicon

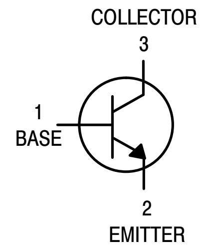
MMBT6521LT1G, SMMBT6521LT1G



SOT-23 (TO-236)
CASE 318
STYLE 6

Features

- S Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	V_{CEO}	25	Vdc
Collector-Base Voltage	V_{CBO}	40	Vdc
Emitter-Base Voltage	V_{EBO}	4.0	Vdc
Collector Current − Continuous	I_C	100	mAdc

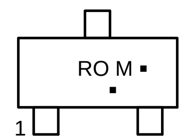
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation FR-5 Board (Note 1) @ T_A = 25 °C Derate above 25 °C	P_D	225 1.8	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	556	°C/W
Total Device Dissipation Alumina Substrate, (Note 2) @ T_A = 25 °C Derate above 25 °C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	417	°C/W
Junction and Storage Temperature	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 × 0.75 × 0.062 in.
2. Alumina = 0.4 × 0.3 × 0.024 in. 99.5% alumina.

MARKING DIAGRAM



RO = Specific Device Code
M = Date Code*
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.

ORDERING INFORMATION

Device	Package	Shipping[†]
MMBT6521LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel
SMMBT6521LT1G	SOT-23 (Pb-Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25 °C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector-Emitter Breakdown Voltage (I_C = 0.5 mAdc, I_B = 0)	$V_{(BR)CEO}$	25	–	Vdc
Emitter-Base Breakdown Voltage (I_E = 10 μAdc, I_C = 0)	$V_{(BR)EBO}$	4.0	–	Vdc
Collector Cutoff Current (V_{CB} = 30 Vdc, I_E = 0)	I_{CBO}	–	0.5	μAdc
Emitter Cutoff Current (V_{EB} = 5.0 Vdc, I_C = 0)	I_{EBO}	–	10	nAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 100 μAdc, V_{CE} = 10 Vdc) (I_C = 2.0 mAdc, V_{CE} = 10 Vdc)	h_{FE}	 150 300	 – 600	–
Collector-Emitter Saturation Voltage (I_C = 50 mAdc, I_B = 5.0 mAdc)	$V_{CE(sat)}$	–	0.5	Vdc
SMALL-SIGNAL CHARACTERISTICS				
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 1.0 MHz)	C_{obo}	–	3.5	pF
Noise Figure (I_C = 10 μAdc, V_{CE} = 5.0 Vdc, Power Bandwidth = 15.7 kHz, 3.0 dB points @ = 10 Hz and 10 kHz)	NF	–	3.0	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

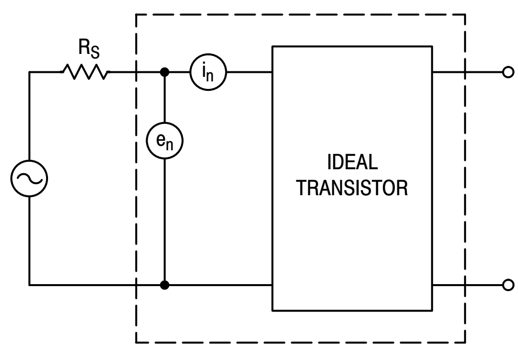
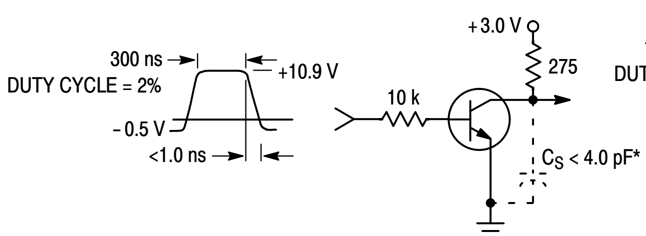
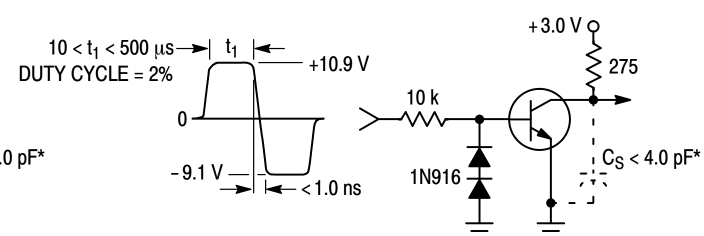


Figure 1. Transistor Noise Model

EQUIVALENT SWITCHING TIME TEST CIRCUITS





*Total shunt capacitance of test jig and connectors

Figure 2. Turn-On Time

Figure 3. Turn-Off Time

TYPICAL NOISE CHARACTERISTICS

(V_{CE} = 5.0 VDC, T_A = 25 °C)

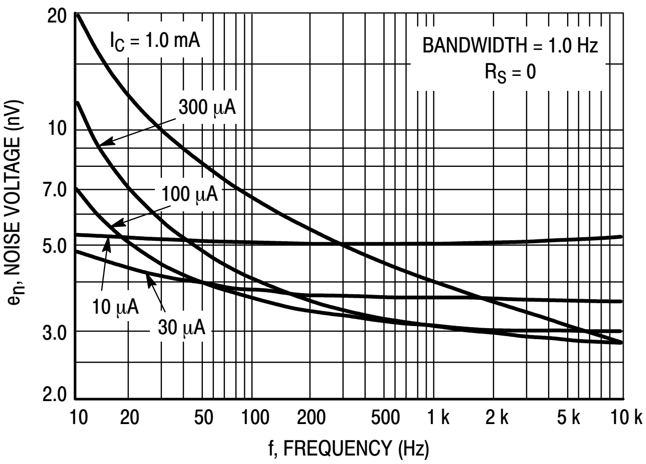


Figure 4. Noise Voltage

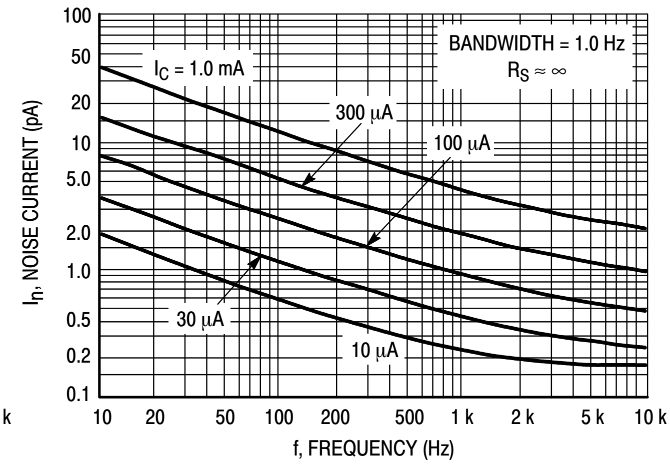


Figure 5. Noise Current

NOISE FIGURE CONTOURS

(V_{CE} = 5.0 VDC, T_A = 25 °C)

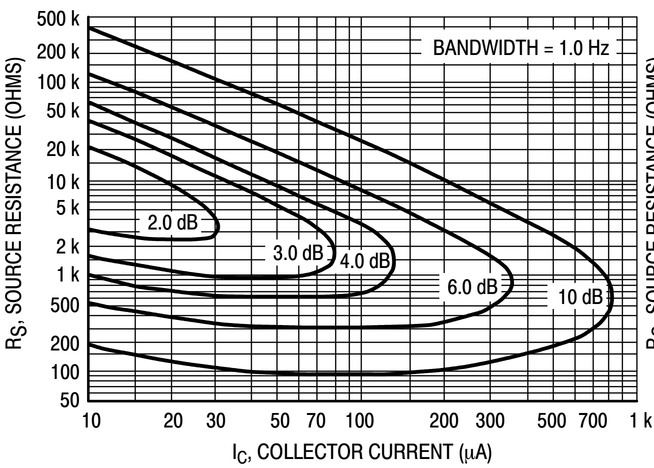


Figure 6. Narrow Band, 100 Hz

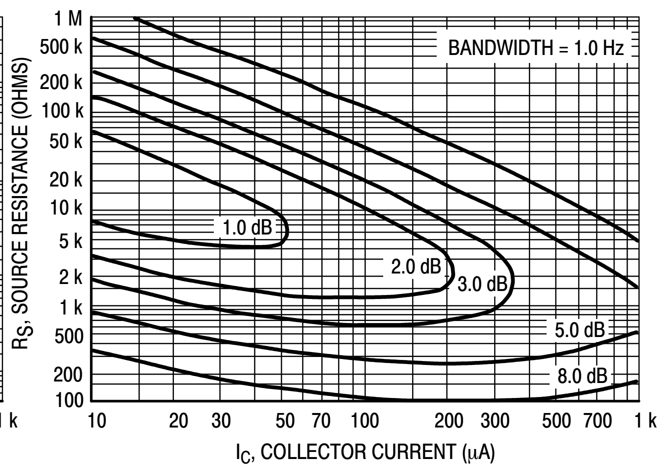


Figure 7. Narrow Band, 1.0 kHz

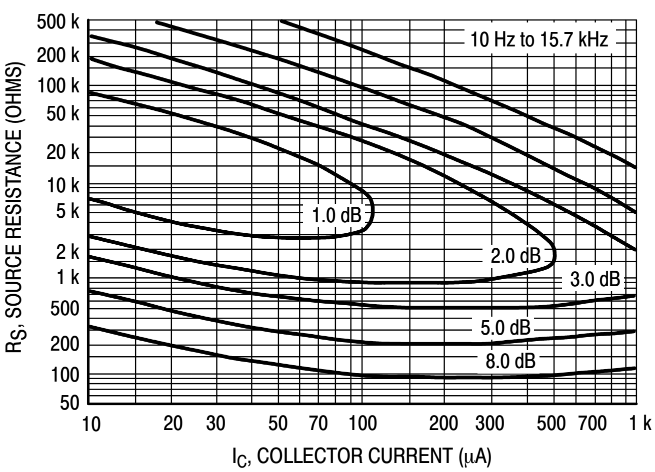


Figure 8. Wideband

Noise Figure is defined as:

$$NF = 20 \log_{10} \left(\frac{e_n^2 + 4KTR_S + I_n{}^2 R_S{}^2}{4KTR_S} \right)^{1/2}$$

e_n = Noise Voltage of the Transistor referred to the input. (Figure 3)
I_n = Noise Current of the Transistor referred to the input. (Figure 4)
K = Boltzman's Constant (1.38 x 10^{-23} j/°K)
T = Temperature of the Source Resistance (°K)
R_S = Source Resistance (Ohms)

TYPICAL STATIC CHARACTERISTICS

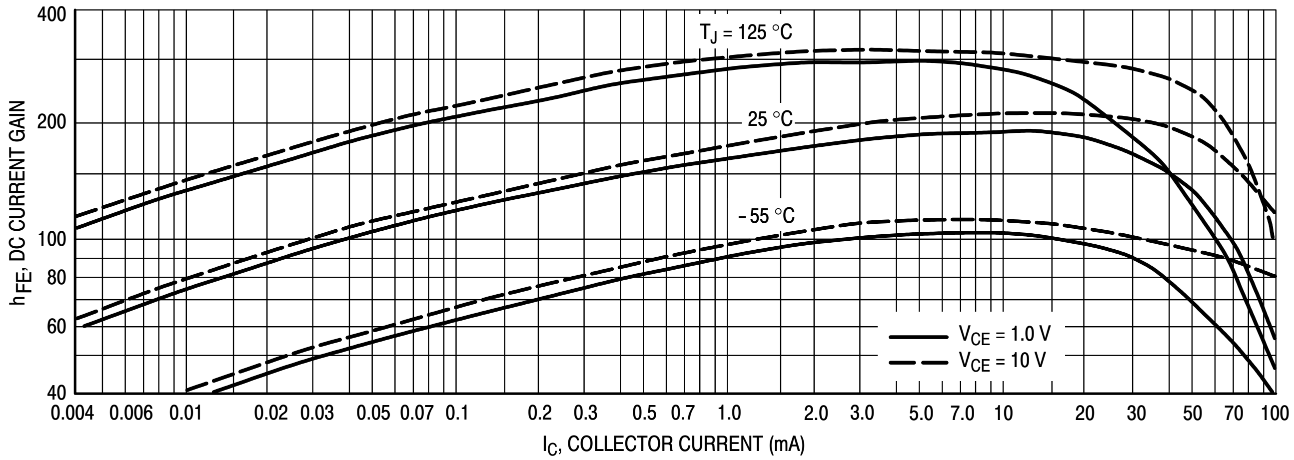


Figure 9. DC Current Gain

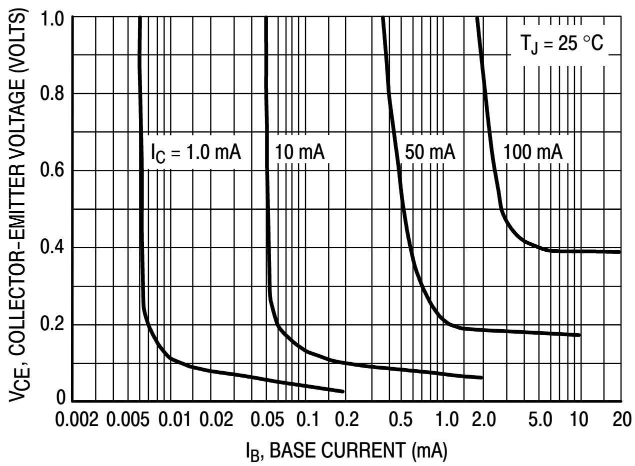


Figure 10. Collector Saturation Region

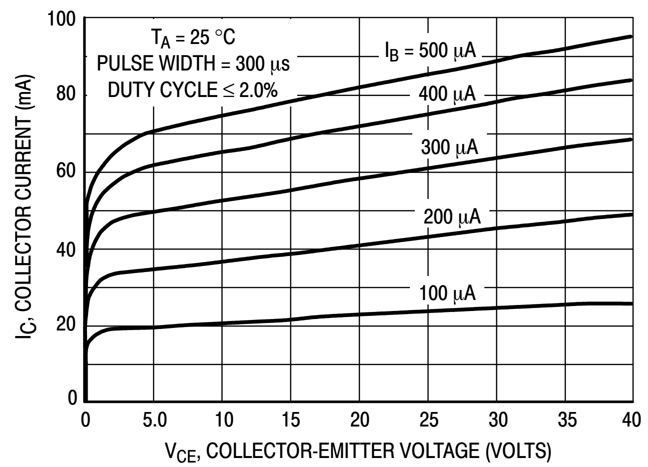


Figure 11. Collector Characteristics

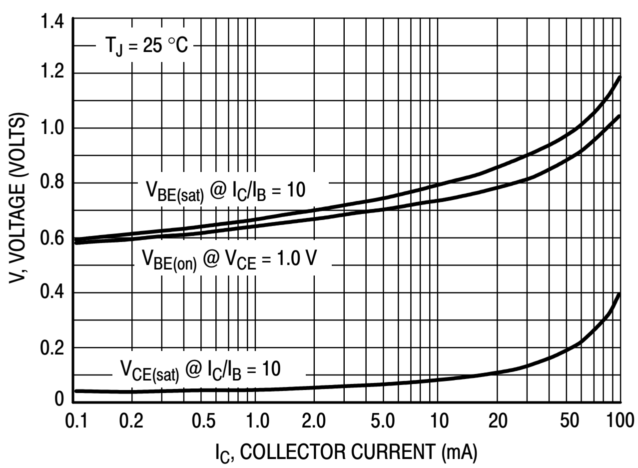


Figure 12. "On" Voltages

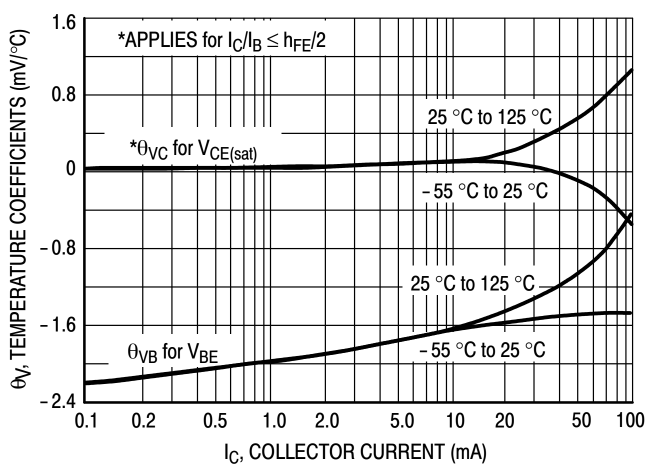


Figure 13. Temperature Coefficients

TYPICAL DYNAMIC CHARACTERISTICS

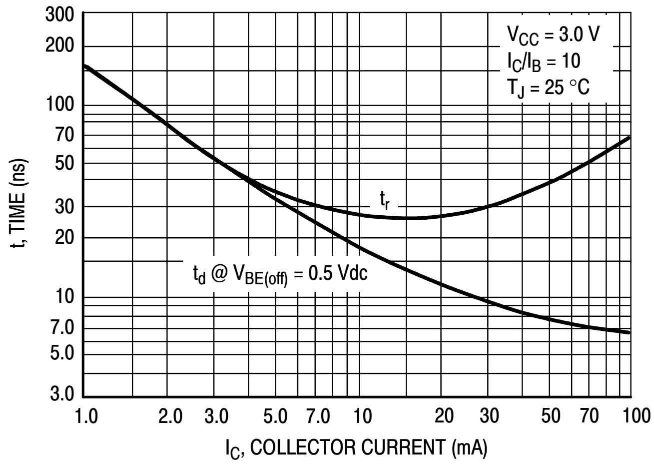


Figure 14. Turn-On Time

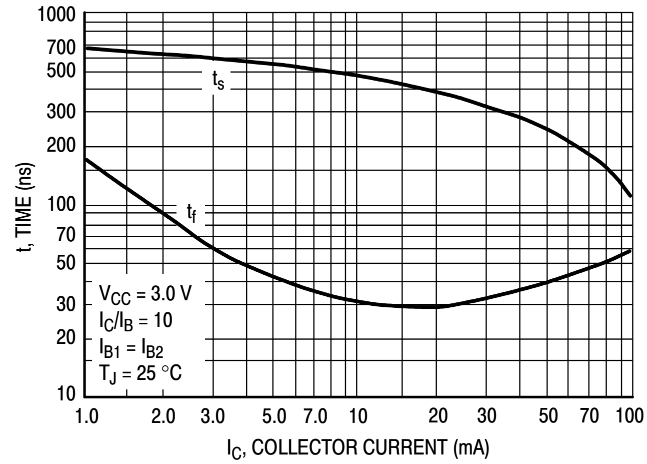


Figure 15. Turn-Off Time

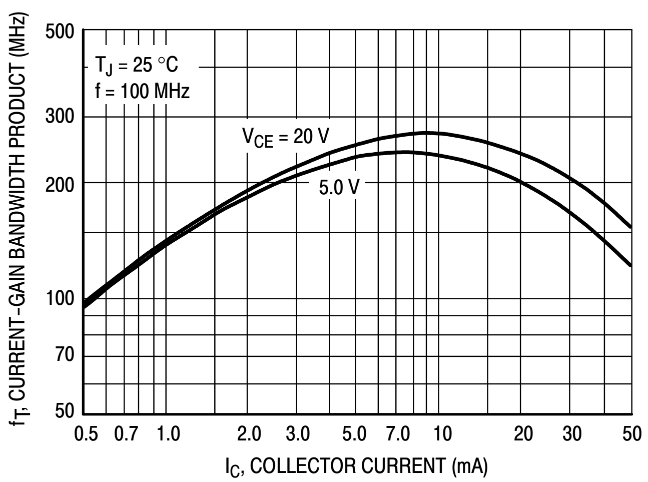


Figure 16. Current-Gain − Bandwidth Product

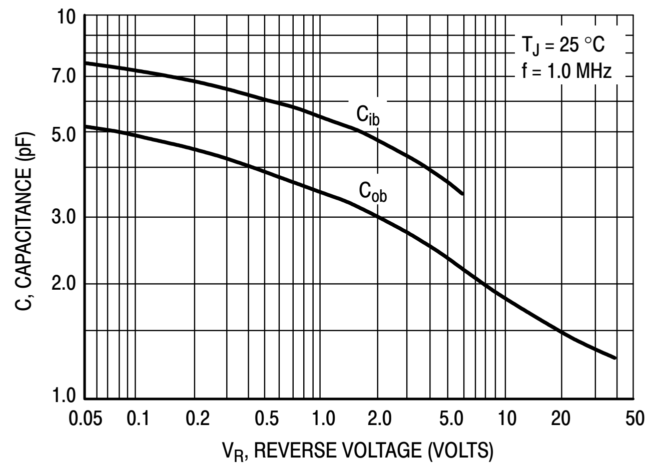


Figure 17. Capacitance

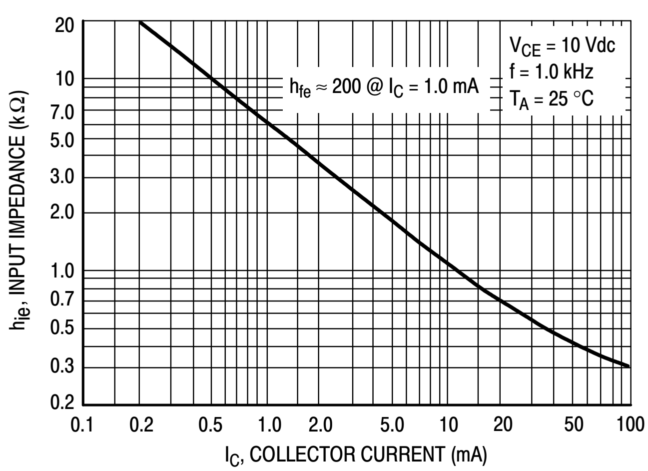


Figure 18. Input Impedance

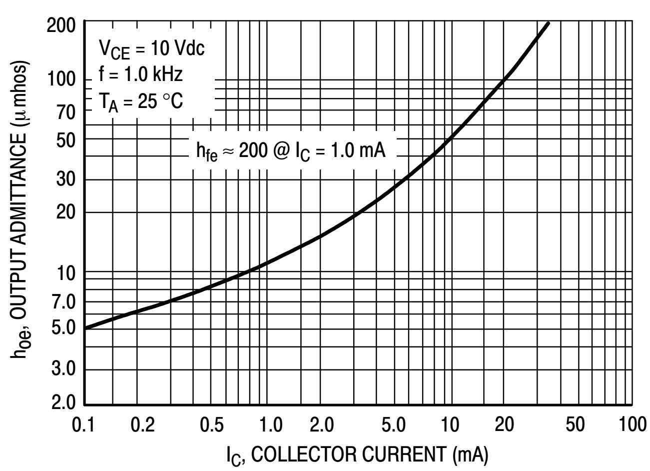


Figure 19. Output Admittance

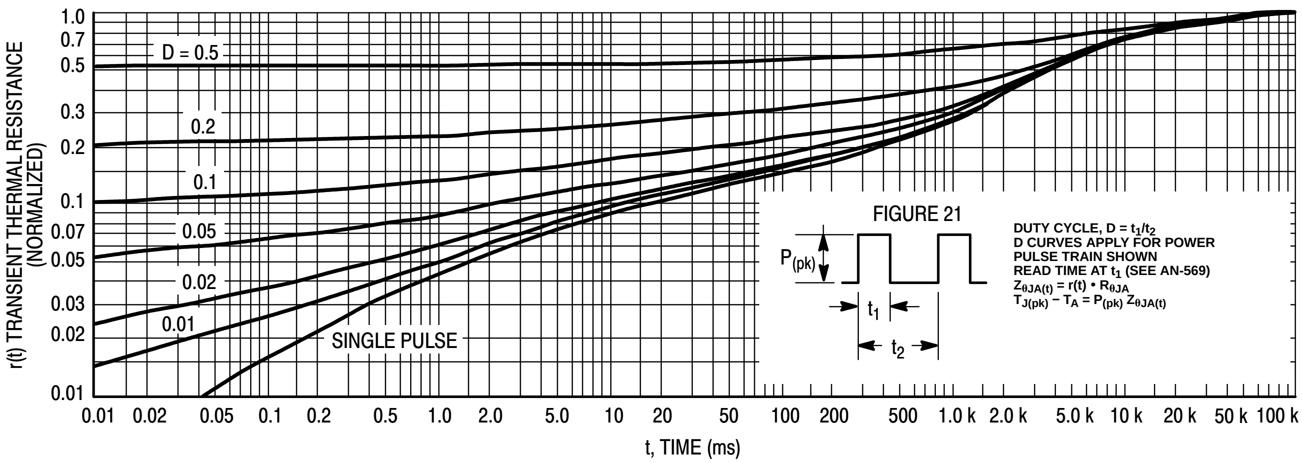


Figure 20. Thermal Response

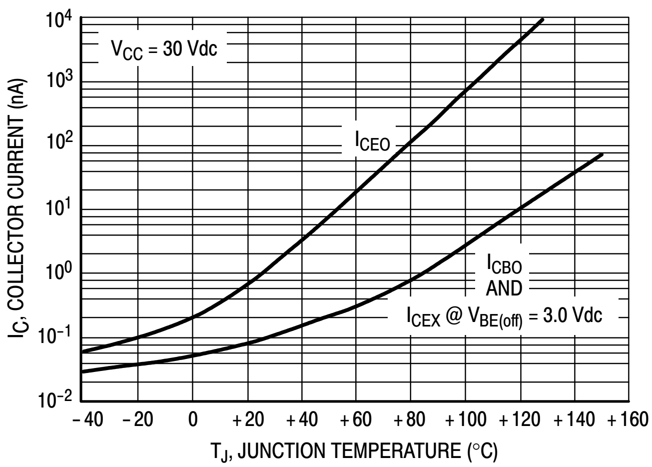


Figure 21.

DESIGN NOTE: USE OF THERMAL RESPONSE DATA

A train of periodical power pulses can be represented by the model as shown in Figure 21. Using the model and the device thermal response the normalized effective transient thermal resistance of Figure 20 was calculated for various duty cycles.

To find $Z_{\theta JA(t)}$, multiply the value obtained from Figure 20 by the steady state value $R_{\theta JA}$.

Example:

The MPS6521 is dissipating 2.0 watts peak under the following conditions:

t_1 = 1.0 ms, t_2 = 5.0 ms. (D = 0.2)

Using Figure 20 at a pulse width of 1.0 ms and D = 0.2, the reading of r(t) is 0.22.

The peak rise in junction temperature is therefore

$\Delta T = r(t) \times P_{(pk)} \times R_{\theta JA} = 0.22 \times 2.0 \times 200 = 88$ °C.

For more information, see **onsemi** Application Note AN569/D, available from the Literature Distribution Center or on our website at **www.onsemi.com**.

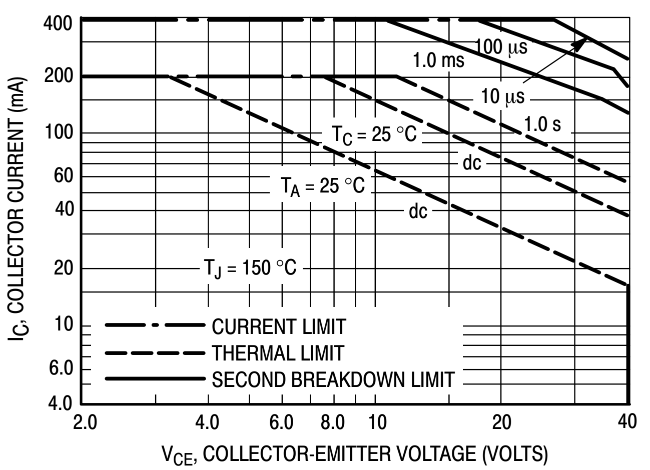
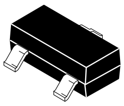


Figure 22.

The safe operating area curves indicate I_C−V_{CE} limits of the transistor that must be observed for reliable operation. Collector load lines for specific circuits must fall below the limits indicated by the applicable curve.

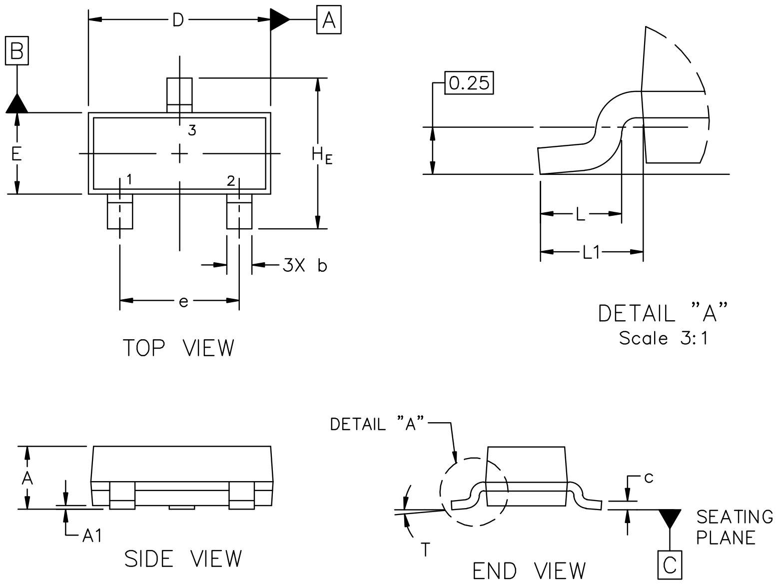
The data of Figure 22 is based upon $T_{J(pk)}$ = 150 °C; T_C or T_A is variable depending upon conditions. Pulse curves are valid for duty cycles to 10% provided $T_{J(pk)} \leq$ 150 °C. $T_{J(pk)}$ may be calculated from the data in Figure 20. At high case or ambient temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.



SCALE 4:1

SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

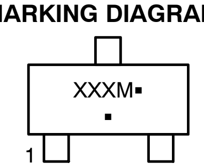
DATE 14 AUG 2024



MILLIMETERS			
DIM	MIN	NOM	MAX
A	0.89	1.00	1.11
A1	0.01	0.06	0.10
b	0.37	0.44	0.50
c	0.08	0.14	0.20
D	2.80	2.90	3.04
E	1.20	1.30	1.40
e	1.78	1.90	2.04
L	0.30	0.43	0.55
L1	0.35	0.54	0.69
H_E	2.10	2.40	2.64
T	0°	---	10°

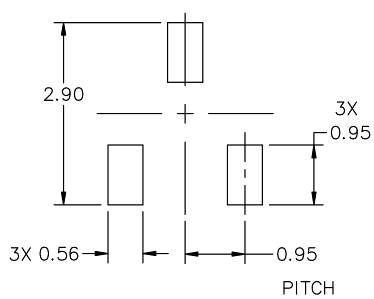
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF THE BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLES ON PAGE 2

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SOT−23 (TO−236) 2.90x1.30x1.00 1.90P
CASE 318
ISSUE AU

DATE 14 AUG 2024

STYLE 1 THRU 5:
CANCELLED

STYLE 6:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 7:
PIN 1. EMITTER
2. BASE
3. COLLECTOR

STYLE 8:
PIN 1. ANODE
2. NO CONNECTION
3. CATHODE

STYLE 9:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 10:
PIN 1. DRAIN
2. SOURCE
3. GATE

STYLE 11:
PIN 1. ANODE
2. CATHODE
3. CATHODE−ANODE

STYLE 12:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 13:
PIN 1. SOURCE
2. DRAIN
3. GATE

STYLE 14:
PIN 1. CATHODE
2. GATE
3. ANODE

STYLE 15:
PIN 1. GATE
2. CATHODE
3. ANODE

STYLE 16:
PIN 1. ANODE
2. CATHODE
3. CATHODE

STYLE 17:
PIN 1. NO CONNECTION
2. ANODE
3. CATHODE

STYLE 18:
PIN 1. NO CONNECTION
2. CATHODE
3. ANODE

STYLE 19:
PIN 1. CATHODE
2. ANODE
3. CATHODE−ANODE

STYLE 20:
PIN 1. CATHODE
2. ANODE
3. GATE

STYLE 21:
PIN 1. GATE
2. SOURCE
3. DRAIN

STYLE 22:
PIN 1. RETURN
2. OUTPUT
3. INPUT

STYLE 23:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 24:
PIN 1. GATE
2. DRAIN
3. SOURCE

STYLE 25:
PIN 1. ANODE
2. CATHODE
3. GATE

STYLE 26:
PIN 1. CATHODE
2. ANODE
3. NO CONNECTION

STYLE 27:
PIN 1. CATHODE
2. CATHODE
3. CATHODE

STYLE 28:
PIN 1. ANODE
2. ANODE
3. ANODE

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