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8-Input Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

The MC74ACT323 is an 8-bit universal shift/storage register with3-state outputs. Its function is similar to the MC74ACT299 with the exception of Synchronous Reset. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

- Common Parallel I/O for Reduced Pin Count
- Additional Serial Inputs and Outputs for Expansion
- Four Operating Modes: Shift Left, Shift Right, Load and Store
- 3-State Outputs for Bus-Oriented Applications
- Outputs Source/Sink 24 mA
- TTL Compatible Inputs

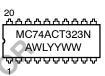


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MARKING DIAGRAMS







SO-20 DW SUFFIX CASE 751D





TSSOP-20 DT SUFFIX CASE 948E



A = Assembly Location

L, WL = Wafer Lot Y, YY = Year W, WW = Work Week

ORDERING INFORMATION

Device	Package	Shipping						
MC74ACT323N	PDIP-20	18 Units/Rail						
MC74ACT323DW	SOIC-20	38 Units/Rail						
MC74ACT323DWR2	SOIC-20	1000 Tape & Reel						
MC74ACT323DT	TSSOP-20	75 Units/Rail						
MC74ACT323DTR2	TSSOP-20	2500 Tape & Reel						

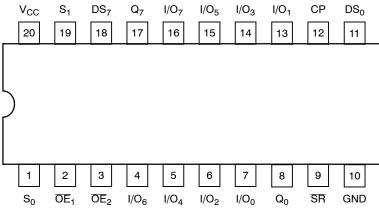


Figure 1. Pinout: 20-Lead Packages Conductors (Top View)

PIN ASSIGNMENT

PIN	FUNCTION				
СР	Clock Pulse Input				
DS ₀	Serial Data Input for Right Shift				
DS ₇	Serial Data Input for Left Shift				
S ₀ , S ₁	Mode Select Inputs				
SR	Synchronous Master Reset				
$\overline{OE}_{1,}\overline{OE}_{2}$	3-State Output Enable Inputs				
I/O ₀ –I/O ₇	Multipled Parallel Data Inputs or 3-State Parallel Data Outputs				
Q ₀ , Q ₇	Serial Outputs				

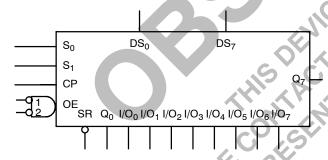


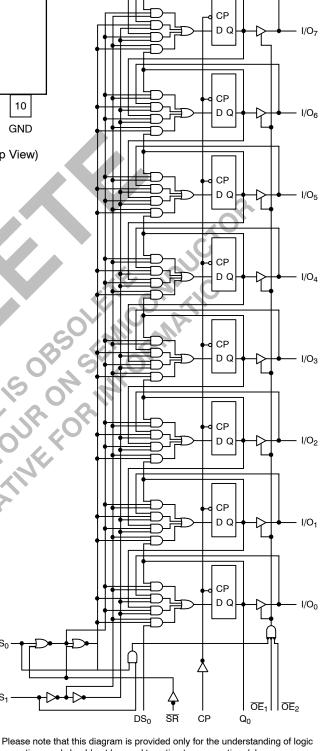
Figure 3. Logic Symbol

TRUTH TABLE

	Inputs			
SR	S ₁	S ₀	СР	Response
L	Х	Х	۲	Synchronous Reset; Q ₀ – Q ₇ = LOW
Н	Н	Н	工	Parallel Load; $I/O_n \rightarrow Q_n$
Н	L	Н	工	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
Н	Н	L	工	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
Н	L	L	Х	Hold

H = HIGH Voltage Level X = Immaterial

L = LOW Voltage Level



DS₇

operations and should not be used to estimate propagation delays.

Figure 2. LOGIC DIAGRAM

FUNCTIONAL DESCRIPTION

The MC74ACT323 contains eight edge- triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3 state buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on \overline{SR} overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP.

All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

A HIGH signal on either \overline{OE}_1 or \overline{OE}_2 disables the 3-state buffers and puts the I/O pins in the high impedance state. In this condition the shift, hold, load and reset operations can still occur. The 3-state buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

MAXIMUM RATINGS (Note 1)

Symbol	Parameter		Value	Unit
V _{CC}	DC Supply Voltage		-0.5 to +7.0	V
VI	DC Input Voltage		$-0.5 \le V_{J} \le V_{CC} + 0.5$	V
Vo	DC Output Voltage	(Note 2)	$-0.5 \le V_{O} \le V_{CC} + 0.5$	V
I _{IK}	DC Input Diode Current		±20	mA
I _{OK}	DC Output Diode Current		±50	mA
Io	DC Output Sink/Source Current		±50	mA
I _{CC}	DC Supply Current per Output Pin	SIMI	±50	mA
I _{GND}	DC Ground Current per Output Pin	00 00	±50	mA
T _{STG}	Storage Temperature Range	Nr 42 2	-65 to +150	°C
T _L	Lead temperature, 1 mm from Case for 10 Seconds	12.0,111	260	°C
TJ	Junction temperature under Bias	11/2 0/2	+ 150	°C
θ_{JA}	Thermal resistance	PDIP SOIC TSSOP	67 96 128	°C/W
P _D	Power Dissipation in Still Air at 85°C	PDIP SOIC TSSOP	750 500 450	mW
MSL	Moisture Sensitivity		Level 1	
F _R	Flammability Rating	Oxygen Index: 30% - 35%	UL 94 V-0 @ 0.125 in	
V _{ESD}	6 AY	uman Body Model (Note 3) Machine Model (Note 4) ged Device Model (Note 5)	> 2000 > 200 >1000	V
I _{Latch-Up}	Latch-Up Performance Above V _{CC} and B	elow GND at 85°C (Note 6)	± 100	mA
				•

Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Extended exposure to these
conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum-rated
conditions is not implied.

^{2.} IO absolute maximum rating must be observed.

^{3.} Tested to EIA/JESD22-A114-A.

^{4.} Tested to EIA/JESD22-A115-A.

^{5.} Tested to JESD22-C101-A.

^{6.} Tested to EIA/JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Тур	Max	Unit
V _{CC}	DC Input Voltage (Referenced to GND)				5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)				V _{CC}	V
T _A	Operating Temperature, All Package Types		-40	25	+85	°C
t _r , t _f	Input Rise and Fall Time (Note 8)	V _{CC} = 4.5 V V _{CC} = 5.5 V	0 0	10 8.0	10 8.0	ns/V
TJ	Junction Temperature (PDIP)				140	°C
I _{OH}	Output Current – High				-24	mA
I _{OL}	Output Current - Low				24	mA

DC CHARACTERISTICS

			T _A = -	+25°C	T _A = -40°C to +85°C		OP	
Symbol	Parameter	V _{CC} (V)	Тур	Guar	anteed Limits	Unit	Conditions	
V _{IH}	Minimum High Level Input Voltage	4.5 5.5	1.5 1.5	2.0 2.0	2.0 2.0	V V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
V _{IL}	Maximum Low Level Input Voltage	4.5 5.5	1.5 1.5	0.8 0.8	0.8 0.8	C V	V _{OUT} = 0.1 V or V _{CC} - 0.1 V	
V _{OH}	Minimum High Level Output Voltage	4.5 5.5	4.49 5.49	4.4 5.4	4.4 5.4	V V	I _{OUT} = -50 μA	
		4.5 5.5		3.86 4.86	3.76 4.76	\ \ \	$^*V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 m -24	
V _{OL}	Maximum Low Level Output Voltage	4.5 5.5	0.001 0.001	0.1 0.1	0.1 0.1	V	Ι _{ΟUT} = 50 μΑ	
		4.5 5.5	1	0.36 0.36	0.44 0.44	V	$^{*}V_{IN} = V_{IL} \text{ or } V_{IH}$ -24 -24	
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μΑ	$V_I = V_{CC}$, GND	
ΔI_{CCT}	Additional Maximum I _{CC} /Input	5.5	0.6	•	1.5	mA	V _I = V _{CC} - 2.1 V	
l _{OZ}	Maximum 3-State Current	5.5		±0.5	±5.0	μΑ	V_{I} (OE) = V_{IL} , V_{IH} V_{I} = V_{CC} , GND V_{O} = V_{CC} , GND	
I _{OLD} I _{OHD}	†Minimum Dynamic Output Current	5.5 5.5			75 –75	mA mA	V _{OLD} = 1.65 V Max V _{OHD} = 3.85 V Min	
I _{CC}	Maximum Quiescent Supply Current	5.5		8.0	80	μΑ	V _{IN} = V _{CC} or GND	

^{*}All outputs loaded; thresholds on input associated with output under test.

^{7.} Unused Inputs may not be left open. All inputs must be tied to a high voltage level or low logic voltage level.
8. V_{in} from 0.8 V to 2.0 V; refer to individual Data Sheets for devices that differ from the typical input rise and fall times.

[†]Maximum test duration 2.0 ms, one output loaded at a time.

AC CHARACTERISTICS $t_r = t_f = 3.0$ ns (For Figures and Waveforms, See Figures 4 and 5.)

				T _A = +25°C C _L = 50 pF			T _A = -40°0 C _L =		
Symbol	Parame	ter	V _{CC} * (V)	Min	Тур	Max	Min	Max	Unit
f _{max}	Maximum Input Freque	ncy	5.0	120	125		110		MHz
t _{PLH}	Propagation Delay	CP to Q _{0 or} Q ₇	5.0	5.0	9.0	12.5	4.0	14	ns
t _{PHL}	Propagation Delay	CP to Q _{0 or} Q ₇	5.0	5.0	9.0	13.5	4.5	15	ns
t _{PLH}	Propagation Delay	CP to I/O _n	5.0	5.0	8.5	12.5	4.5	14.5	ns
t _{PZH}	Output Enable Time		5.0	3.5	7.5	11	3.0	12.5	ns
t _{PZL}	Output Enable Time		5.0	3.5	7.5	11.5	3.0	13	ns
t _{PHZ}	Output Disable Time		5.0	4.0	8.5	12.5	3.0	13.5	ns
t _{PLZ}	Output Disable Time		5.0	3.0	8.0	11.5	2.5	12.5	ns

^{*}Voltage Range 5.0 V is 5.0 V \pm 0.5 V

AC OPERATING REQUIREMENTS

Symbol	I Parameter			T _A = +25°C C _L = 50 pF	$T_A = -40$ °C to +85°C $C_L = 50 \text{ pF}$	Unit
			Тур	Guarant	eed Minimum	
ts	Setup Time, HIGH or LOW S ₀ or S ₁ to CP	5.0	2.0	5.0	5.0	ns
t _h	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0	1.5	1.5	ns
ts	Setup Time, HIGH or LOW I/On, DS ₀ , DS ₇ to CP	5.0	1.0	4.0	4.5	ns
t _h	Hold Time, HIGH or LOW I/O _n , DS ₀ , DS ₇ to CP	5.0	0	1.0	1.0	ns
t _s	Setup Time, HIGH or LOW SR to CP	5.0	1.0	2.5	2.5	ns
t _h	Hold Time, HIGH or LOW SR to CP	5.0	0	1.0	1.0	ns
t _w	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns

^{*}Voltage Range 5.0 V is 5.0 V ±0.5 V

CAPACITANCE

Symbol	Parameter	Value Typ	Unit	Test Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = 5.0 V
C _{PD}	Power Dissipation Capacitance	170	pF	V _{CC} = 5.0 V

SWITCHING WAVEFORMS

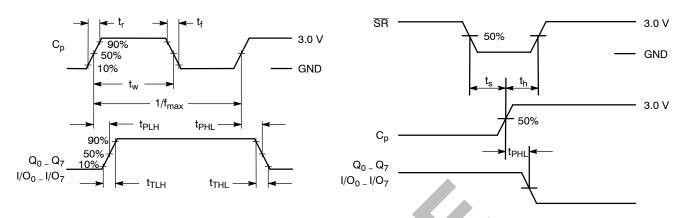


Figure 4.

Figure 5.

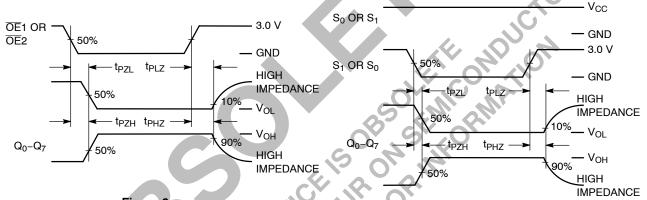


Figure 6.

Figure 7.

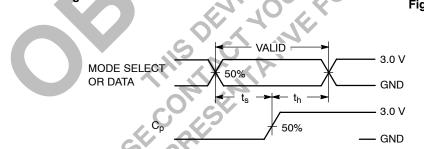
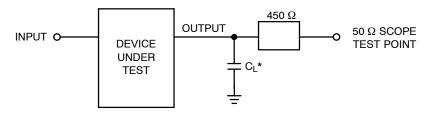


Figure 8.

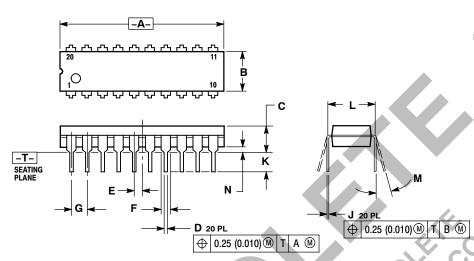


*Includes all probe and jig capacitance

Figure 9. Test Circuit

PACKAGE DIMENSIONS

PDIP-20 **N SUFFIX** 20 PIN PLASTIC DIP PACKAGE CASE 738-03 **ISSUE E**

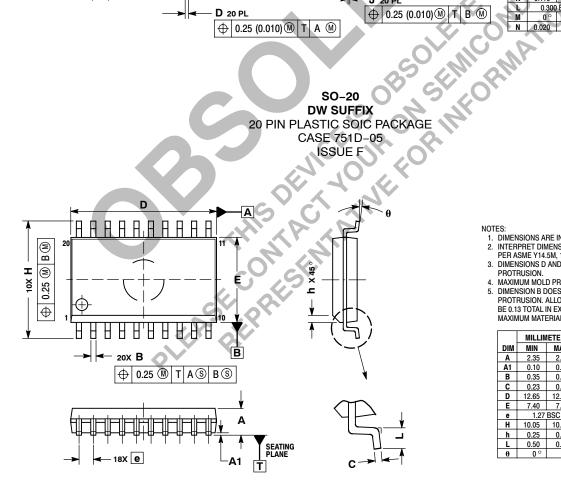


NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

 4. DIMENSION B DOES NOT INCLUDE MOLD

	INC	HES	MILLIMETERS		
DIM	MIN	MAX	MIN	MAX	
Α	1.010	1.070	25.66	27.17	
В	0.240	0.260	6.10	6.60	
С	0.150	0.180	3.81	4.57	
D	0.015	0.022	0.39	0.55	
Е	0.050	BSC	1.27 BSC		
F	0.050	0.070	1.27	1.77	
G	0.100	BSC	2.54 BSC		
J∢	0.008	0.015	0.21	0.38	
K	0.110	0.140	2.80	3.55	
	0.300 BSC		7.62 BSC		
M	0°	15°	0°	15°	
N	0.020	0.040	0.51	1.01	



- NOTES:

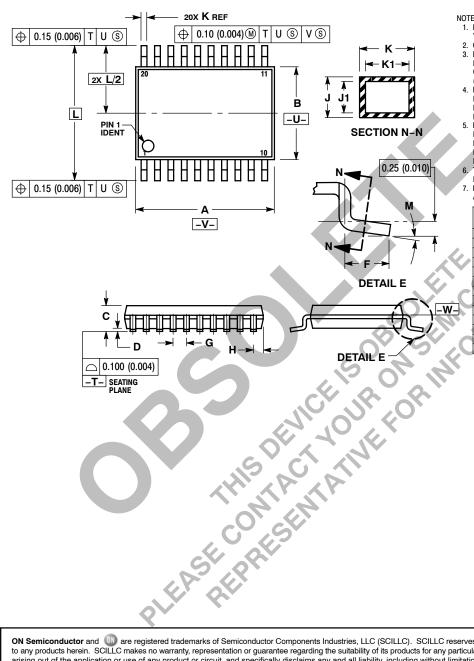
 1. DIMENSIONS ARE IN MILLIMETERS.
 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
- 3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
- MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
 DIMENSION B DOES NOT INCLUDE DAMBAR
 PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS					
DIM	MIN	MAX				
Α	2.35	2.65				
A1	0.10	0.25				
В	0.35	0.49				
С	0.23	0.32				
D	12.65	12.95				
Е	7.40	7.60				
е	1.27	BSC				
Н	10.05	10.55				
h	0.25	0.75				
Ĺ	0.50	0.90				
А	N٥	7 0				

PACKAGE DIMENSIONS

TSSOP-20 **DT SUFFIX**

20 PIN PLASTIC TSSOP PACKAGE CASE 948E-02 **ISSUE A**



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15
- (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE INTERLEAD
 FLASH OR PROTRUSION. INTERLEAD FLASH OR
 PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 DIMENSION K DOES NOT INCLUDE DAMBAR
- PROTRUSION. ALLOWABLE DAMBAR
 PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES	
DIM	MIN	MAX	MIN	MAX	
Α	6.40	6.60	0.252	0.260	
В	4.30	4.50	0.169	0.177	
С	1	1.20	ļ	0.047	
D	0.05	0.15	0.002	0.006	
F	0.50	0.75	0.020	0.030	
G	0.65	BSC	0.026 BSC		
H	0.27	0.37	0.011	0.015	
J	0.09	0.20	0.004	0.008	
J1_	0.09	0.16	0.004	0.006	
K	0.19	0.30	0.007	0.012	
K1.	0.19	0.25	0.007	0.010	
	6.40 BSC		0.252 BSC		
M	0°	8°	0°	8°	

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