16-bit Microcontroller 512K-byte Flash ROM / 47.5K-byte RAM / 100-pin

LC88FC3H0A is a 16-bit Microcontroller with 512K-byte Flash ROM/47.5Kbyte RAM in 100-pin package. Main features are infrared remote controller receiver circuit (supports PPM and Manchester encoding), 16 channels of 12bit resolution ADC, internal reset circuit, CRC circuit and etc. that are software friendly circuits and these peripheral circuit can contribute to less external components. Also, plenty of serial interface circuits (synchronous serial \times 3, $I^2C \times 3$, UART \times 3) can communicate with other LSIs and are suitable for home appliances and white goods which need complicated control. For software development, there is our original software development environment and with On-Chip Debugging function, it is easy to debug with user's actual application.

Features

- 16-channel 12-bit resolution AD converter
- Infrared remote controller receiver circuit
- CRC operating circuit
- Internal Reset Function

Performance

• 100ns (10.0MHz) VDD=2.7 to 3.6V Ta=-40°C to +85

Function Descriptions

- Xstromy16 CPU
 - 4G-byte address space
 - General-purpose registers: 16 bits × 16 registers
- Ports
 - I/O Ports 86
 - Power supply pins 8 (VSS1 to VSS4, VOD1 to VDD4
- Timer
 - 16-bit timers $\times 8$
- Base timer serving as a time-of-day clock
- Serial interfaces
- Synchronous SIO interfaces × 3
- (with automatic transmission capability)
- Single master I²C/synchronous StO interface $\times 2$
- Slave 1²C/synchronous SIO interface
- Asynchronous SIO (UAR^T) interfaces × 3
- Multifrequency 12-bit PV/M modules
- 16-channel 12-bit resolution AD converter
- Watchdog timer
- Infrared remote controller receiver circuit
- CRC operating circuit
- Real time clock
- System clock frequency divider
- CF oscillator circuit, Crystal oscillator circuit, RC oscillator circuit
- 61-source 14-vector interrupt feature
- On-chip debugger function

Application

Home audio, White goods

* This product is licensed from Silicon Storage Technology, Inc. (USA).

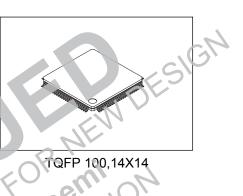
ORDERING INFORMATION

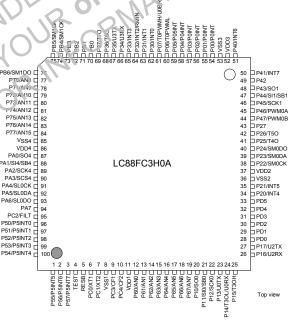
See detailed ordering and shipping information on page 48 of this data sheet.



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Pin Assignment (Top view)

Function Details

- Xstromy16 CPU
 - 4G-byte address space
 - General-purpose registers : 16 bits × 16 registers

■ Flash ROM

- 524288 × 8 bits
- Programming voltage level : 2.7 to 3.6V.
- Block-erasable in 2K byte units.
- Data written in 2-byte units.

■ RAM

- 48640 × 8 bits
- Minimum instruction cycle time (tCYC)
 100 ns (10 MHz), V_{DD} = 2.7 to 3.6V
- Ports
 - Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1 bit units : 86 (P0n P1n, P2n, P3n, P4n, P5n, P6n, P7n, PAn PB0 to PB6, PC2, PD0 to PD5)

4 (PC0, PC1, PC3, PC4)

DD1 to 4)

(RESB)

(VSS1 to

1 (TEST)

ESIGN

- Oscillation/normal withstand voltage I/O ports
- Reset pins
- TEST pins
- Power pins
- Timers
 - Timer 0 : 16-bit timer that supports PW M/toggle outputs
 - <1> 5-bit prescaler
 - <2> 8-bit PWM × 2 8-bit timer + 8-bit PWM mode selectable
 - <3> Clock som ce selectable from sys em clock. CSC0, OSC1, and internal RC oscillator.
 - Timer 1 : 16-bit timer with capture registers
 - <1>5-bit prescale
 - 2> May be divided into 2 channels of 8 bit time:
 - <3> Clock source scleetable from system clock_OSC0, OSC1, and internal RC oscillator
 - Timer 2 : 16-bit timer with captur : registers
 - >4-bit prescaler
 - <2> May be divided into 2 channels of 8-bit timer
 - <3> Clock source selectable from system clock, OSC0, OSC1, and external events
 - Timer 3 : 16-bit timer that shpports PWM/toggle outputs
 - <1> 8-bit prescaler
 - <2> 8-bit timer > 2ch or 8-bit timer+8-bit PWM mode selectable

<3> Clock source selectable from system clock, OSC0, OSC1, and external events

- Timer 4 : 16-bit timer that supports toggle outputs
 - <1> Clock source selectable from system clock and prescaler 0
- Timer 5 : 16-bit timer that supports toggle output
 - <1> Clock source selectable from system clock and prescaler 0
- Timer 6 : 16-bit timer that supports toggle outputs
 - ${<}1{>}\operatorname{Clock}$ source selectable from system clock and prescaler 1
- Timer 7 : 16-bit timer that supports toggle output
 - ${<}1{>}\operatorname{Clock}$ source selectable from system clock and prescaler 1

*Prescaler 0 and 1 are consisted of 4bits and can choose their clock source from OSC0 or OSC1.

- Base timer
 - <1> Clock may be selected from OSC0 (32.768 kHz crystal oscillator) and frequency-divided output of system clock.
 - <2> Interrupts can be generated in 7 timing schemes.

■ Real time clock

- <1> Calender with Jan. 1, 2000 to Dec.31, 2799 including automatic leapyear calculation function.
- <2> Consisted of Indipendent second-minuit-hour-day-month-yeare-century counters.
- Serial interfaces
 - SIO0 : 8-bit synchronous SIO
 - <1> LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
 - SIO1 : 8-bit synchronous SIO
 - <1>LSB first/MSB first mode selectable
 - N DESIGN <2> Supports data communication with a data length of 8 bits or less (1 to 8 bits specifiable)
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9- to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
 - SIO4 : 8-bit synchronous SIO
 - <1>LSB first/MSB first mode selectable
 - <2> Supports data communication with a data length of 8 b. or less (1 to 8 bits specifiable) OR INFORMATION
 - <3> Built-in 8-bit baudrate generator (4 tCYC to 512 tCYC transfer clocks)
 - <4> Continuous/automatic data transmission (9) to 32768-bit units specifiable)
 - <5> Interval function (intervals specifiable in 0 to 64tSCK units)
 - <6> Wakeup function
 - SMIIC0 : Single master I²C/8-bit synchronous SIO Mode 0 : Single-master mode communication
 - Mode 1 : Synchronous 8-bit serial I/O (MSB first)
 - SMIIC1 : Single master I²C 8-bit synchronous SIO Mode 0 : Single-master mode communication Mode 1 : Synchronous 8-bit serial I/O (MSB first)
- SLIIC0 : Slave I²C/8-bit synchronous SIO Mode $0: I^2C$ slave mode communication Mode 1 : Synchronous 8-bit serial I/O (MSB first) THIS DEVICE PLEASEN Note: usable only with the external clock source

• UART0

<1> Data length : 8 bits (LSB first)

<2> Start bits : 1 bit

<3> Stop bits : 1 bit

<4> Parity bits : None/even parity/odd parity

- <5> Transfer rate : 4/8 cycle
- <6> Baudrate source clock: P07 input signal used as a 1 cycle signal (T0PWMH can be used as a clock source) or Timer4 cycle.
- <7> Full duplex communication
- Note : The "cycle" refers to one period of the baudrate clock source.

• UART2

- <1> Data length : 8 bits (LSB first)
- : 1 bit <2> Start bits
- <3> Stop bits : 1/2 bit
- : None/even parity/odd parity <4> Parity bits
- <5> Transfer rate : 8 to 4096 cycle
- OR NEW DESIGN nsemi RMATION <6> Baudrate source clock: System clock/OSC0/OSC1/P26 input signal
- <7> Wakeup function
- <8> Full duplex communication

Note : The "cycle" refers to one period of the baudrate clock source

• UART3

- <1> Data length : 8 bits (LSB first)
- <2> Start bits : 1 bit
- <3> Stop bits : 1/2 bit
- : None/even parity/odd parity <4> Parity bits
- <5> Transfer rate : 8 to 4096 cycle
- <6> Baudrate source clock: System clock/OSC /OSC1/P36 input signal
- <7> Wakeup function
- <8> Full duplex communication
- Note : The "cycle" refers to one period of the bandrate clock sour

■ AD converter

- <1>12/8 bits resolution selectable
- <2> Analog input: 16 channels
- <3> Comparator mode

🗆 PWM

- PWM 0 : Multifrequency 12 bit PWM × 2 channels (PWM0A and PWM0B)
 - <1> 2-channel pairs controlled independently of one another
 - <2> Clock source selectable from system clock or OSC1
 - <3> 8-bit prescaler: TPW1/R0= (prescaler value + 1) × clock period
 - <4> 8-bit fundamental wave PWM generator circuit + 4-bit additional pulse generator circuit
 - <5> Fundamental wave PWM mode
 - Fundamental wave period : 16 TPWMR0 to 256 TPWMR0
 - High pulse width : 0 to (Fundamental wave period - TPWMR0)
 - <6> Fundamental wave + additional pulse mode
 - Fundamental wave period : 16 TPWMR0 to 256 TPWMR0
 - Overall period : Fundamental wave period $\times 16$
 - High pulse width : 0 to (Fundamental wave period - TPWMR0)
- CRC operating circuit
- Watchdog timer
 - <1> Driven by the base timer + internal watchdog timer dedicated counter
 - <2> Interrupt or reset mode selectable

- Infrared Remote Controller Receiver Circuit
 - 1) Noise rejection function (noise filter time constant: Approx. 120µs when the 32.768kHz crystal oscillator is selected as the reference clock source)
 - 2) Supports data encording systems such as PPM (Pulse Position Modulation) and Manchester encording
 - 3) X'tal HOLD mode release function
- Internal Reset Function
 - Power-on reset (POR) function
 - 1) POR reset is generated only at power-on time.
 - 2) The POR release level can be selected through option configuration.
 - Low-voltage detection reset (LVD) function
 - 1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
 - 2) The use/disuse of the LVD function and the low voltage threshold level can be selected by option configuration.
- Interrupts (peripheral function)
 - 61 sources (33 modules), 14 vector addresses
 - <1> Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
 - <2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence

No	o .	Vector Address	Interrupt Module
1		08000H	Watchdog timer (1)
2	2	08004H	Base timer (2)
3		08008H	Timer 0 (2)
4	Ļ	0800CH	INT ⁽¹⁾
5	;	08014H	INT1 (1)
6	5	08018H	INT2 (1) / timer 1 (2) / UAKT2 (4)
7		0801CH	INT3 (1) / timer 2 (4) / SMIIC0 (1) / SLIIC1 (1)
8		08020Н	IN14 (1) / timer 3 (2) / Infared remote control receiver(4)
9		08024H	INT5 (1) / timer 4 (1) / SIO1 (2)
	0	0802CH	PWM0(1)/SMIIC1(1)
1	<u>i</u>	08020H	ADC (1) / timer 5 (1) / SIO4(2)
	2	08034H	INT6 (1) / timer 6 (1) / UART 3 (4)
	3	08038H	INT7 (1) / SIO0 (2) / SIO0(2)
14	4	0803CH	Port 0 (3) / Port 5 (8) / RTC (1) / CRC (1)

- 3 priority levels selectable
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

• A number enclosed in parentheses denotes the number of sources.

- Subroutine stack : RAM area
- Subroutine calls that automatically save PSW, interrupt vector calls: 6 bytes
- Subroutine calls that do not automatically save PSW: 4 bytes
- Multiplication/division instructions
 - 16 bits × 16 bits (4 tCYC execution time)
 - 16 bits ÷ 16 bits (18 to 19 tCYC execution time)
 - 32 bits ÷ 16 bits (18 to 19 tCYC execution time)

Oscillator circuits

- RC oscillator circuit (internal)
- : For system clock
- CF oscillator circuit (built-in Rf circuit) : For system clock(OSC1)
- Crystal oscillator circuit (built-in Rf circuit) : For low-speed system clock (OSC0)

 SLRC oscillator circuit (internal) : For system clock (In the case of exception processing)

- VCO oscillator circuit
- : For timer3, 4, 5, 6, 7 clock
- System clock divider function
 - Can run on low current.
 - 1/1 to 1/128 of the system clock frequency can be set.
- Standby function
 - HALT mode : Halts instruction execution while allowing the peripheral circuits to continue operation. DESIGN
 - <1> Oscillation is not stopped automatically.
 - <2> Released by a system reset or occurrence of an interrupt.
 - HOLD mode : Suspends instruction execution and the operation of the peripher circu
 - <1>OSC1, RC, and OSC0 oscillations automatically stop.
 - <2> There are six ways of releasing the HOLD mode:
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INT0, INT1, INT2, INT4, INT5, INT6, and INT7 pirs to the specified level
 - (3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established at port 5
 - (5) Having an interrupt established at SICO. SIO1 or SIO4
 - (6) Having an interrupt established at UART2 or UART3
 - HOLDX mode : Suspends instruction execution and the operation of the peripheral circuits except those
 - which run on OSCO. <1> OSC1 and RC oscillations automatically stop.
 - <2> OSC0 maintains the state that is established when the HOLDX mode is entered.
 - <3> There are nine ways of releasing the HOLDX mode.
 - (1) Setting the reset pin to the low level
 - (2) Setting at least one of the INTO, INTO level
 - 3) Having an interrupt source established at port 0
 - (4) Having an interrupt source established at port 5
 - (5) Having an interrupt source established at the base timer circuit
 - (6) Having an interrupt established at SIO0, SIO1 or SIO4
 - (7) Having an interrupt established at UART2 or UATR3
 - (8) Having an interrupt established at Infared remote control receiver.
 - (9) Having an interrupt source established at the real time clock circuit
- On-chip debugger function
 - Supports software debugging with the IC mounted on the target board.
 - Supports source line debugging and tracing functions, and breakpoint setting and real time display.
 - Single-wire communication
- Package form
 - TQFP100, 14×14 : Pb-Free and Halogen Free type

Development tools

• On-chip debugger : EOCUIF1 or EOCUIF2 + LC88FC3H0A

Programming board

1	Package	Programming Board
	TQFP 100, 14 × 14	W88F52TQ

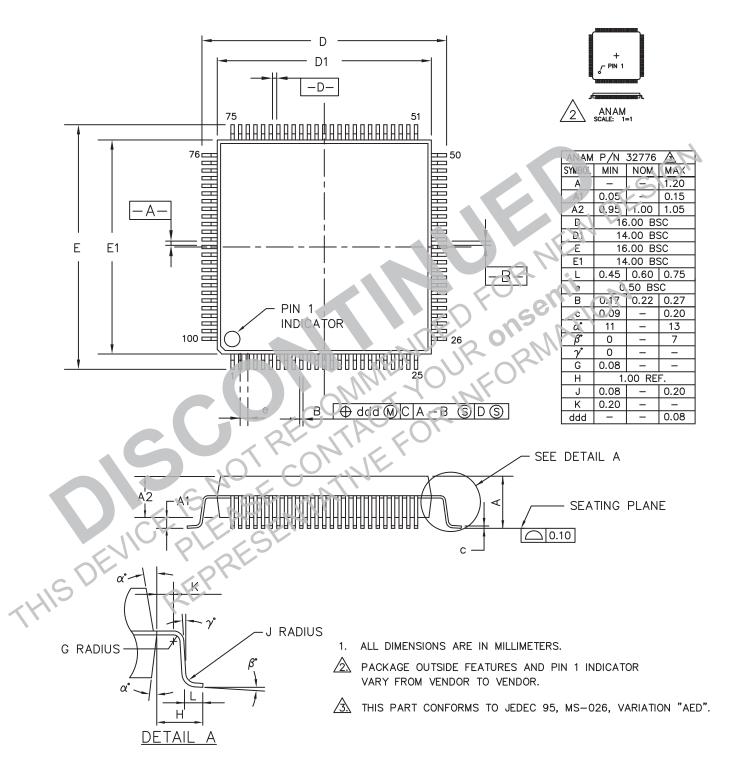
■ Flash ROM Programmer

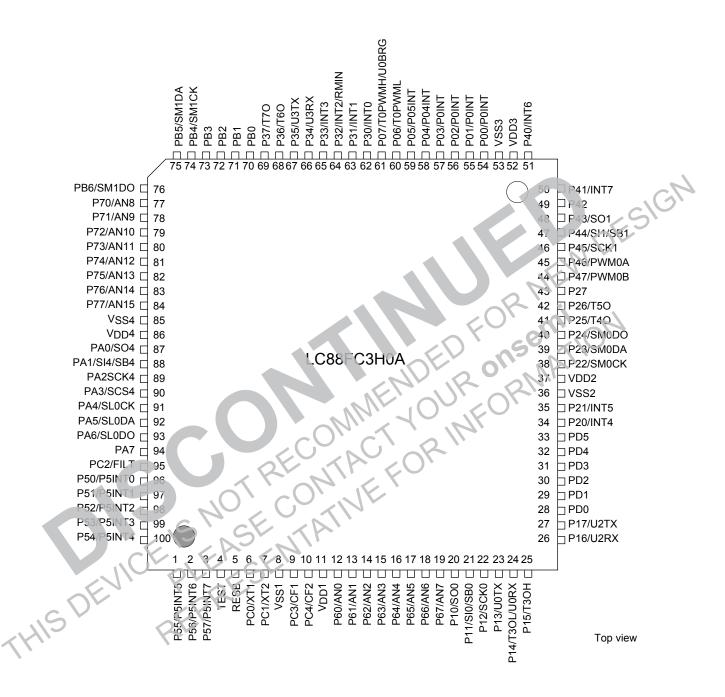
	Mak	er	Model	Supported Version	Device
	ON	Single / Gang programmer	SKK Type C (SanyoFWS)	Application Version After 1.08A Chip Data Version After 2.51	LC88FC3x0
	Semiconductor	On-board Single programmer	FWS-X16DI Type 3	Application Version After 1.08A Chip Data Version After 2.51	LC88FC3x0
THIS	DEVICE	S NOI PLEAS PLEAS	RECONNE HOR CONTRECOR	D FOR NE	N ion

Package Dimensions

unit : mm

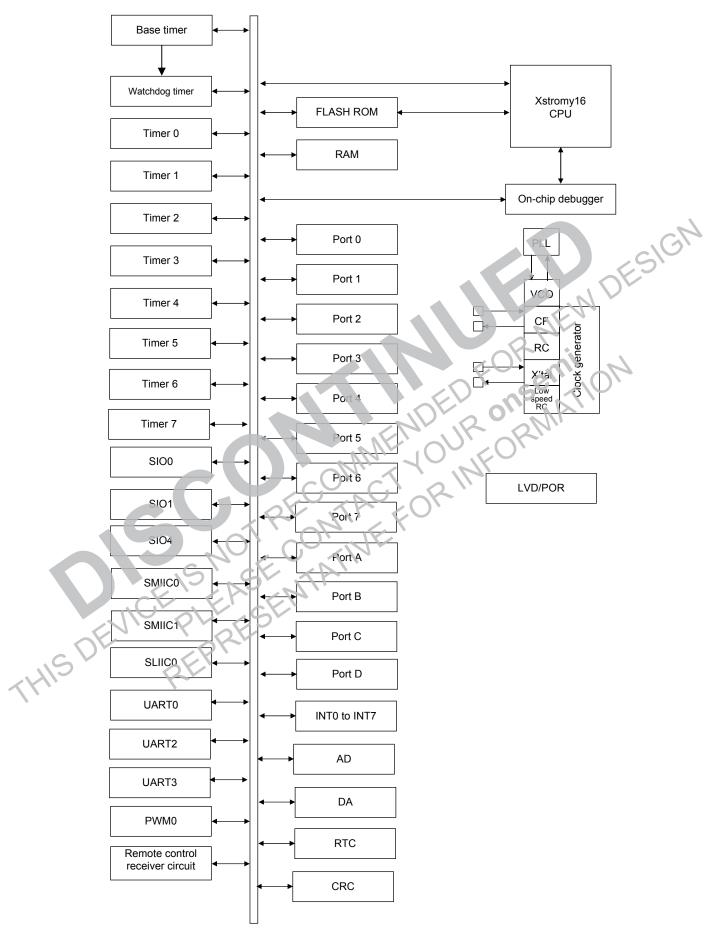
TQFP 100, 14x14 CASE 932AN-01 ISSUE O





TQFP100,14×14 (Pb-Free and Halogen Free type)

System Block Diagram



Pin Description

Pin Name	I/O	Description
VSS1, VSS2,	_	– power sources
VSS3, VSS4		
VDD1, VDD2,	_	+ power sources
VDD3, VDD4		
Port 0	I/O	• 8-bit I/O port
P00 to P07		• I/O specifiable in 1-bit units
100 10 107		• Pull-up resistors can be turned on and off in 1 bit units
		• HOLD release input (P00 to P03, P04, P05)
		• Port 0 interrupt input (P00 to P03, P04, P05)
		• Pin functions
		P06 : Timer 0L output
		P07 : Timer 0L output/UART0 clock input
Port 1	I/O	 8-bit I/O port I/O specifiable in 1-bit units Pull-up resistors can be turned on and off in 1 bit units Pin functions P10 : SIO0 data output
P10 to P17		• I/O specifiable in 1-bit units
P10 to P17		• Pull-up resistors can be turned on and off in 1 bit units
		• Pin functions
		P10 : SIO0 data output
		P11 : SIO0 data input/pulse input/output
		P12 : SIO0 clock input/output
		P13 : UARTO transmit
		P14 : Timer 3L output/UART0 receive
		P15 : Timer 3H output
		P16 : UART2 receive
		P13 : UART0 transmit P14 : Timer 3L output/UART0 receive P15 : Timer 3H output P16 : UART2 receive P17 : UART2 transmit
Port 2	I/O	• 8-bit I/O port
P20 to P27		• I/O specifiable in 1-bit units
F20 10 F27		• Pull-up resistors can be turned on and off in 1 bit units
		• Pin functions
		P20 : INT4 input/HOLD release input/timer 3 even. input/
		timer 2L capture input/time: 2H capture in sut
		P21 : INT5 input/HOLD release input/timer 3 event input/
		timer 2L capture input/timer 2H capture input
		P22.: SMIIC0 clock input/output
		P23 : SMICO bus input/output/data input
		P24 · SMIIC0 data output (used in 3-wire SIO mode)
	CX	P25. Timer 4 output
	\sim	F26 : Timer 5 output
EN		Interrupt acknowledge type
SDEV		IN 14, INT5 : H level, L level, H edge, L edge, both edges
0		
,		Continued on next page

Continued from preceding page.

Pin Name	I/O	Description
Port 3	I/O	• 8-bit I/O port
P30 to P37		• I/O specifiable in 1-bit units
1 50 10 1 57		• Pull-up resistors can be turned on and off in 1 bit units
		Pin functions
		P30 : INT0 input/HOLD release/timer 2L capture input
		P31 : INT1 input/HOLD release/timer 2H capture input
		P32 : INT2 input/HOLD release/timer 2 event input/timer 2L capture input/
		Infrared Remote Controller Receiver input P33 : INT3 input/HOLD release/timer 2 event input/timer 2H capture input
		P33 : UART3 receive
		P35 : UART3 transmit
		P36 : Timer 6 output
		P37 : Timer 7 output
		Interrupt acknowledge type
		INT0 to INT3 : H level, L level, H edge, L edge, both edges
Port 4	I/O	• 8-bit I/O port
P40 to P47		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1 bit units
		• Pin functions
		P40 : INT6 input/HOLD release input
		P41 : INT7 input/HOLD release input
		P43 : SIO1 data output
		P44 : SIO1 data input/bus input/output P45 : SIO1 clock input/output
		P46 : PWM0A output
		P47 : PWM0Boutput
		Interrupt acknowledge type
		INT6, INT7 : H level, L level, H edge, L edge, both edges
Port 5	I/O	• 8-bit I/O port
P50 to P57		• I/O specifiable in 1-bit units
		• Pull-up resistors can be turned on and off in 1 bit units
		HOLD release input
		Port 0 interrupt input
Port 6	I/O	8-bit I/O port
P60 to P67		• I/O specifiable in 1-bit units
10010107		Pull-up resistors can be surred on and off in 1 bit units
		• Pin functions
		ANO (P60) o AN7 (P67) · A D converter input port
Port 7	I/O	• 8-bit I/O port
	CV	• I/O specifiable in 1-bit units
P70 to P77	\sim	• Pull-up resistors can be turned on and off in 1 bit units
AL N		Pin functions
		ANS (P70) to AN15 (P77) : AD converter input port

Continued from preceding page.

Pin Name	I/O	Description
Port A	I/O	• 8-bit I/O port
PA0 to PA7	ł	• I/O specifiable in 1-bit units
rA0 to rA/		• Pull-up resistors can be turned on and off in 1 bit units
		• Multiplexed pin functions
		PA0 : SIO4 data output
		PA1 : SIO4 data input/pulse input/output
		PA2 : SIO4 clock input/output
		PA3 : SIO4 chip select input
		PA4 : SLIIC0 clock input
		PA5 : SLIIC0 bus input/output/data input
		PA6 : SLIIC0 data output (used in 3-wire SIO mode)
Port B	I/o	• 7-bit I/O port
PB0 to PB6		• I/O specifiable in 1-bit units
	l	• Pull-up resistors can be turned on and off in 1 bit units
		• Multiplexed pin functions
	l	PB4 : SMIIC1 clock input/output PB5 : SMIIC1 bus input/output/data input
	l	PB5 : SMIIC1 bus input/output/data input PB6 : SMIIC1 data output (used in 3-wire SIO mode)
Port C	I/O	Switc i data output (used in 5-wite Sto mode) So i Store i data output (used in 5-wite Store i output)
	1/0	• I/O specifiable in 1-bit units
PC0 to PC4	l	 I/O specifiable in 1-bit units Pull-up resistors can be turned on and off in 1 bit units (PC2) Pin functions PC0 : 32.768 kHz crystal oscillator input PC1 : 32.768 kHz crystal oscillator output PC2 : FILT of VCO PC3 : Ceramic oscillator input PC4 : Ceramic oscillator output/VCO output 6-bit I/O port I/O specifiable in 1-bit units
	l	Pin functions
		PC0 : 32.768 kHz crystal oscillator input
		PC1 : 32.768 kHz crystal oscillator output
	l	PC2 : FILT of VCO
		PC3 : Ceramic oscillator input
		PC4 : Ceramic oscillator output/VCO output
Port D	I/O	• 6-bit I/O port
PD0 to PD5	ł	• I/O specifiable in 1-bit units
	l	• Puil-up resistors can be turned on and off in 1 bit units
TEST	I/O	TEST pin
		Used to ommunicate with on-chip debugger.
		• Connects an external 100 k Ω pull-down resistor.
RESB	I/0	Reset pin
		NOTAN
RESB		• connects an external 100 kΩ pull-down resistor. Reset pin
		alt'sch
		Pr Co.
NY.		ORY
SV		

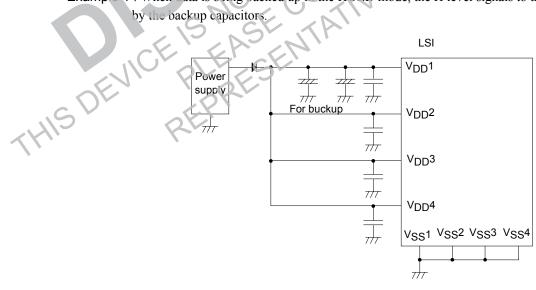
Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

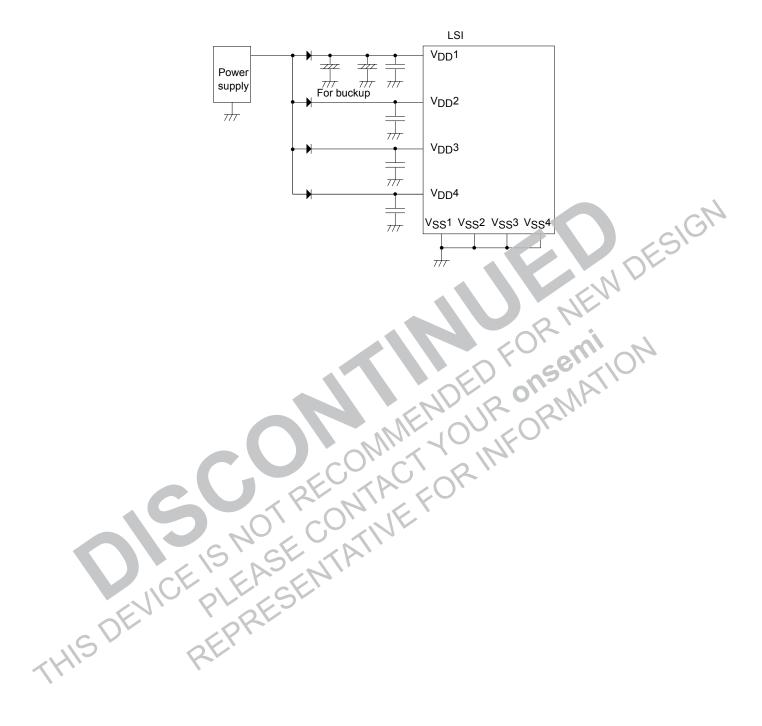
Port Name	Option Selected in Units of	Output Type	Pull-up Resistor
200 to P07		CMOS	
P10 to P17 P20 to P27 P30 to P37 P40 to P47 P50 to P57 P60 to P67 P70 to P77 PA0 to PA7 PB0 to PB6	1 bit	Able to program special functions'output type from CMOS output or Nch-opendrain	Programmable
60 to P67 70 to p77 D0 to PD5 C2		CMOS	EW
C0	_	N-channel open drain (32.768 kHz crystal oscillator input)	None
C1	-	Nch-open drain (32,768k kHz crystal oscillator output)	S None
C3	-	CMOS (ceramic oscillator input)	None
C4	-	CMOS (ceramic oscillator output)	None

* Make the following connection to minimize the noise input to the VDD1 pin and prolong the backup time. Be sure to electrically short the VSS1, VSS2, VSS3 and VSS4 pins.

Example 1: when data is being backed up in the HOLD mode, the H level signals to the output ports are fed by the backup capacitors



Example 2 : When data is being backed up in the HOLD mode, the H level output at any ports is not sustained and is unpredictable.



■ Absolute Maximum Ratings at Ta=25°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

	Parameter	Symbol	Applicable Pin	Conditions			Specific	cation	
	T drameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
	ximum supply tage	V _{DD} max	V _{DD} 1, V _{DD} 2, V _{DD} 3, V _{DD} 4	$V_{DD} = V_{DD} = V$		-0.3		+4.6	
Inp	ut voltage	VI (1)	RESB			-0.3		V _{DD} +0.3	v
Inp	ut/output voltage	VIO (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D			-0.3		VDD +0.3	, v
High level output current	Peak output current	IOPH (1)	Ports 0, 1, 2, 3 P40 to P45 Ports 7, A, D PB2 to PB6	CMOS output selected Per applicable pin		-7.5			
outp		IOPH (2)	P46, P47 PB0, PB1	Per applicable pin		-12.5			
ut curr		IOPH (3)	Port 5, 6 PC0 to PC4	Per applicable pin		-4.5			
ent	Average output current (Note 1-1)	IOMH (1)	Ports 0, 1, 2, 3 P40 to P45 Ports 5, 6, 7, A PB2 to PB6 Ports D	CMOS output selected Per applicable pin		-5			C.
		IOMH (2)	P46, P47 PB0, PB1	Per applicable pin		-10	NE		
		IOMH (3)	Port 5, 6 PC0 to PC4	Per applicable pin		2			
	Total output current	$\Sigma IOAH(1)$	Pprts 5 PC0 to PC4	Total of currents at applicable pins		-10	en	10	1
		$\Sigma IOAH (2)$	Port 6	Total of currents at applicable pins	EV	-10	NÁ		mA
		$\Sigma IOAH (3)$	Port 5, 6 PC0 to PC4	Fotal of currents at applicable pirs	N, P	-20	SU		
		$\Sigma IOAH (4)$	Ports 1,D1 P20 to P21	Total of currents at applicable bins	0,	-20			
		ΣΙΟΑΗ (5)	P22 to P27	Total of currents at applicable pins	70	-20			
		ΣΙΟΑΗ (6)	Ports 1, 2, D	Total of currents at applicable pins		-40			
		SIOAH (7)	Ports 4	Total of currents at applicable pins		-20			
		$\Sigma IOAH(8)$	Ports 0, 3	Total of currents at applicable pins		-20			
		ΣIOAH (9)	Port: 0, 3, 4	Total of currents at applicable pins		-40			
		Σ'OAH (10)	Ports B, 7	Total of currents at applicable pins		-20			
	EV.	ΣΙΟΑΙ' (11)	Poits A	Total of currents at applicable pins		-20			
~	V	ΣIOAH (12)	Ports 7, A, B	Total of currents at applicable pins		-40			

Continued from preceding page.

Para	ameter	Symbol	Applicable Pin	Conditions			Specific	cation	
1 are	ameter	5	/Remarks		V _{DD} [V]	min	typ	max	unit
	k output rent	IOPL (1)	Ports 0, 1, 3, 4 Ports 7, D P20, P21, P24 to P27 PA0 to PA4, PA6, PA7 PB0 to PB4, PB6,	Per applicable pin				15	
ut current		IOPL (2)	P22, P23 PA4, PA5 PB4, PB5	Per applicable pin				20	
H		IOPL (3)	Ports 5, 6 PC0 to PC4	Per applicable pin				7.5	
curi	erage output rent ote 1-1)	IOML (1)	Ports 0, 1, 3, 4 Ports 7, D P20, P21, P24 to P27 PA0 to PA4, PA6, PA7 PB0 to PB4, PB6, PB7	Per applicable pin				12.5	
		IOML (2)	P22, P23 PA4, PA5 PB4, PB5	Per applicable pin				15	K,S
		IOML (3)	Ports 5, 6 PC0 to PC4	Per applicable pin				5	
	al output rent	$\Sigma IOAL(1)$	Ports 5 PC0 to PC2	Total of currents at applicable pins			NE	10	mA
		$\Sigma IOAL(2)$	Port 6 PC3 to PC4	Total of currents at applicable pins				10	
		$\Sigma IOAL(3)$	Port 5, 6 PC0 to PC4	Total of currents at applicable pins			.en	20	4
		$\Sigma IOAL$ (4)	Ports 1, D P20, P21	Total of currents at applicable pins	EV	00	P N D	35	
		$\Sigma IOAL(5)$	P22 to P27	Total of currents at applicable pins	Y.R		Ż	35	
		$\Sigma IOAL$ (6)	Ports 1, 2, D	Total of currents at applicable pins	00,	çΟ`		70	
		ΣIOAL (7)	Port 4	Total of current, at applicable pins	71			35	
		ΣΙΟΑL (8)	Port 0, 5	Total of currents at appricable pins	Dr			35	
		ΣIOAL (9)	Port 0, 3, 4	Total of currents at applicable pins				70	
		ΣΙΟ AL (10)	Port [*] , B	Total of currents at applicable pins				35	
		ΣΙΟΑL (11)	Port A	Total of currents at applicable pins				35	
			Port 7, A, B	Total of currents at applicable pins				70	
Allowab dissipatio	le power on	Pa max	TQFP100	Ta=-40 to +85°C Package with thermal resistance bord (Note 1-2)				460	mW
Operatin temperat	g ambient ure	Topi		, ,		-40		+85	
Storage a	orage ambient mperature	Tstg				-55		+125	°C

Note 1-1 : Average output current refers to the average of output currents measured for a period of 100 ms. Note 1-2 : SEMI standards thermal resistance board (size : $76.1 \times 114.3 \times 1.6$ tmm, glass epoxy) is used.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Parameter	Symbol	Applicable Pin/Remarks	Conditions			Specific	cation	
Farameter	Symbol	Applicable Fill/Relliarks	Conditions	$V_{DD}[V]$	min	typ	max	unit
Operating supply voltage (Note 2-1)	V _{DD} (1)	V _{DD} 1=V _{DD} 2=V _{DD} 3	$0.098 \mu s \le tCYC \le 66 \mu s$		2.7		3.6	
Memory sustaining supply voltage	VHD	V _{DD} 1=V _{DD} 2=V _{DD} 3	RAM and register contents sustained in HOLD mode		2.0		3.6	
High level input voltage	VIH (1)	Ports 0, 1, 2, 3, 4 Port 5, A, B		2.7 to 3.6	0.3V _{DD} +0.7		V _{DD}	
	VIH (2)	Ports 6, 7, D,PC2		2.7 to 3.6	0.3V _{DD} +0.7		V _{DD}	
	VIH (3)	RESB PC0, PC1, PC3, PC4		2.7 to 3.6	0.75V _{DD}		V _{DD}	
	VIH (4)	P22, P23, PA4, PA5, PB4, PB5 I2C side		2.7 to 3.6	0.7V _{DD}		V _{DD}	y
Low level input voltage	VIL (1)	When ports 1, 2, 3, 4, 5, A and port B, PnFSAn=0 Ports 0, 6, 7, D, PC2		2.7 to 3.6	V _{SS}	NE	0.2V _{DD}	
	VIL (2)	When ports 1, 2, 3, 4, 5, A and port B, PnFSAn=1		2.7 to 3.6	V _{SS}	emi	0.2V _{DD}	
	VIL (3)	CF1, RESB PC0, PC1,PC3, PC4		2.7 to 3.6	VSS	AN.	0.25V _{DD}	
	VIL (4)	P22, P23, PA4, PA5, PB4, PB5 12C side	NER.	2.7 to 3.6	VSS		0.3V _{DD}	
Instruction cycle time (Note 2-1)	tCYC		CONNET	2 7 to 3.6	0.098		66	μs
External system clock frequency	FEXCF (1)		 CF2 pin open System clock frequency division ratio = 1/1 External system clock D JTY50±5% 	2.7 to 3.6	0.1		10	MHz
EVI	CEP	EASEN	 CF2 pin open System clock frequency division ratio = 1/2 	2.7 to 3.6	0.2		20	
		between tCYC and o CF when the ratio is	scillation frequency is 1 1/2.	/FmCF wł	hen frequ	-	vision rat	

■ Allowable Operating Conditions at Ta=-40 to +85°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

Continued from preceding page.

Parameter	Symbol	Applicable Pin	Conditions			Specific	cation		
frequency range	Symoor	/Remarks	Conditions	$V_{DD}[V]$	min	typ	max	unit	
Oscillation frequency range (Note 2-2)	FmCF	PC3(CF1), PC4(CF2)	10 MHz ceramic oscillator mode See Fig. 1.	2.7 to 3.6		10		MIL	
	FmRC		Internal RC oscillation	2.7 to 3.6	0.5	1.0	2.0	MHz	
	FmSLRC		Internal low-speed RC oscillation	2.7 to 3.6	18	30	45		
	FsX'tal	XT1, XT2	32.768 kHz crystal oscillator mode See Fig. 2.	2.7 to 3.6		32.768		kHz	
	FmVCO(1)		VCO oscillator When setting FRQSEL=0 See Fig. 9.	2.7 to 3.6	12		28		
	FmVCO(2)		VCO oscillator When setting FRQSEL=1 See Fig. 9.	2.7 to 3.6	38		70	MHz	C
	FmVCO(5)		VCO oscillator	2.7 to 3.6		Note 2-3	NV		

Note 2-2 : See Tables 1 and 2 for oscillator constant values.

Note 2-3 : VCO oscillation frequency = Ceramic oscillator frequency × Setting point of SELREF

ed Exercise reserverses reserverse Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to significant the Recommended

■ Electrical Characteristics at Ta=-40 to +85°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

D	0 1 1	Applicable Pin				Specific	cation		
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
High level input current	IIH (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B,C, D RESB	Output disabled Pull-up resistor off VIN=VDD (including output Tr. off leakage current)	2.7 to 3.6			1		
Low level input current	IIL (1)	Ports 0, 1, 2 Ports 3, 4, 5 Ports 6, 7 Ports A, B, C, D RESB	Output disabled Pull-up resistor off VIN=VSS (including output Tr. off leakage current)	2.7 to 3.6	-1			μA	
High level output voltage	VOH (1)	Ports 0, 1, 2, 3 Ports 5, 6	IOH=-0.4mA	3.0 to 3.6	V _{DD} -0.4				1
	VOH (2)	Ports A, D, PC2 P40 to P45 PB2 to PB6	IOH=-0.2mA	2.7 to 3.6	V _{DD} -0.4			ES	G
		P46, P47	IOH=-1.6mA	3.0 to 3.6	V _D D-0.4		$\overline{\lambda} \overline{\lambda}$		
	VOH (4)	PB0, PB1	IOH=-1.0mA	2.7 to 3.6	VDD-0.4		1		
	VOH (5)	PC0, PC1,	IOH=-1.0mA	3.0 to 3.6	VDD-04	4r			
	VOH (6)	PC3, PC4,	IOH=-0.4mA	2.7 to 3.6	V _{DD} -0.4				
Low level output voltage	VOL (1)	Ports 0, 1, 3 , 4 Ports 5, 6, 7, D PC2	IOL=1.6mA	5.0 to 3.6	one	en	0.4	v	
	VOL (2)	P20 to P21, P24 to P27 PA0 to PA3 PA6 to PA7 PB0 to FB3, PB6	TOL=1.0mA	2.7 to 3.6	FOR	14.	0.4		
	VOL (3)	P22, P23,	10L=3.0r.A	3.0 to 3.6			0.4		
	VOL (4)	РА4, РА5 РВ4, ГВ5	IOI = 1.3mA	2.7 to 3.6			0.4		
	VOL (5)	PC0_PC1,	IOL=1 CmA	3.0 to 3.6			0.4		
	VOL (0)	PC3, PC4,	IOL=0.4mA	2.7 to 3.6			0.4		
Pull-up resistor	Кри (1)	Forts 0, 1, 2, 3 Ports 4, 5, 6, 7	voh=0.9V _{DD}	3.0 to 3.6	15	35	80	kΩ	
ENI	Rpu (2)	Ports A, B, D, PC2		2.7 to 3.6	15	35	100		
Hysteresis voltage	VHYS	RESB When ports 1, 2, 3, 4, A, B PnFSAn=1		2.7 to 3.6		0.1V _{DD}		V	
Pin capacitance	СР	All pins	Pins other than that under test VIN=VSS f=1 MHz Ta=25°C	2.7 to 3.6		10		pF	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

72

■ Serial I/O Characteristics at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$ Serial I/O Characteristics (Wakeup Function Disabled) (Note 4-1-1)

		Parameter	Symbol	Applicable	Conditions			Specif	ication	1
			Symbol	Pin/Remarks		V _{DD} [V]	min	typ	max	unit
Seri	Inpu	Period	tSCK (1)	SCK0 (P12)	• See Fig. 6.		4			
Serial clock	Input clock	Low level pulse width	tSCKL (1)				2			
^		High level	tSCKH(1)				2			
		pulse width	tSCKHA (1)		 Automatic communication mode See Fig. 6. 	2.7 to 3.6	6			
			tSCKHBSY		Automatic communication					tCYC
			(1a)		• See Fig. 6.		23			
			tSCKHBSY	•	• Mode other than automatic	-				
			(1b)		• See Fig. 6.		4			5
	Outpu	Period	tSCK (2)	SCK0 (P12)	• CMOS output selected • See Fig. 6.		4		ND	
	Output clock	Low level pulse width	tSCKL (2)					1/2		10.CV
		High level pulse width	tSCKH (2)				OK	1/2		tSCK
			tSCKHA (2)		Automatic communication mode CMOS output selected See Fig. 6.	2.7 to 3.6	ons	MA	(10)	
			tSCKHBSY (2a)		Automatic communication mode • CMOS output selected • See Fig. 6.		4		23	tCYC
		C	tSCKHBSY (25)	TR	Mode other than automatic communication mode • See Fig. 6.	K	4			
Serial	Da	ata setup time	tsDI (1)	SIC (P11), SB0 (P11)	Specified with respect to rising edge of SIOCLK		0.03			
input	Da	ata hold time	thDL(1)	ASL	• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Input clock	Output delay time	tcD0 (1)	SO0 (P10), SB0 (P11)	• (Note 4-1-2)				1tCYC +0.05	μs
	Output clock		tdDO (2)	+	• (Note 4-1-2)	2.7 to 3.6			1tCYC +0.05	

Note 4-1-1 : These specifications are theoretical values. Add margin depending on its use.

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Note 4-1-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

$\begin{array}{ c c c c c c c c c c c c c c c c c c c$		т	Parameter	Symbol	Applicable	Conditions			Speci	fication	
$\begin{array}{c c c c c c c c c c c c c c c c c c c $		ſ	rarameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Image width ISCKH (3) ISCKHBSY (3) 2.7 to 3.6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 </td <td>Seri</td> <td>Inpu</td> <td>Period</td> <td>tSCK (3)</td> <td>SCK0 (P12)</td> <td>• See Fig. 6.</td> <td></td> <td>2</td> <td></td> <td></td> <td></td>	Seri	Inpu	Period	tSCK (3)	SCK0 (P12)	• See Fig. 6.		2			
High level pulse width tSCKH (3) iSCKHBSY (3) tCY4 0 Data setup time tsD1 (2) istribution SI0 (P11), SB0 (P11) Specified with respect to rising edge of SIOCLK 'See Fig. 6. 0.03 0.03 0 Data hold time thD1 (2) SI0 (P10), SB0 (P11) 'Specified with respect to rising edge of SIOCLK 'See Fig. 6. 0.03 0.03 0.03 0 Data hold time thD1 (2) SO0 (P10), SB0 (P11) '(Note 4-2-2) 0.03 0.03 0.03 0 Dutput delay time tdD0 (3) SO0 (P10), SB0 (P11) '(Note 4-2-2) 0.03 0.03 0.05 Note 4-2-1 : These specifications are theoretical values. Add margin depc ding on its use. 0.05 0.05 0.05 Note 4-2-2 : Specified with respect to the falling edge of SIOCLIC Specified as the interval up to the time an output change begins in the open drain output node. See Fig. 6. 0.00	al clock	ıt clock		tSCKL (3)				1			
Image: Section of the section of th	~		High level	tSCKH (3)	-		2.7 to 3.6	1			tCYO
Image: Determine Image: Determine SB0 (P11) rising edge of SIOCLK 0.03 0.03 Image: Determine thDI (2) SB0 (P11) 'See Fig. 6. 2.7 to 3.6 0.03 1000 Image: Determine thDI (2) SB0 (P11) 'Note 4-2-2) 2.7 to 3.6 0.03 11CYC Note 4-2-1 : These specifications are theoretical values. Add margin depending on its use. Note 4-2-2 : Specified with respect to the falling edge of SIOCLK Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.			pulse width		-			2			
Serial Output delay ime tdD0 (3) SO0 (P10), SB0 (P11) * (Note 4-2-2) 2.7 to 2.6 1tCYC +0.05 Note 4-2-1 : These specifications are theoretical values. Add margin depending on its use. Note 4-2-2 : Specified with respect to the falling edge of SIO CLC Specified as the interval up to the time an output change begins in the open drain on put mode. See Fig. 6.	Serial	Da	ta setup time	tsDI (2)		rising edge of SIOCLK		0.03			
Image of time IdD0 (3) S00 (P10), S00 (P10), S00 (P10) Prove 4-2-2) 2.7 to 3.6 IntCVC +0.05 Note 4-2-1 : These specifications are theoretical values. Add margin depending on its use. Note 4-2-2 : Specified with respect to the falling edge of SIO CLC Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.	input	Da	ta hold time	thDI (2)		• See Fig. 6.	2.7 to 3.6	0.03			
Note 4-2-1 : These specifications are theoretical values. Add margin depending on its use Note 4-2-2 : Specified with respect to the falling edge of SIOCLE. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.	Seria	Inpu		tdD0 (3)		• (Note 4-2-2)					цs
Note 4-2-1 : These specifications are theoretical values. Add margin depending on its use Note 4-2-2 : Specified with respect to the falling edge of SIOCLE. Specified as the interval up to the time an output change begins in the open drain on put mode. See Fig. 6.	ıl output	t clock	ume		SB0 (P11)		2.7 to 3.6				
			S.	C	OTR	ECONTACT CONTACTO	OR IN				

SIO0 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-2-1)

SIO1 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-3-1)

	-	-		、 <u>·</u>						1
	Parameter	Symbol	Applicable	Conditions	r		Specif	ication	r	-
		Symoor	Pin/Remarks		V _{DD} [V]	min	typ	max	unit	
Inp	Period	tSCK (4)	SCK1 (P45)	• See Fig. 6.		4				
Input clock Serial clock	Low level	tSCKL (4)				2				
lock	pulse width					2				
	High level	tSCKH (4)				2				
	pulse width	tSCKHA (4)		Automatic communication						
				mode	271 26	6				
			_	• See Fig. 6.	2.7 to 3.6				tCYC	
		tSCKHBSY		• Automatic communication					ic re	
		(4a)		mode		23				
		tSCKHBSY	-	See Fig. 6. Mode other than automatic						
		(4b)		communication mode		4				
		(10)		• See Fig. 6.		4				C
0	Period	tSCK (5)	SCK1 (P45)	· CMOS output selected					20	
utpu				• See Fig. 6.		4				
Output clock	Low level	tSCKL (5)					1/2	N		
ck	I		_				1.2		tSCK	
	High level	tSCKH (5)				2	1/2		iber	
	pulse width		-							
		tSCKHA (5)		Automatic communication mode			0			
				CMOS output selected	2.7 to 3.6	6 9		$\langle \vee \rangle$		
				• See Fig. 6.	2.7 10 5.0	01	NP.			
		tSCKHBSY		• Automatic communication		2	74			
		(5a)		mode	\mathcal{O}	-0			tCYC	
				• CMOS output selected	$\langle A, \rangle$	4		23		
				• See Fig. 6.	2					
		tSCKHBSY		• Mode other than automatic						
		(5 b)	$ \times \forall$	communication mode	Í	4				
	Data sa tima	t D [(2)	SI (B44)							
ieria	oata setup tille	(5)				0.03				
	Data hold time	thDI(3)			2.7 to 3.6		1			
Ē			22		2.7 to 5.0	0.03				
		Y AV	I.CV							
Inp	J Output delay	tdD0 (4)	SO1 (P43),	• (Note 4-3-2)						
ial o	₹ time		SB1 (P44)					1tCYC		
lock	lock	24							μs	
Ħ		V .								
	_	tdDO (5)	+	\cdot (Note 4_{-3} -2)	2.7 to 3.6					
Jutp	Jufp	(J)		(11010 7-3-2)						
ut cl	If cl							1tCYC		
	2		1	1	1	1		+0.05	l I	1
	Dutput delay	FOLE	SII (P44), SB1 (P44) SOI (P43), SB1 (P44)	See Fig. 6. Specified with respect to risins edge of SIOCLK See Fig. 6. (Note 4-3-2) (Note 4-3-2)	2.7 to 3.6	0.03			μs	

Note 4-3-1 : These specifications are theoretical values. Add margin depending on its use.

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Note 4-3-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.

Note 4-1:1 These specifications are theoretical values. Add margin dequired as the threeval up to the time an output change begins in the open drain output mode. See Fig. 6.		I	Parameter	Symbol	Applicable	Conditions			Specif	ication	
$\frac{1}{100} \frac{1}{100} \frac{1}$		1	diameter	byinoor	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
n High level pulse width High level High le	Ser	Inp	Period	tSCK (6)	SCK1 (P45)	• See Fig. 6.		2			
n High level pulse width High level High le	ial cl	ut cle	Low level	tSCKL (6)	-						
Image room Image room <td>ock</td> <td>ock</td> <td>pulse width</td> <td></td> <td></td> <td></td> <td></td> <td>1</td> <td></td> <td></td> <td></td>	ock	ock	pulse width					1			
Image: Section of the section of th			e	tSCKH (6)			2.7 to 3.6	1			tCYC
induction			pulse width	tSCKHBSY	1						
Image: Data hold time thDI (4) SB1 (P44) rising edge of SIOCLK 0.03 0.03 0.03 Image: See Fig. 6. 2.7 to 3.6 0.03 0.03 0.03 0.03 0.03 See Fig. 6. 2.7 to 3.6 0.03 0.03 0.03 0.03 0.03 0.03 See Fig. 6. SO1 (P43), * (Note 4.4-2) * (Note 4.4-2) 2.7 to 3.6 0.03 100 (f) 0.05 Note 4-4-1 : These specifications are theoretical values. Add margin depending on its use. Note 4-4-2 : Specified with respect to the falling edge of SIC CLY. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.				(6)				2			
Image: Sensitive of the sensite of the sensitive of the sensitive of the sensitive of the sens	Serial	Da	ta setup time	tsDI (4)				0.03			
Image of the product delay induction in the product of the produc	input	Da	ta hold time	thDI (4)		• See Fig. 6.	2.7 to 3.6	0.03			
Image: Second state in the image is the	Serial	Input o		tdD0 (6)		• (Note 4-4-2)					μs
Note 4-4-1 : These specifications are theoretical values. Add margin depending on its use; Note 4-4-2 : Specified with respect to the falling edge of SIGCEY. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.	output	clock					2.7 to 3.6			1	
							DER	0	NP		

	т	Doromotor	Qumbal	Applicable	Conditions			Specif	ication	
	ŀ	Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Ser	Inp	Period	tSCK (7)	SCK4 (PA2)	• See Fig. 6.		4			
Serial clock	Input clock	Low level	tSCKL (7)				2			
lock	ock	pulse width		_			2			
		High level	tSCKH (7)				2			
		pulse width	tSCKHA (7)		Automatic communication					
					mode	2.7 to 3.6	6			
			CONTROL		• See Fig. 6.	2.7 10 3.0				tCYC
			tSCKHBSY		Automatic communication		22			lere
			(7a)		mode • See Fig. 6.		23			
			tSCKHBSY	-	• Mode other than automatic					
			(7b)		communication mode		4			
					• See Fig. 6.					S
	Ou	Period	tSCK (8)	SCK4 (PA2)	• CMOS output selected					K
	Output clock			4	• See Fig. 6.				NV	
	cloc	Low level	tSCKL (8)					1/2		
	k	pulse width High level	+SCVII (9)					h_{h}		tSCK
		pulse width	tSCKH (8)					1/2		
		pulse what	tSCKHA (8)		Automatic communication					
					mode	\sim	S		k (U)	~
					• CMOS output selected	2.7 to 3.6	0	NP		
					See Fig. 6.	R		Q''		
			tSCKHBSY		• Automatic communication	D.	- 05			
			(8a)		mode • CMOS output selected		4		23	tCYC
					• See Fig. 6.	0				
			tSCKHBSY		• Mode other than automatic	5				
			(8b)	1	communication mode		4			
				h	• See Fig. 6.					
Se	Da	ta setup time	tsDI (5)	S14 (PA1),	· Specified with respect to		0.03			
ial ir			5	S54 (FA!)	rising edge of SIOCLK		0.05			
iput	Da	ta hold time	thDi (5)	12 1	• See Fig. 6.	2.7 to 3.6	0.02			
			1 ol	1,SV	*		0.03			
S	H	Output delay	tdD0 (7)	SC4 (PA0),	• (Note 4-5-2)					
Serial cutput	Input clock	lime		SB14(PA1)					1. OVG	
outp	cloc		24						1tCYC	μs
ut	×		X -						+0.05	
		-		-		2.7 to 3.6				
	Output clock		tdDO (8)		• (Note 4-5-2)					
	yut c								1tCYC	
	lock								+0.05	
	1									

SIO4 Serial Input/Output Characteristics (Wakeup Function Disabled) (Note 4-5-1)

 $\langle \gamma \rangle$

 Note 4-5-1 : These specifications are theoretical values. Add margin depending on its use.

 Note 4-5-2 : Specified with respect to the falling edge of SIOCLK. Specified as the interval up to the time an

 output change begins in the open drain output mode. See Fig. 6.

SIO4 Serial Input/Output Characteristics (Wakeup Function Enabled) (Note 4-6-1)

$\frac{\left \begin{array}{c} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\$		I	Parameter	Symbol	Applicable	Conditions	r		Specif	ication	
Image: Decemption of the last of th		-		Symoor	Pin/Remarks		V _{DD} [V]	min	typ	max	unit
A High level pulse width tSCKH (9) tSCKHBSY (9) 2.7 to 3.6 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Seri	Inpu	Period	tSCK (9)	SCK4 (P45)	• See Fig. 6.		2			
Image: High level pulse width ISCKH (9) pulse width ISCKHBSY (9) Data setup time IsD1 (6) SB4 (P44) · Specified with respect to rising edge of SIOCLK 2.7 to 3.6 0.03 Image: Data setup time IsD1 (6) SB4 (P44) · Specified with respect to rising edge of SIOCLK 2.7 to 3.6 0.03 Image: Data hold time thDI (6) SB4 (P44) · See Fig. 6. Vent of the second setup time thDD (9) SO4 (P43), setup time · (Note 4-6-2) Image: Data hold time thDD (9) SO4 (P43), setup time · (Note 4-6-2) Image: Data hold time thDD (9) SO4 (P43), setup time · (Note 4-6-2) Image: Data hold time thDD (9) SO4 (P43), setup time · (Note 4-6-2) Image: Data hold time thDD (9) Note 4-6-1 : These specifications are theoretical values. Add marge: Data hold me on its use: Note 4-6-2 : Specified with respect to the falling edge of SIOCLK Specified with respect to the falling edge of SIOCLK Specified as the interval up to the time an output change begins in the open drain output model. Sec Fig. 6.	al clock	ıt clock		tSCKL (9)				1			
Image: Secting of the setup time tsD1 (6) S14 (P44), SBecified with respect to rising edge of SIOCLK 0.03 0.03 Image: Data setup time tsD1 (6) S14 (P44), SB4 (P44) * Specified with respect to rising edge of SIOCLK 0.03 0.03 0.03 Image: Data hold time thD1 (6) S04 (P43), * (Note 4-6-2) 0.03 0.03 0.03 0.03 Verified output delay tdD0 (9) SO4 (P43), * (Note 4-6-2) 2.7 to 7.6 0.03 0.05 0.05 Note 4-6-1 : These specifications are theoretical values. Add marg.u depending. on its use: Note 4-6-2 : Specified with respect to the falling edge of SIOCD*. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.			-	tSCKH (9)			2.7 to 3.6	1			tCYC
Image:			pulse width		-			2			
Image: Sensitive of the sensite of the sensitive of the sensitive of the sensitive of the sens	Serial	Da	ta setup time	tsDI (6)				0.03			
Image of product delay (abb (9)) S04 (P43), SB4(P44) P(Note 4-6-2) 2.7 to 3.6 P(CYC 40.02) Note 4-6-1 : These specifications are theoretical values. Add margin depending on its use. Note 4-6-2 : Specified with respect to the falling edge of SIC CDK. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.	input	Da	ta hold time	thDI (6)		• See Fig. 6.	2.7 to 3.6	0.03			
Note 4-6-1 : These specifications are theoretical values. Add margin depending on its use: Note 4-6-2 : Specified with respect to the falling edge of SIOCHY. Specified as the interval up to the time an output change begins in the open drain output mode. See Fig. 6.	Serial output	Input clock			SB4(P44)					+0.05	ES
				C	0	ONIMEN	OUN	FOR	1.		

	I	Parameter	Symbol	Applicable	Conditions			Specif	ication	I
	1	arameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (10)	SM0CK (P22)	See Fig. 6.		4			
clock	lock	Low level pulse width	tSCKL (10)			2.7 to 3.6	2			~~~~
		High level pulse width	tSCKH (10)				2			tCYC
	Outpu	Period	tSCK (11)	SM0CK (P22)	CMOS output selected See Fig. 6.		4			
	Output clock	Low level pulse width	tSCKL (11)			2.7 to 3.6		1/2		
		High level pulse width	tSCKH (11)					1/2		tSCK
Serial input	Da	ta setup time	tsDI (7)	SM0DA (P23),	• Specified with respect to rising edge of SIOCLK		0.03			C.
input	Da	ta hold time	thDI (7)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Ou	tput delay time	tdD0 (10)	SM0DO (P24), SM0DA	 Specified with respect to falling edge of SIOCLK Specified as interval up to 			NF	1tCYC	μs
put				(P23)	time when output state starts changing. • See Fig. 6.	2.7 to 3.6		en	+0.05	1
				\mathbf{O}	ECONTACT CONTACT CONTACT CONTACT CONTACT	OUR	FOP			

SMIIC0 Simple SIO Mode Input/Output Characteristics (Note 4-7-1)

SMIIC0 I²C Mode Input/Output Characteristics (Note 4-8-1) (Note 4-8-2) (Note 4-8-4)

	Р	arameter		Symbol	Applicable	Conditions	[Specif	ication	r
				Symeet	Pin/Remarks		V _{DD} [V]	min	typ	max	unit
Clock	Input clock	Period		tSCL	SM0CK (P22)	• See Fig. 8.		5			
	lock	Low level pulse widt		tSCLL			2.7 to 3.6	2.5			TCh
		High level pulse widt		tSCLH				2			Tfilt
	Output clock	Period		tSCLx	SM0CK (P22)	• Specified as interval up to time when output state starts		10			
	t clock	Low level pulse widt		tSCLLx		changing.	2.7 to 3.6		1/2		
		High level pulse widt		tSCLHx					1/2		tSCL
pin	ns inp	K and SM0I put spike ssion time	DA	tsp	SM0CK (P22) SM0DA (P23)	• See Fig. 8.	2.7 to 3.6			1	Tfin
			Input	tBUF	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		2.5	NF		Tfilt
	twee	ease time n start and	0	tBUFx	SM0CK (P22) SM0DA (P23)	Standard clock mode Specified as interval up to time when output state stars changing.	2.7 to 3.6	5.5	en		1
	Ψ		Output			High-speed clock mode Specified as interval up to time when output state starts	OUR	1.6	MP		μs
				tHD;STA	SM0CK (P22) SM0DA (P23)	changing. • When SMIIC register control bit. 12CSHDS=0 • See Fig. 8.	RA	2.0			
	art/re		nput	515	ASE	• When SMIC register control bi, 12CSI (DS=1 • See Fig. 8.		2.5			Tfilt
tin	ne	on nold		tHD;STAx	SM0CK (Р22) SM0DA (Р23)	Standard clock mode Specified as interval up to time when output state starts changing.	2.7 to 3.6	4.1			
			Output	RL		High-speed clock mode Specified as interval up to time when output state starts changing.		1.0			μs
			Input	tSU;STA	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		1.0			Tfilt
	start up ti	condition me	Output	tSU;STAx	SM0CK (P22) SM0DA (P23)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	5.5			μs
			put			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.6			μο

D (0 1 1	Applicable				Specific	ation		
Parameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Min	typ	max	Unit	
	Input	tSU;STO	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		1.0			Tfilt	
Stop condition setup time	Ou	tSU;STOx	SM0CK (P22) SM0DA (P23)	Standard clock mode Specified as interval up to time when output state starts changing.	2.7 to 3.6	4.9				
	Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.1			μs	
	Input	tHD;DAT	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		0				
Data hold time	Output	tHD;DATx	SM0CK (P22) SM0DA (P23)	• Specified as interval up to time when output state starts changing.	2.7 to 3.6	1		1.5	Tfilt	G
	Input	tSU;DAT	SM0CK (P22) SM0DA (P23)	• See Fig. 8.		1	NE	Ŋ		
Data setup time	Output	tSU;DATx	SM0CK (P22) SM0DA (P23)	• Specified as interval up to time when output state starts changing.	2.7 to 3.6	l†SCL- 1.5Tfilt	emi	,01	Tfilt	
	Input	tF	SM0CK (P22) SM0DA (P23)	• See Fig. 8.	2.7 to 3 6	ons	MA	300		
SM0CK and SM0DA pins fall time	Outp	tF	8 MOCK (P22) S MODA (P23)	 hen SMIIC register controi bits PSLW=1, P5V=1 	3	20+0.1Cb (Note 4-8-3)		250	ns	
	put		JP.	 SM0CK, SM0DA port output F. ST mode Cb ≤ 100pF 	3.0 to 3.6			100		

Note 4-8-1 These specifications are theoretical values. Add margin depending on its use. Note 4-8-2 The value of Tfilt is determined by the values of the register SMIC0BRG, bits 7 and 6 (BRP1, BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
	0	tCYC×1
0	1	tCYC×2
	0	tCYC×3
1	1	tCYC×4

THISDEVI Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range : $250 \text{ ns} \ge \text{Tfilt} > 140 \text{ ns}$

Note 4-8-3: Cb represents the total loads (in pF) connected to the bus pins. $Cb \le 100 \text{ pF}$

Note 4-8-4: The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows : ns

$$250 \text{ ns} \ge \text{Tfilt} > 140$$

BRDQ (bit5) =
$$1$$

SCL frequency setting $\leq 100 \text{ kHz}$

The high-speed clock mode refers to a mode that is entered by configuring SMIC0BRG as follows : $250 \text{ ns} \ge \text{Tfilt} > 140 \text{ ns}$

BRDQ (bit5) = 0

SCL frequency setting $\leq 400 \text{ kHz}$

	I	Parameter	Symbol	Applicable	Conditions	r		Specif	ication	T
	1	arameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
Serial clock	Input clock	Period	tSCK (12)	SM0CK (PB4)	See Fig. 6.		4			
clock	lock	Low level pulse width	tSCKL (12)			2.7 to 3.6	2			
		High level pulse width	tSCKH (12)				2			tCYC
	Outpu	Period	tSCK (13)	SM0CK (PB4)	CMOS output selected See Fig. 6.		4			
	Output clock	Low level pulse width	tSCKL (13)			2.7 to 3.6		1/2		
		High level pulse width	tSCKH (13)					1/2		tSCK
Serial input	Da	ta setup time	tsDI (8)	SM0DA (PB5),	• Specified with respect to rising edge of SIOCLK		0.03			CC.
input	Da	ta hold time	thDI (8)		• See Fig. 6.	2.7 to 3.6	0.03			
Serial output	Ou	tput delay time	tdD0 (12)	SM0DO (PB6),	• Specified with respect to falling edge of SIOCLK			NF		μs
output				SM0DA (PB5)	• Specified as interval up to time when output state starts	2.7 to 3.6	FOR		1tCYC +0.05	4
					changing. • See Fig. 6.	20	1	6	<u> </u>	
					ECONINER	OUK	FOR	14.		

SMIIC1 Simple SIO Mode Input/Output Characteristics (Note 4-9-1)

SMIIC1 I²C Mode Input/Output Characteristics (Note 4-10-1) (Note 4-10-2) (Note 4-10-4)

<u> </u>				• 	•	`	, (,,		,	
	Р	arameter		Symbol	Applicable	Conditions			Specif	fication	1
	1	arameter		Symoor	Pin/Remarks	Conditions	$V_{DD}[V]$	Min	typ	max	unit
Clo	Inp	Period		tSCL	SM1CK	• See Fig. 8.		5			
Clock	Input clock				(PB4)			5			
	lock	Low level		tSCLL			2.7 to 3.6	2.5			
		pulse widt					2.7 10 5.0	2.0			Tfilt
		High level		tSCLH				2			
	0	pulse widt Period	n	tSCLx	SM1CK	Specified as interval up to					
)utpi	1 chou		IJCLX	(PB4)	time when output state starts		10			
	Output clock	Low level		tSCLLx	()	changing.				1	
	ock	pulse widt	h				2.7 to 3.6		1/2		
		High level	l	tSCLHx					1/2		tSCL
_		pulse widt	h								
		K and SM0I	DA	tsp	SM1CK (PB4)	• See Fig. 8.					C
		out spike			SM1DA (PB5)		2.7 to 3.6			1	Tfilt
su	ppres	sion time	r	ļ							
			Input	tBUF	SM1CK (PB4)	• See Fig. 8.				N	m.e.t.
1			Jut		SM1DA (PB5)			2.5	N		Tfilt
			F	tBUFx	SM1CK (PB4)	Standard clock mode		2			
Вι	ıs rel	ease time			SM1DA (PB5)	• Specified as interval up to		20`		7-1	Δ
be	twee	n start and				time when output state starts	2.7 to 3.6	5.5	6,	~\O`	
sto	ор		Output			changing.	EV		2		µsec
			out			High-speed clock mode Specified as interval up to	V. 0	0.	Nr		•
						time when output state starts		1.6			
						changing	O,	60°			
				tHD;STA	SMICK (PB4)	When SMIIC register	7/				
					SMIDA (PB5)			2.0			
					1,2	J2CSHDS=0	D .	2.0			
			Input		\sim	• See Fig. ² . When SMIIC registor					Tfilt
			Ē			control oit					
				5,51	CV.	I2CSI4DS=1		2.5			
	art/re	start on hold				• See Fig. 8.	274.26				
			Ū	tHD;STAx	SM1CK (PE+)	· Standard clock mode	2.7 to 3.6				
		21			SM1DA (PB5)	• Specified as interval up to		4.1			
	<		С	.0	Kr	time when output state starts changing.					
C	`	EVI	Output	SET		High-speed clock mode	1				μsec
	-		It	\sim		• Specified as interval up to					
						time when output state starts		1.0			
				ļ		changing.					
1			Input	tSU;STA	SM1CK (PB4)	• See Fig. 8.		1.0			Tfilt
1			out		SM1DA (PB5)		ļ	1.0			11111
			_	tSU;STAx	SM1CK (PB4)	Standard clock mode					
n	1	414°			SM1DA (PB5)	• Specified as interval up to		5.5			
	estart tup ti	condition me				time when output state starts	2.7 to 3.6	5.5			
50	արս	une	Output			changing.	ļ				μsec
			ut			High-speed clock mode					
						 Specified as interval up to 	1	1		1	1
						time when output state starts		1.6			

D			Applicable			S	pecificat	tion		
Parameter		Symbol	Pin/Remarks	Conditions	$V_{DD}[V]$	Min	typ	max	unit	
	Input	tSU;STO	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		1.0			Tfilt	
Stop condition setup time	Ou	tSU;STOx	SM1CK (PB4) SM1DA (PB5)	 Standard clock mode Specified as interval up to time when output state starts changing. 	2.7 to 3.6	4.9				
	Output			 High-speed clock mode Specified as interval up to time when output state starts changing. 		1.1			μsec	
	Input	tHD;DAT	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.		0				~~~
Data hold time	Output	tHD;DATx	SM1CK (PB4) SM1DA (PB5)	• Specified as interval up to time when output state starts changing.	2.7 to 3.6	I		1.5	Tfilt	G
	Input	tSU;DAT	SM1CK (PB4) SM1DA (PB5)	• See Fig. 8.			JEV			
Data setup time	Output	tSU;DATx	SM1CK (PB4) SM1DA (PB5)	Specified as interval up to time when output state starts changing.	2.7 to 3.6	1:SCL-1.5Tfilt	mi	0	Tfilt	
	Input	tF	SM1CK (PB4) SM1DA (PE5)	• See Fig. 8.	2.7 to 3 6	ons	NA	300		
SM0CK and SM0DA pins fall time	Outp	tF	8M1CK (PB4) SM1DA (PB5)	 hen SMIIC register controi bits PSLW=1, PHV=1 	R ³	20+0.1Cb (Note 4-10-3)		250	ns	
	put		JP.	SM0CK, SM0DA port output F. ST mode Cb ≤ 100pF	3 to 3.6			100		

Note 4-10-1 : These specifications are theoretical values. Add margin depending on its use. Note 4-10-2 The value of Tfilt is determined by the values of the register SMIC1BRG, bits 7 and 6 (BRP1, BR^P0) and the system clock frequency.

	BRP1	BRP0	Tfilt
X	0	0	tCYC×1
	0	1	tCYC×2
2	1	0	tCYC×3
	1	1	tCYC×4

THIS DEVI Set bits (BPR1, BPR0) so that the value of Tfilt falls between the following range : $250 \text{ ns} \ge \text{Tfilt} > 140 \text{ ns}$

Note 4-10-3 : Cb represents the total loads (in pF) connected to the bus pins. $Cb \le 100 \text{ pF}$

Note 4-10-4 : The standard clock mode refers to a mode that is entered by configuring SMIC0BRG as follows :

> $250 \text{ ns} \ge \text{Tfilt} > 140 \text{ ns}$ BRDQ (bit5) = 1

SCL frequency setting $\leq 100 \text{ kHz}$

The high-speed clock mode refers to a mode that is entered by configuring SMIC1BRG as follows :

 $250 \text{ ns} \ge T \text{filt} > 140 \text{ ns}$

BRDQ (bit5) = 0

SCL frequency setting $\leq 400 \text{ kHz}$

$\begin{array}{c c c c c c c c c c c c c c c c c c c $		р	arameter	Symbol	Applicable	Conditions			Specifi	cation	1
Image: Construction of the second		1	arameter	Symbol	Pin/Remarks	Conditions	$V_{DD}[V]$	min	typ	max	unit
pulse width High level pulse width tSCKH (13) pulse width SLODA (PA5), Specified with respect to rising edge of SIOCLK See Fig. 6. 0.03 0.03 0 utput delay time tdD0 (13) SLODA (PA5), Specified with respect to rising edge of SIOCLK See Fig. 6. 2.7 to 3.6 0.03 0.03 0.03 0.03 0 utput delay time tdD0 (13) SLODA (PA5), Specified with respect to falling edge of SIOCLK (PA5) Specified as interval up to time when output state starts changing. 2.7 to 3.6 0.03 0.03 0.05 Note 4-11-1 : These specifications are theoretical values. Add margin dependent on its use.	Serial	Input	Period	tSCK (13)		See Fig. 6.		4			
High level pulse width tSCKH (13) 2 1 0 Data setup time tsDI (9) SLODA (PA5), (PA5), See Fig. 6. Specified with respect to rising edge of SIOCLK 0.03 1 0 Data hold time thDI (9) SLODO (PA6), SLODA (PA5), See Fig. 6. Specified with respect to falling edge of SIOCLK 2.7 to 3.6 0.03 1 0 Output delay time tdD0 (13) SLODO (PA6), SLODA (PA5) Specified as interval up to time when output state starts changing. 2.7 to 3.6 11CYC (0.05) 0 SLODA (PA5) See Fig. 6. 11CYC (0.05) 1000 1000 Note 4-11-1 : These specifications are theoretical values. Add margin depending on us use. See Fig. 6. 1000 1000	clock	clock		tSCKL (13)			2.7 to 3.6	2			tCYC
bata setup time tsDI (9) SL0DA (PA5), · Specified with respect to rising edge of SIOCLK · See Fig. 6. 2.7 to 3.6 0.03 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 <t< td=""><td></td><td></td><td>High level</td><td>tSCKH (13)</td><td></td><td></td><td></td><td>2</td><td></td><td></td><td></td></t<>			High level	tSCKH (13)				2			
Serie Output delay time tdD0 (13) SL0DO · Specified with respect to falling edge of SIOCLK · Specified as interval up to · Specified as interval up to · Specified as interval up to · CYC 0.05 · PA5) · Specified as interval up to · Specified as interval up to · CYC 0.05 · CYC · Note 4-11-1 : These specifications are theoretical values. Add margin dependence on its use. · See Fig. 6. · Output on its use.	Seria	Dat		tsDI (9)				0.03			
Image: State of the second state state of the second state	input	Dat	a hold time	thDI (9)	(- //		2.7 to 3.6	0.03			-
Changing. • See Fig. 6. Note 4-11-1 : These specifications are theoretical values. Add margin depending on its use.	Serial outpu	Out	put delay time	tdD0 (13)	(PA6), SL0DA	falling edge of SIOCLK Specified as interval up to 	2.7 to 3.6				μs
Note 4-11-1 : These specifications are theoretical values. Add margin depending on its use.	ut				(PA5)	changing.	2.7 10 5.0			+0.05	
CONNERVOLR ORMATION	Ļ		4 1 1 1 771	· ~	· 1			<u> </u>		\overline{H}	
						NMER	OUK	FOF	5/14.		

SLIIC0 Simple SIO Mode Input/Output Characteristics (Note 4-11-1)

D. (0.1.1	Applicable				Specifi	ication		
Parameter		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Min	typ	max	unit	
Clock Period Low level		tSCL	SLOCK (PA4)	• See Fig. 8.		5				
Low level	1	tSCLL			2.7 to 3.6	2.5			Tfilt	
High level pulse width		tSCLH				2				
SLOCK and SLODA pins input spike suppression time	L	tsp	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6			1	Tfilt	
Bus release time between start and stop	Input	tBUF	SLOCK (PA4) SLODA (PA5)	• See Fig. 8.	2.7 to 3.6	2.5			Tfilt	Ċ
Start/restart	I.	tHD;STA	SLOCK (PA4) SLODA (PA5)	 When SMIIC register control bit, I2CSHDS=0 See Fig. 8. 		2.0		NC	ES	
condition hold time	Input			• When SMIIC register control bit I2CSHDS=1 • See Fig. 8	2.7 to 3.6	25	NE		Tfilt	
Restart condition setup time	Input	tSU;STA	SLOCK (PA4) SLODA (PA5)	• See Lig. 8.	2. (te 3.6	50	Ser	ζlΘ,	Tfilt	
Stop condition setup time	Inpu	tSU;STO	SLOCK (PA4) SLODA (PA5)	See Fig. 8.	27 to 3.6	1.0			Tfilt	
		5	OTR	CONTREEL						
	Input	tHD;DAT	SLOCK (F 44) SI 0DA (PA5)	• See Fig. 8.		0				
Data hold time	Output	tHD;DA Fx	SLOCK (PA4) SLODA (PA5)	Specified as interval up to time when output state starts changing.	2.7 to 3.6	1		1.5	Tfilt	
	Input	ISU DAT	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.		1				
Data setup time	Output	tSU;DATx	SLOCK (PA4) SLODA (PA5)	• Specified as interval up to time when output state starts changing.	2.7 to 3.6	1tSCL- 1.5Tfilt			Tfilt	

74

Parameter		6 1 1	Applicable			S			
		Symbol	Pin/Remarks	Conditions	V _{DD} [V]	Min	typ	max	Unit
	Input	tF	SL0CK (PA4) SL0DA (PA5)	• See Fig. 8.	2.7 to 3.6			300	
SL0CK and SL0DA pins fall time	Output	tF	SLOCK (PA4) SLODA (PA5)	• When SLIIC0 register control bits PSLW=1, PHV=1	3	20+0.1Cb (Note 4-12-3)		250	ns
	put			 SL0CK, SL0DA port output FAST mode Cb ≤ 100pF 	3.0 to 3.6			100	

Note 4-12-1 : These specifications are theoretical values. Add margin depending on its use.

Note 4-12-2 : The value of Tfilt is determined by the values of the register SLICOPCNT, bits 5 and 4 (BRP1, NDESIGN BRP0) and the system clock frequency.

BRP1	BRP0	Tfilt
0	0	tCYC×1
0	1	tCYC×2
1	0	tCYC×3
1	1	tCYC×4

wing range: .spins. 65 \$100 pF

UART0 Operati	ng Conditi	ions at Ta=-	$-40 \text{ to } +85^{\circ}\text{C},$	V _{SS} 1=V _{SS} 2=V	SS3=VSS4=0V

Deremeter	Symbol	Applicable Pin/Remarks	Conditions		Specification				
Parameter	Symbol		Conditions	V _{DD} [V]	min	typ	max	unit	
Transfer rate	UBR0	U0RX (P13), U0TX (P14), U0BRG (P07)		2.7 to 3.6	4		8	tBGCYC	

Note 4-9 : tBGCYC denotes one cycle of the baudrate clock source.

UART2 Operating Conditions at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V$

Parameter	Symbol	Applicable	Conditions			Spec	ification		
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
Transfer rate	UBR2	U2RX (P16), U2TX (P17),		2.7 to 3.6	8		4096	tBGCYC	GM

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Note 4-10: tBGCYC denotes one cycle of the baudrate clock source.

UART3 Operating Conditions at Ta=-40 to +85°C, $V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0$ V

Parameter	Symbol	Applicable Pin/Remarks	Conditions V _{DD} [V] min typ	afication max	unit
Transfer rate	UBR3	U3RX (P34) U3TX (P35),	2.7 00 3 6 8. 0 2.1	4096	tBGCYC

Note 4-10 : tBGCYC denotes one cycle of the baudrate clock source.

■ Pulse i. put Conclusions at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V

	Parameter	Symbol	Applicable Pin/Remarks	Conditions		Specification			
					V _{DD} [V]	min	typ	max	unit
TH	High low level pulse width	фэн (1) tPIL (1)	NT0 (P30) INT1 (P21) INT2 (P32), INT3 (P33), INT4 (P20), INT5 (P21), INT6 (P40), INT7 (P41)	 Interrupt source flag can be set. Event inputs for timers 2 and 3 are enabled. 	2.7 to 3.6	2			tCYC
		tPIL (2)	RESB	Resetting is enabled.	2.7 to 3.6	10			μs

■ AD Converter Characteristics at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V 12-bit AD Conversion Mode

Demonstern	Parameter Symbol Applic		Conditions		Specification					
Parameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit		
Resolution	NAD	AN0 (P60) to AN7 (P67),		2.7 to 3.6		12		bit		
Absolute accuracy	ETAD	AN8 (P70)	(Note 6-1)	2.7 to 3.6			±16	LSB		
Conversion time	TCAD12	to AN15 (P77)	Conversion time calculated	3.0 to 3.6	64		115			
				2.7 to 3.6	128		230	μs		
Analog input voltage range	VAIN			2.7 to 3.6	V _{SS}		V _{DD}	V		
Analog port input current	IAINH		VAIN=V _{DD}	2.7 to 3.6			1			
input current	IAINL		VAIN=V _{SS}	2.7 to 3.6	-1			μΑ		

- Conversion time calculation formula : TCAD12 = $\left(\frac{52}{\text{AD division ratio}} + 2\right) \times \text{tCYC}$

8-bit AD Conversion Mode

- Conversion tim	ie calcula	tion formula :	$1CAD12 = \left(\frac{D2}{AD \text{ division ratio}}\right)$	$+2) \times tC YC$				-1-
B-bit AD Conve	ersion N	lode					, G/	3
Parameter	Symbol	Applicable Pin	Conditions		Specif	ication		
Farameter	Symbol	/Remarks	Conditions	V _{DD} [V]	min typ	max	unit	
Resolution	NAD	AN0 (P60) to AN7 (P67),		2.7 to 3.6	8		bit	
Absolute accuracy	ETAD	AN8 (P70)	(Note 6-1)	2.7 to 3.6		±1.5	LSB	
Conversion time	TCAD8	to AN15 (P77)	Conversion time calculated	3.0 to 3.6 2.7 to 3.6	<u>39</u> 79	71 140	μs	
Analog input voltage range	VAIN			2.7 to 3.6	V _{SS}	V _{DD}	V	
Analog port input current	IAINH		VAIN=VDD	2.7 to 3.6	0.	1		
input current	IAINL		VAIN=VSS	2.7 to 3.6	-b		μΑ	

- Conversion time calculation formula : $TCAD8 = (\frac{52}{AD \text{ division ratio}} + 2) \times tCYC$

Note 6-1 : The quantization error ($\pm 1/2$ LSB) is excluded from the absolute accuracy.

Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.

The conversion time is twice the normal value when one of the following conditions occurs:

- The first AD conversion is executed in the 12-bit AD conversion mode after a system reset.

The first AD conversion is executed after the AD conversion mode is switched from 8-bit to 12-bit AD REPREST conversion mode. THISDE

■ Consumption Current Characteristics at Ta=-40 to +85°C, VSS1=VSS2=VSS3=VSS4=0V typ: 3.3V

Parameter Symbol Phylicken/kk Conditions VDD [V] min typ max unit Normal mode consumption (Note 7-1) IDDOP (1) VDD 1 = VDD3 = VDD4 • FmCF=10 MHz ceramic oscillator mode • System clock set to 10 MHz • Infernal RC oscillation stopped • IDDOP (2) • FmCF=0Hz (oscillation stopped) • FmCYtal=32.768 kHz crystal oscillator mode • System clock set to internal RC oscillation • 1/1 frequency division mode 2.7 to 3.6 0.8 2.1 IDDOP (3) • FmCF=0Hz (oscillation stopped) • FmXtal=32.768 kHz crystal oscillator mode 2.7 to 3.6 0.8 2.1 IDDOP (3) • FmCF=0Hz (oscillation stopped) • FmXtal=32.768 kHz crystal oscillator mode 2.7 to 3.6 0.8 2.1 • System clock set to internal RC oscillation mode • System clock set to 32.768 kHz • Internal RC oscillation stopped) • FmXtal=32.768 kHz crystal oscillator mode 2.7 to 3.6 0.8 2.1		Symbol	Applicable	Conditions		Specification			
consumption current (Note 7-1) =VD2 =VD3 =VD4 mode • FmXtal=32.768 kHz crystal oscillator mode 2.7 to 3.6 5.0 12.0 IDDOP (2) • FmCF=0Hz (oscillation stopped) • FmCtal=32.768 kHz crystal oscillator mode 2.7 to 3.6 5.0 12.0 IDDOP (2) • FmCF=0Hz (oscillation stopped) • FmCtal=32.768 kHz crystal oscillator mode 2.7 to 3.6 0.8 2.1 IDDOP (3) • FmCF=0Hz (oscillation stopped) • FmCtal=32.768 kHz crystal oscillator mode 2.7 to 3.6 0.8 2.1 IDDOP (3) • FmCF=0Hz (oscillation stopped) • FmCtal=32.768 kHz crystal oscillator mode 2.7 to 3.6 0.8 2.1			Pin/Remarks		$V_{DD}[V]$	min	typ	max	unit
IDDOP (2) · FmCF=0Hz (oscillation stopped) · System clock set to internal RC oscillation · 1/1 frequency division mode · FmCF=0Hz (oscillation stopped) · FmCYtal=32.768 kHz crystal oscillator mode · System clock set to 32.768 kHz · Internal RC oscillation stopped · 1/1 frequency division mode · 1/1 frequency division mode · System clock set to 32.768 kHz · Internal RC oscillation stopped · 1/1 frequency division mode · System clock set to 32.768 kHz · Internal RC oscillation stopped · 1/1 frequency division mode	consumption current	IDDOP (1)	=V _{DD} 2 =V _{DD} 3	mode • FmX'tal=32.768 kHz crystal oscillator mode • System clock set to 10 MHz • Internal RC oscillation stopped	2.7 to 3.6		5.0	12.0	
• FmX'tal=32.768 kHz crystal oscillator mode • System clock set to 32.768 kHz • Internal RC oscillation stopped • 1/1 frequency division mode Continued on next page Continued on next page		IDDOP (2)		 FmX'tal=32.768 kHz crystal oscillator mode System clock set to internal RC oscillation 	2.7 to 3.6		0.8	2.1	mA
CONNENDED FOR MATION		IDDOP (3)		 FmX'tal=32.768 kHz crystal oscillator mode System clock set to 32.768 kHz Internal RC oscillation stopped 	2.7 to 3.6		30	136	μA
			-(ONIME Y	JU.		-		

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Parameter	Course has 1	Applicable	Carditiana		Specification				
	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit	
HALT mode consumption current (Note 7-1)	IDDHALT (1)	V_{DD1} $=V_{DD2}$ $=V_{DD3}$ $=V_{DD4}$	 HALT mode FmCF=10 MHz ceramic oscillator mode FmX'tal=32.768 kHz crystal oscillator mode System clock set to 10 MHz Internal RC oscillation stopped 1/1 frequency division mode 	2.7 to 3.6		1.5	3.2		
	IDDHALT (2)		 HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768 kHz crystal oscillator mode System clock set to internal RC oscillation 1/1 frequency division mode 	2.7 to 3.6		0.2	0.8	mA	2
	IDDHALT (3)		 HALT mode FmCF=0Hz (oscillation stopped) FmX'tal=32.768 kHz crystal oscillator mode System clock set to 32.768 kHz Internal RC oscillation stopped 1/1 frequency division mode 	2.7 to 3.6		.5	78	μA ext page.	G
				EV	one	NÁ	(10)		
	S ICE D	NO	RECONNERO	DUR DUR RINF	ons	Contra			

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Demonstern	Seconda e 1	Applicable Pin/Remarks	Carditiana			Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	V _{DD} [V]	min	typ	max	unit
HOLD mode consumption current	IDDHOLD (1)	V _{DD} 1	HOLD mode • CF1=VDD or open (external clock mode)	2.7 to 3.6		0.2	50	
	IDDHOLD (2)		HOLD mode • CF1=VDD or open (external clock mode) • LVD option selected	2.7 to 3.6		1.2	53	
HOLDX mode consumption current	IDDHOLD (3)		HOLDX mode • CF1=VDD or open (external clock mode) • FmX'tal=32.768 kHz crystal oscillator mode	2.7 to 3.6		4.6	71	μΑ
	IDDHOLD (4)		HOLDX mode • CF1=VDD or open (external clock mode) • FmX'tal=32.768 kHz crystal oscillator mode • LVD option selected	2.7 to 3.6		5.6	74	

Note 7-1 : The consumption current value includes none of the currents that flow into the output transistor and internal pull-up resistors.

■ F-ROM Programming Characteristics at Ta=+10 to +55°C, V_{SS} = V_{SS} = V_{SS} = 0V

Parameter	Symbol	Applicable Pin/Remarks	Conditions		68	Specifi		
Onboard programming current	IDDFW (1)	V _{DD} 1	Microcontroller crase current current is excluded.	V _{DD} [V] 2.7 to 3.6	min	typ	<u>max</u> 10	unit mA
Onboard programming time	tFW (1)		• 2K-byte erase operation	2.7 to 3.6	OP	W.	25	ms
	tFW (2)		• 2 byte programming operation	2.7 to 3.6			45	μs
THIS DE	S ICE P	PRE	SENTATIVEFC	~				

D						Specif	ication	
Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit
Por release	PORRL		Select from option.	2.57V	2.47	2.57	2.72	
voltage			(Note 8-1)	2.87V	2.77	2.87	3.02	
Detction voltage unknown state	POUKS		• See Fig 10. (Note 8-2)			0.7	0.95	V
Power supply rise time	PORIS		• Power supply rise time from 0V to 1.6V.				100	ms

■ Power-on Reset (POR) Characteristics at Ta=-40 to +85°C, V_{SS}1=V_{SS}2=V_{SS}3=V_{SS}4=0V

Note8-1 : The POR release level can be selected out of 2 levels only when the LVD reset function is disabled. Note8-2 : POR is in an unknown state before transistors start operation.

■ Low Voltage Detection Reset (LVD) Characteristics

			LVD) Characteristics =V _{SS} 3=V _{SS} 4=0V					25	GN
	a	D: (D 1				Specif	ication		
Parameter	Symbol	Pin/Remarks	Conditions	Option selected voltage	min	typ	max	unit	
LVD reset voltage (Note 9-1)	LVDET		Select from option. (Note 9-2) See Fig 11.	2.81V	2.71	2.81	2.96	v	
LVD hysteresis width	LVHYS			2.81V		60	017	mV	
Detection voltage unknown state	LVUKS		• See Fig 11. (Note 9-3)	NDIR	0,	107	0.95	V	
Low voltage detection minimum width (Replay sensitivity)	TLVDW		• See Fig.12.	10 IN	0.2			ms	

Note9-1 : LVD reset voltage specification values do not include hysteresis voltage.

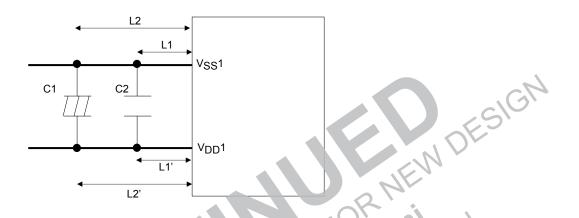
Note9-2 : LVD reset voltage may exceed its specification values when port output state changes and/or when a large current flows through port. Note9-3 LVD is in an unknown state before transistors start operation.

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Power Pin Treatment Conditions 1 (VDD1, VSS1)

Connect capacitors that meet the following conditions between the $V_{DD}1$ and $V_{SS}1$ pins :

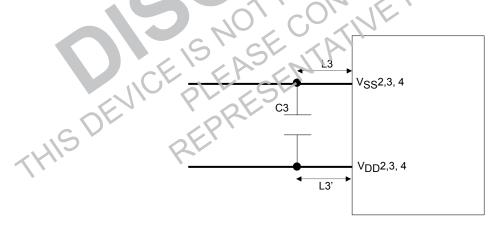
- Connect among the V_{DD}1 and V_{SS}1 pins and the capacitors C1 and C2 with the shortest possible lead wires, of the same length (L1=L1', L2=L2') wherever possible.
- Connect a large-capacity capacitor C1 and a small-capacity capacitor C2 in parallel. The capacitance of C2 should be approximately 0.1μ F or larger.
- The VDD1 and VSS1 traces must be thicker than the other traces.



■ Power Pin Treatment Conditions 2 (V[]2, 3, and VS2, 3, 4)

Connect capacitors that meet the following condition between the VDD2, 3, 4 and VSS2, 3, 4 pins :

- Connect among the V_{DD2}, 3–4 and \vee 3S2, 3, 4 pins and the capacitor C3 with the shortest possible lead wires, of the same length (L3=L3') wherever possible.
- The capacitance of C3 should be approximately 0.1μ F or larger.
- The V_{DD} 2, 3, 4 and V_{SS} 2, 3, 4 traces must be thicker than the other traces.



■ Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Resonator

Nominal	Vendor Name	Percentar		Circuit	Constant		Operating Voltage	Oscill Stabilizat		Remarks
Frequency	vendor Ivame	Resonator	C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]	Range [V]	typ [ms]	max [ms]	Remarks
10 MHz	MURATA	CSTCE10M0G52-R0	(10)	(10)	OPEN	680	2.2 to 2.6	0.02	0.2	C1, C2 integrated type
		CSTLS10M0G53-B0	(15)	(15)	OPEN	680	2.2 to 3.6	0.02	0.2	C1, C2 integrated type

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the lower limit level of the operating voltage range (see Figure 4)

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a Our Company -designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

■ Table 2 Characteristics of a Sample Subsystem Clock Oscillator Clicuit with a Crystal Resonator

Nominal	Vendor Name	Description		Circuit	Constan	t	Operating Voltage	Oscill Stabilizati		Devession
Frequency	vendor Name	Resonator	C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]	Range [V]	typ [s]	max [s]	Remarks
32.768 kHz	EPSON TOYOCOM	MC-306	10	10	Open	330K	2.2 to 3.6	1.0	3.0	CL=7.0pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillator circuit is executed plus the time interval that is required for the oscillation to get stabilized after the HOLD mode is released (see Figure 4).

Note : The traces to and from the components that are involved in oscillation should be kept as short as possible as the oscillation characteristics are affected by their trace pattern

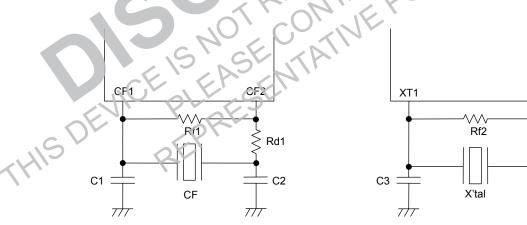
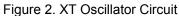


Figure 1. CF oscillator circuit



XT2

77

Rd2

C4



Figure 3. AC Timing Measurement Point

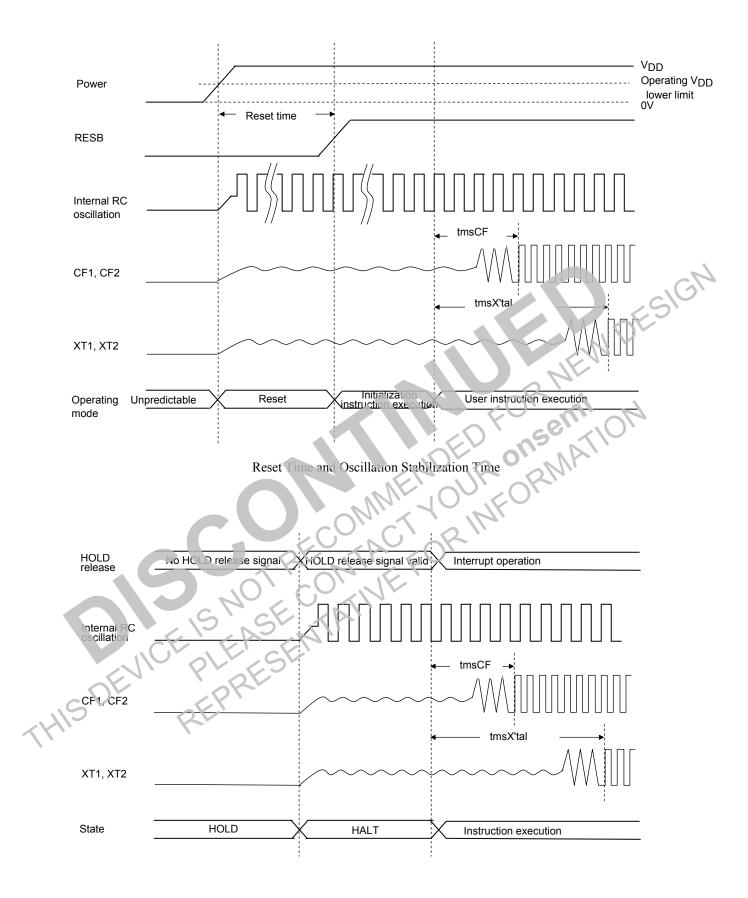
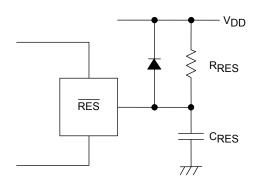




Figure 4. Oscillation Stabilization Time Timing Charts

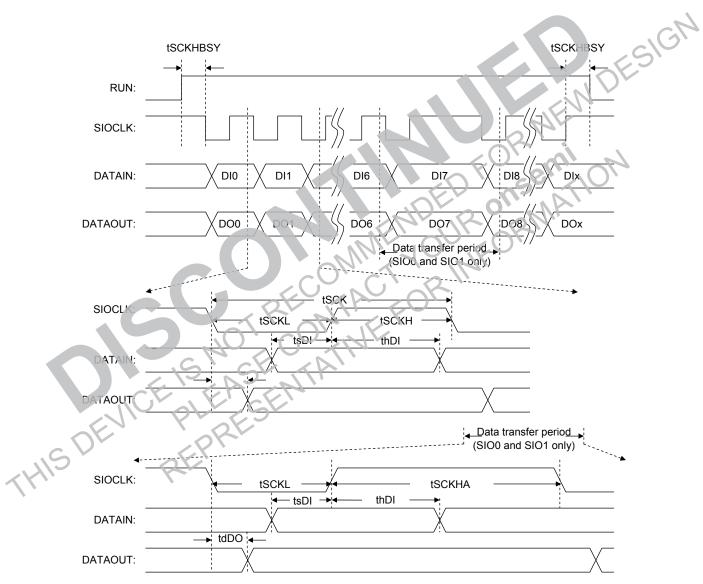


Note :

Reset signal must be present when power supply rises.

Determine the value of C_{RES} and R_{RES} so that the reset signal is present for 10 µs after the supply voltage gets stabilized.





* Remarks: DIx and DOx denote the last bits communicated; x=0 to 32768

Figure 6. Serial I/O Waveforms

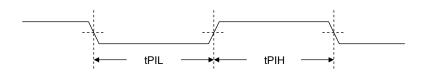
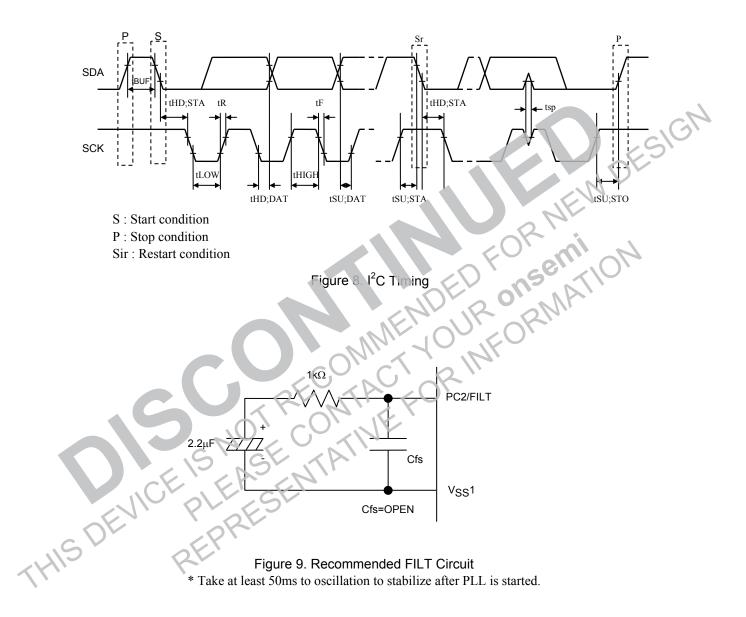


Figure 7. Pulse Input Timing Signal Waveform



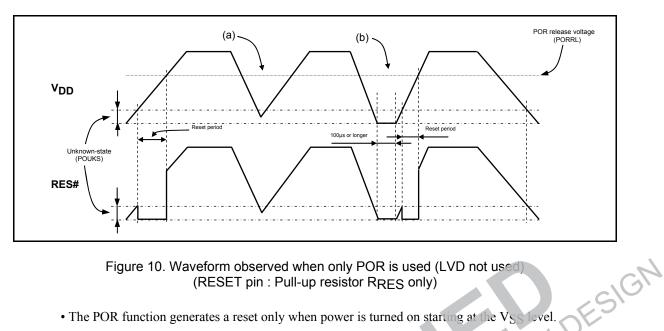
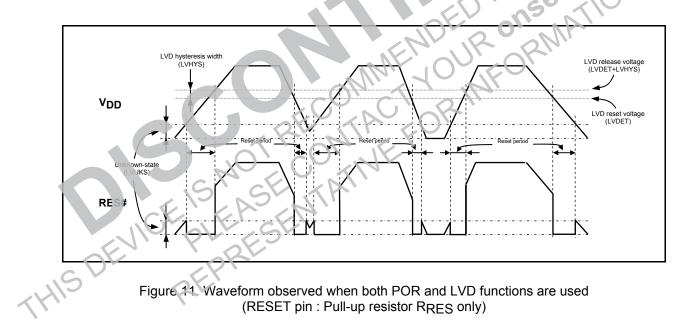
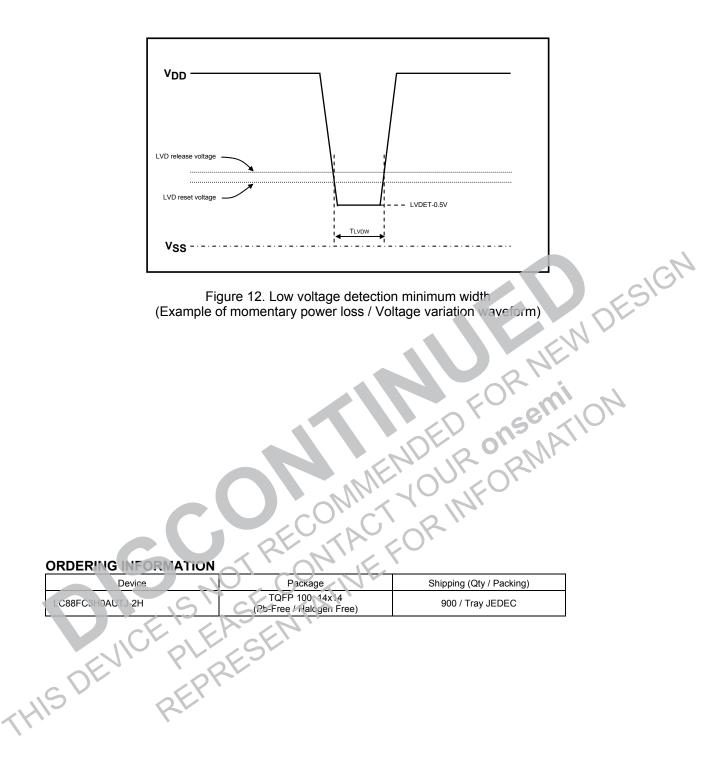


Figure 10. Waveform observed when only POR is used (LVD not used) (RESET pin : Pull-up resistor RRES only)

- The POR function generates a reset only when power is turned on starting at the VSS level
- No stable reset will be generated if power is turned on again when the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit.
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100us or longer.



- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.



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