

Dual Bias Resistor Transistor

NPN Surface Mount

IMH20TR1G

• Low V_{CC} (sat) 80 mV max at IC/IB = 50 mA/2.5 mA

• High Current: $I_C = 600 \text{ mA max}$

• This is a Pb-Free Device

MAXIMUM RATINGS (T_A = 25°C)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V _{(BR)CBO}	30	Vdc
Collector-Emitter Voltage	V _{(BR)CEO}	15	Vdc
Emitter-Base Voltage	V _{(BR)EBO}	5.0	Vdc
Collector Current - Continuous	I _C	600	mAdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Power Dissipation*	P_{D}	300	mW
Junction Temperature	T _J	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

^{*}Total for both Transistors.

Q1 + Q2: NPN

ELECTRICAL CHARACTERISTICS

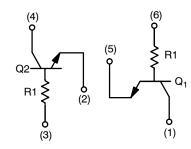
(T_A = 25°C unless otherwise noted)

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Characteristic	Symbol	Min	Max	Unit
Collector–Emitter Breakdown Voltage $(I_C = 1.0 \text{ mAdc}, I_B = 0)$	V _{(BR)CEO}	15	-	Vdc
Collector–Base Breakdown Voltage ($I_C = 50 \mu Adc, I_E = 0$)	V _{(BR)CBO}	30	-	Vdc
Emitter–Base Breakdown Voltage ($I_E = 50 \mu Adc, I_C = 0$)	V _{(BR)EBO}	5.0	-	Vdc
Collector-Base Cutoff Current (V _{CB} = 20 Vdc, I _E = 0)	I _{CBO}	_	0.5	μAdc
Emitter–Base Cutoff Current (V _{EB} = 4.0 V, I _C = 0)	I _{EBO}	-	0.5	μAdc
DC Current Gain (Note 1) (V _{CE} = 5.0 Vdc, I _C = 50 mAdc)	h _{FE}	100	600	_
Collector–Emitter Saturation Voltage (I _C = 50 mAdc, I _B = 2.5 mAdc)	V _{CE(sat)}	-	80	mV
Input Resistance	R ₁	1.54	2.86	kΩ

^{1.} Pulse Test: Pulse Width \leq 300 μ s, D.C. \leq 2%.



SC-74R 318AA Style 21



SC-74

MARKING DIAGRAM



H20 = Specific Device Code M = Date Code

ORDERING INFORMATION

Device	Package	Shipping [†]	
IMH20TR1G	SC-74R	3000/Tape & Reel	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.





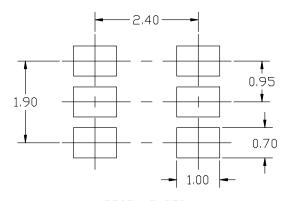
SC74-6 3.00x1.50x0.90, 0.95P CASE 318AA ISSUE C

DATE 22 AUG 2023

NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETERS
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

	MILLIMETERS		
DIM	MIN.	N□M.	MAX.
Α	0.90	1.00	1.10
A1	0.01	0.06	0.10
A2	0.80	0.90	1.00
b	0.25	0.37	0.50
C	0.10	0.18	0.26
D	2.90	3.00	3.10
Е	1.30	1.50	1.70
е	0.85	0.95	1.05
L	0.20	0.40	0.60
HE	2.50	2.75	3.00
М	0°	_	10°



RECOMMENDED MOUNTING FOOTPRINT*

For additional information on our Pb-Free strategy and soldering details, please download the DN Semiconductor Soldering and Mounting Techniques Reference Manual, SDLDERRM/D.

STYLE 20:
PIN 1. COLLECTOR 1
2. BASE 2
3 FMITTER 2

4. COLLECTOR 2 5. BASE 1

6. EMITTER 1

STYLE 21: PIN 1. COLLECTOR 1 2. EMITTER 2 3. BASE 2

4. COLLECTOR 2 5. EMITTER 1 6. BASE 1

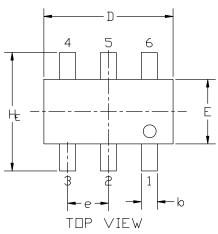
device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "=", may or may not be present. Some products may not follow the Generic Marking.

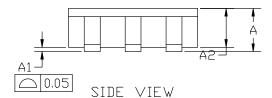
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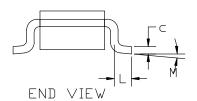
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GENERIC MARKING DIAGRAM*



XXX = Specific Device Code = Date Code Μ

*This information is generic. Please refer to

= Pb-Free Package

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