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## FQP8N90C / FQPF8N90C

### N-Channel QFET® MOSFET

900 V, 6.3 A, 1.9 Ω

#### Description

This N-Channel enhancement mode power MOSFET is • 6.3 A, 900 V,  $R_{DS(on)}$  = 1.9  $\Omega$  (Max.) @  $V_{GS}$  = 10 V, produced using ON Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state

• Low Gate Charge (Typ. 35 nC) resistance, and to provide superior switching performance

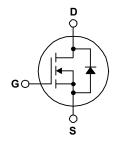
• Low Crss (Typ. 12 pF) and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power • 100% Avalanche Tested factor correction (PFC), and electronic lamp ballasts.

#### **Features**

- $I_D = 3.15 A$







#### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter		FQP8N90C	FQPF8N90C	Unit
$V_{DSS}$	Drain-Source Voltage		9	V	
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C)		6.3	6.3 *	Α
	- Continuous (T <sub>C</sub> = 100°C)		3.8	3.8 *	Α
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	25	25 *	Α
V <sub>GSS</sub>	Gate-Source Voltage		±	V	
E <sub>AS</sub>	Single Pulsed Avalanche Energy	(Note 2)	850		mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	6.3		Α
E <sub>AR</sub>	Repetitive Avalanche Energy	(Note 1)	17.1		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	4.0		V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C)		171	60	W
	- Derate above 25°C		1.37	0.48	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150		°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		3	°C	

<sup>\*</sup> Drain current limited by maximum junction temperature.

#### **Thermal Characteristics**

Symbol	Parameter	FQP8N90C	FQPF8N90C	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.73	2.08	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink Typ, Max.	0.5		°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	62.5	62.5	°C/W

#### **Package Marking and Ordering Information**

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQP8N90C	FQP8N90C	TO-220	Tube	N/A	N/A	50 units
FQPF8N90C	FQPF8N90C	TO-220F	Tube	N/A	N/A	50 units

#### **Electrical Characteristics**

T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	900			V
ΔBV <sub>DSS</sub> / ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		0.95		V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 900 V, V <sub>GS</sub> = 0 V			10	μА
1	Gate-Body Leakage Current, Forward	V <sub>DS</sub> = 720 V, T <sub>C</sub> = 125°C V <sub>GS</sub> = 30 V, V <sub>DS</sub> = 0 V			100	μA nA
I <sub>GSSF</sub>	Gate-Body Leakage Current, Polward  Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, V_{DS} = 0 \text{ V}$			-100	nA
On Cha	aracteristics					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	3.0		5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 3.15 A		1.6	1.9	Ω
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 50 V, I <sub>D</sub> = 3.15 A		5.5		S
	ic Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$		1600	2080	pF
C <sub>oss</sub>	Output Capacitance	f = 1.0 MHz		130	170	pF
C <sub>rss</sub>	Reverse Transfer Capacitance			12	15	pF
Switch	ing Characteristics					
$t_{d(on)}$	Turn-On Delay Time	V <sub>DD</sub> = 450 V, I <sub>D</sub> = 8 A,		40	90	ns
t <sub>r</sub>	Turn-On Rise Time	$R_{G} = 25 \Omega$		110	230	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	- ···		70	150	ns
t <sub>f</sub>	Turn-Off Fall Time	(Note 4)		70	150	ns
Qg	Total Gate Charge	V <sub>DS</sub> = 720 V, I <sub>D</sub> = 8 A,		35	45	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		10		nC
_		7				

#### **Drain-Source Diode Characteristics and Maximum Ratings**

I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current				6.3	Α
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current				25	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 6.3 \text{ A}$			1.4	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 8 A,		530		ns
Q <sub>rr</sub>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/μs		5.8	-	μС

14

nC

 $Q_{gd}$ 

- **Notes:**1. Repetitive rating: pulse-width limited by maximum junction temperature.
  2. L = 40 mH,  $I_{AS}$  = 6.3 A,  $V_{DD}$  = 50 V,  $R_{G}$  = 25  $\Omega$ , starting  $T_{J}$  = 25°C.
  3.  $I_{SD}$  ≤ 8 A, di/dt ≤ 200 A/ $\mu$ s,  $V_{DD}$  ≤ BV $_{DSS}$ , starting  $T_{J}$  = 25°C.
  4. Essentially independent of operating temperature.

Gate-Drain Charge

#### **Typical Characteristics**

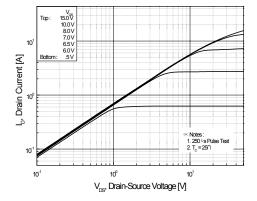


Figure 1. On-Region Characteristics

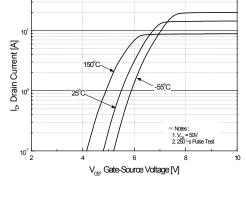


Figure 2. Transfer Characteristics

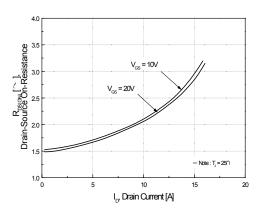


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

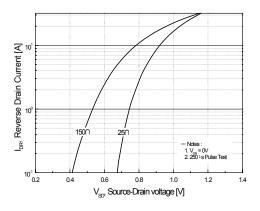


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

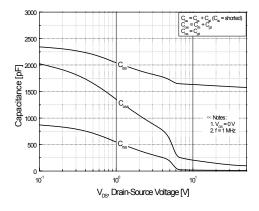


Figure 5. Capacitance Characteristics

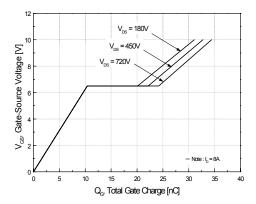


Figure 6. Gate Charge Characteristics

#### Typical Characteristics (Continued)

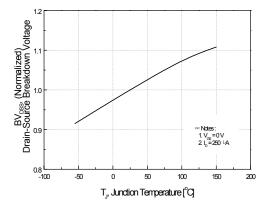


Figure 7. Breakdown Voltage Variation vs Temperature

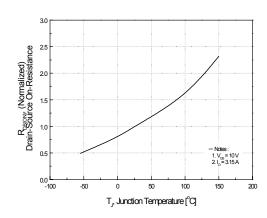


Figure 8. On-Resistance Variation vs Temperature

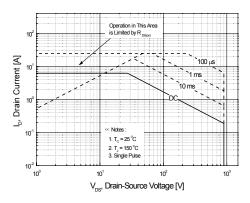


Figure 9-1. Maximum Safe Operating Area for FQP8N90C

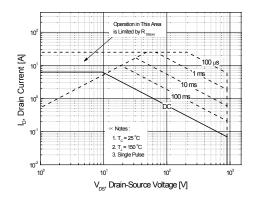


Figure 9-2. Maximum Safe Operating Area for FQPF8N90C

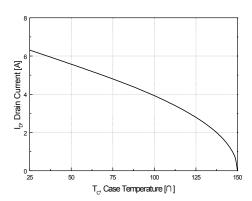


Figure 10. Maximum Drain Current vs Case Temperature

#### Typical Characteristics (Continued)

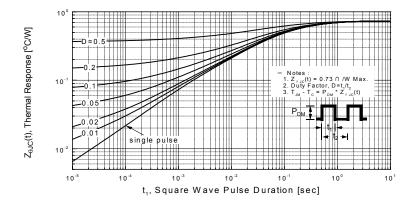


Figure 11-1. Transient Thermal Response Curve for FQP8N90C

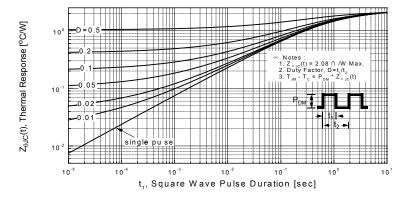


Figure 11-2. Transient Thermal Response Curve for FQPF8N90C

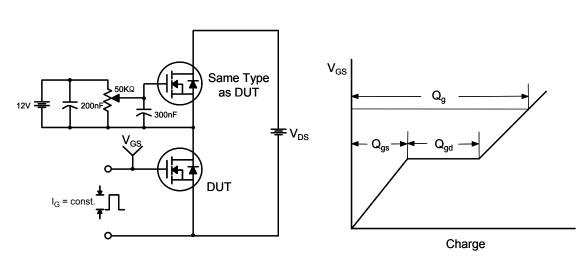


Figure 12. Gate Charge Test Circuit & Waveform

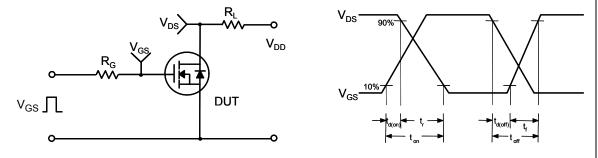


Figure 13. Resistive Switching Test Circuit & Waveforms

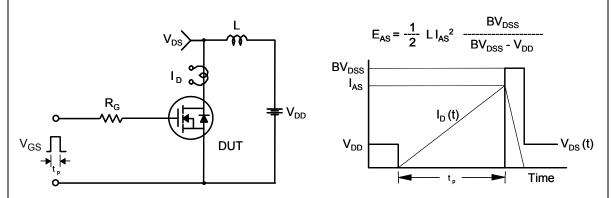
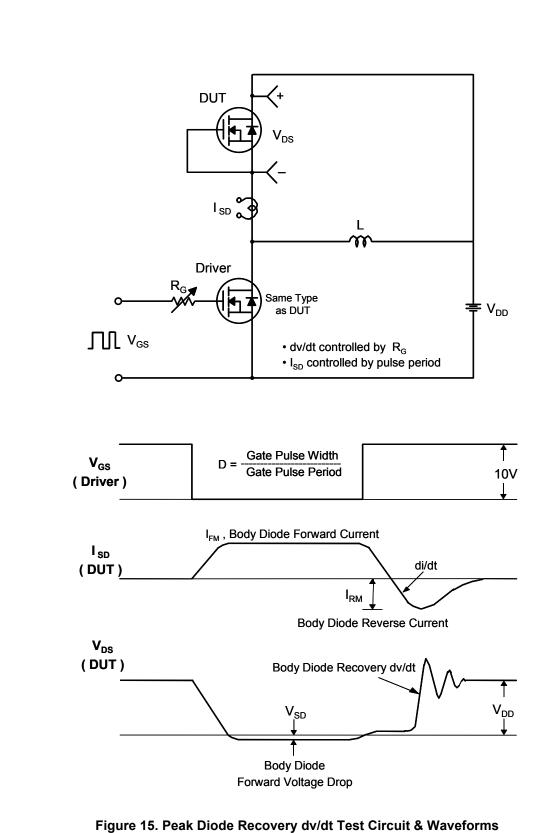
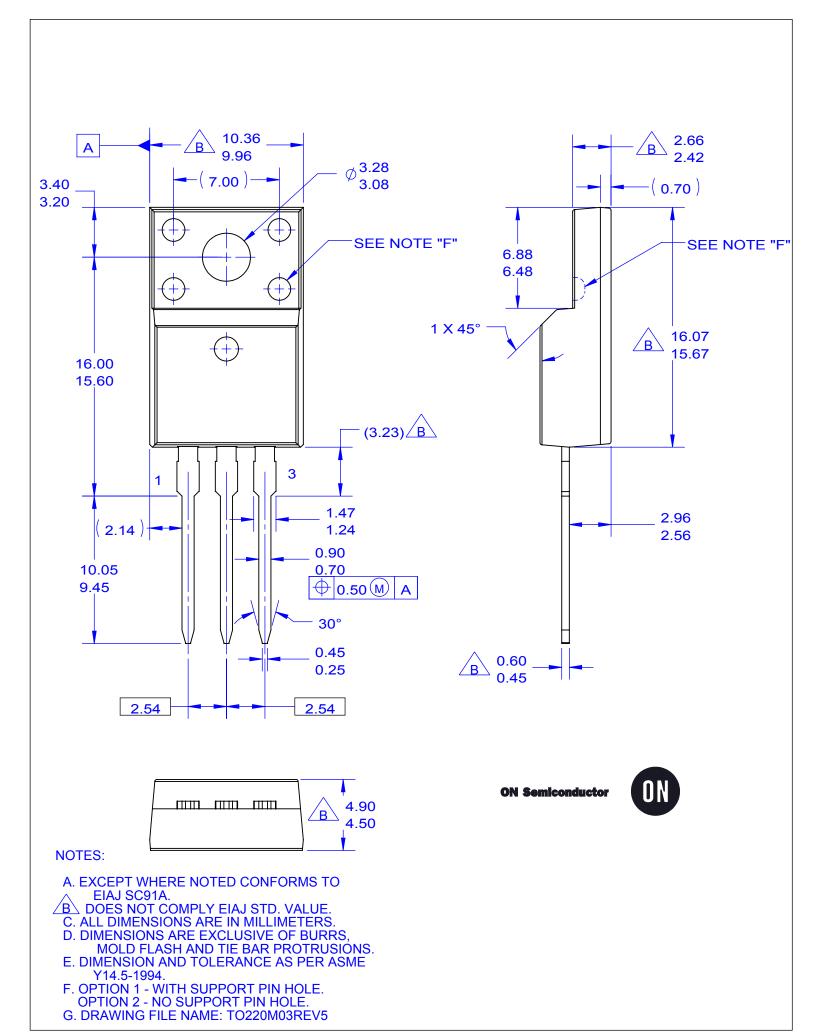


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms







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