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November 2013

FQD7N10L

N-Channel QFET® MOSFET

100 V, 5.8 A, 350 mΩ

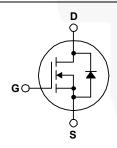
Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

Features

- 5.8 A, 100 V, $R_{DS(on)}$ = 350 m Ω (Max.) @ V_{GS} = 10 V, ID = 2.9 A
- Low Gate Charge (Typ. 4.6 nC)
- Low Crss (Typ. 12 pF)
- · 100% Avalanche Tested





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

| Symbol | Parameter | | FQD7N10LTM | Unit |
|-----------------------------------|---|----------|-------------|------|
| V_{DSS} | Drain-Source Voltage | | 100 | V |
| I _D | Drain Current - Continuous (T _C = 25°C) | | 5.8 | Α |
| | - Continuous (T _C = 100°C) | | 3.67 | Α |
| I _{DM} | Drain Current - Pulsed | (Note 1) | 23.2 | Α |
| V _{GSS} | Gate-Source Voltage | | ± 20 | V |
| E _{AS} | Single Pulsed Avalanche Energy (Note 2) | | 50 | mJ |
| I _{AR} | Avalanche Current | (Note 1) | 5.8 | Α |
| E _{AR} | Repetitive Avalanche Energy (No | | 2.5 | mJ |
| dv/dt | Peak Diode Recovery dv/dt (Note 3) | | 6.0 | V/ns |
| P _D | Power Dissipation (T _A = 25°C) * | | 2.5 | W |
| | Power Dissipation (T _C = 25°C) | | 25 | W |
| | - Derate above 25°C | | 0.2 | W/°C |
| T _J , T _{STG} | Operating and Storage Temperature Range | | -55 to +150 | °C |
| T _L | Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds | | 300 | °C |

Thermal Characteristics

| Symbol | Parameter | FQD7N10LTM | Unit |
|-----------------|---|------------|------|
| R_{\thetaJC} | Thermal Resistance, Junction to Case, Max. | 5.0 | |
| В | Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max. | 110 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (*1 in ² Pad of 2-oz Copper), Max. | 50 | |

Package Marking and Ordering Information

| Part Number | Top Mark | Package | Packing Method | Reel Size | Tape Width | Quantity |
|-------------|----------|---------|----------------|-----------|------------|------------|
| FQD7N10LTM | FQD7N10L | D-PAK | Tape and Reel | 330 mm | 16 mm | 2500 units |

Electrical Characteristics T_c = 25°C unless otherwise noted.

| Symbol | Parameter | Test Conditions | Min. | Тур. | Max. | Unit |
|---|---|---|----------|----------------|--------------|------|
| Off Cha | aracteristics | | | | | |
| BV _{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$ | 100 | | | V |
| ΔBV _{DSS} / ΔT _J | Breakdown Voltage Temperature Coefficient | I_D = 250 μ A, Referenced to 25°C | | 0.1 | | V/°C |
| I _{DSS} | Zana Cata Valtana Duain Comment | V _{DS} = 100 V, V _{GS} = 0 V | | | 1 | μΑ |
| | Zero Gate Voltage Drain Current | V _{DS} = 80 V, T _C = 125°C | | - | 10 | μΑ |
| I _{GSSF} | Gate-Body Leakage Current, Forward | V _{GS} = 20 V, V _{DS} = 0 V | | | 100 | nA |
| I _{GSSR} | Gate-Body Leakage Current, Reverse | V _{GS} = -20 V, V _{DS} = 0 V | | - | -100 | nA |
| On Cha | racteristics | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_{D} = 250 \mu A$ | 1.0 | | 2.0 | V |
| R _{DS(on)} | Static Drain-Source On-Resistance | $V_{GS} = 10 \text{ V}, I_D = 2.9 \text{ A}$ $V_{GS} = 5 \text{ V}, I_D = 2.9 \text{ A}$ | | 0.275 0.300 | 0.35 0.38 | Ω |
| 9 _{FS} | Forward Transconductance | V _{DS} = 30 V, I _D = 2.9 A | | 4.6 | | S |
| Dynam C _{iss} | ic Characteristics Input Capacitance | V = 25 V V = 0 V | | 220 | 290 | pF |
| C _{oss} | Output Capacitance | $V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz | | 55 | 72 | pF |
| C _{rss} | Reverse Transfer Capacitance | 1 - 1.0 WII IZ | | 12 | 15 | pF |
| Switchi | ing Characteristics | | <u> </u> | | | • |
| t _{d(on)} | Turn-On Delay Time | V - 50 V I - 72 A | | 9 | 30 | ns |
| t _r | Turn-On Rise Time | $V_{DD} = 50 \text{ V, } I_{D} = 7.3 \text{ A,}$ $R_{G} = 25 \Omega$ | | 100 | 210 | ns |
| t _{d(off)} | Turn-Off Delay Time | 11.6 2032 | | 17 | 45 | ns |
| t _f | Turn-Off Fall Time | (Note 4) | | 50 | 110 | ns |
| Qg | Total Gate Charge | V _{DS} = 80 V, I _D = 7.3 A, | | 4.6 | 6.0 | nC |
| Q _{gs} | Gate-Source Charge | V _{GS} = 5 V | | 1.0 | | nC |
| Q _{gd} | Gate-Drain Charge | (Note 4) | | 2.6 | | nC |
| Drain-S | Source Diode Characteristics a | nd Maximum Ratings | | | | |
| I _S | Maximum Continuous Drain-Source Diode Forward Current | | | | 5.8 | Α |
| I _{SM} | Maximum Pulsed Drain-Source Diode Forward Current | | | | 23.2 | Α |
| V _{SD} | Drain-Source Diode Forward Voltage | V _{GS} = 0 V, I _S = 5.8 A | | | 1.5 | V |
| t _{rr} | Reverse Recovery Time | V _{GS} = 0 V, I _S = 7.3 A, | | 70 | | ns |
| Q _{rr} | Reverse Recovery Charge | dl _F / dt = 100 A/μs | | 140 | // | nC |

- **Notes:** 1. Repetitive rating : pulse-width limited by maximum junction temperature. 2. L = 2.23 mH, I_{AS} = 5.8 A, V_{DD} = 25 V, R_{G} = 25 Ω , starting T_{J} = 25°C. 3. I_{SD} < 7.3 A, di/dt < 300 A/ μ s, V_{DD} < BV $_{DSS}$, starting T_{J} = 25°C. 4. Essentially independent of operating temperature.

Typical Characteristics

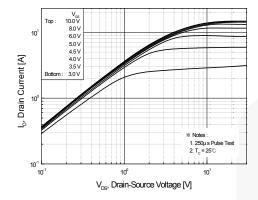


Figure 1. On-Region Characteristics

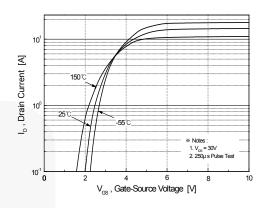


Figure 2. Transfer Characteristics

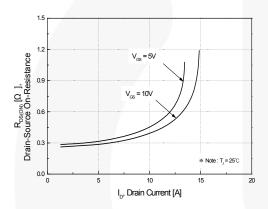


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

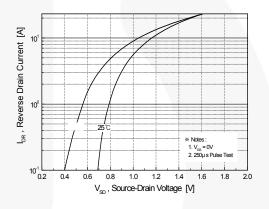


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

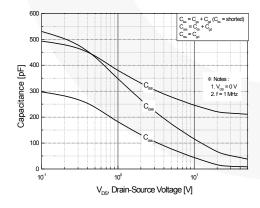


Figure 5. Capacitance Characteristics

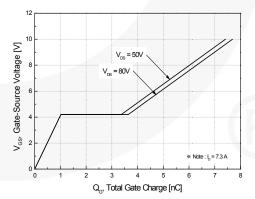


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

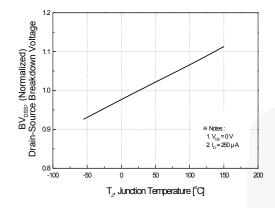
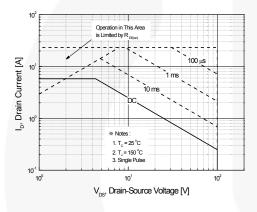


Figure 7. Breakdown Voltage Variation vs. Temperature

Figure 8. On-Resistance Variation vs. Temperature



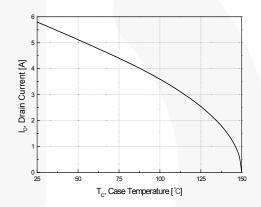


Figure 9. Maximum Safe Operating Area

Figure 10. Maximum Drain Current vs. Case Temperature

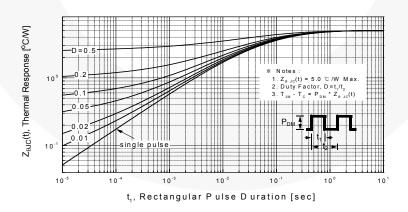


Figure 11. Transient Thermal Response Curve

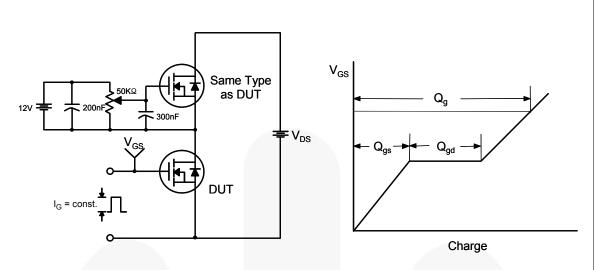


Figure 12. Gate Charge Test Circuit & Waveform

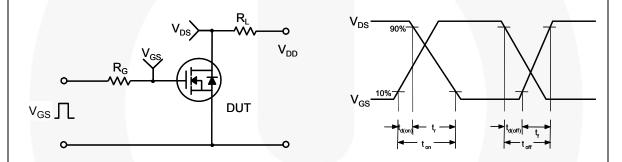


Figure 13. Resistive Switching Test Circuit & Waveforms

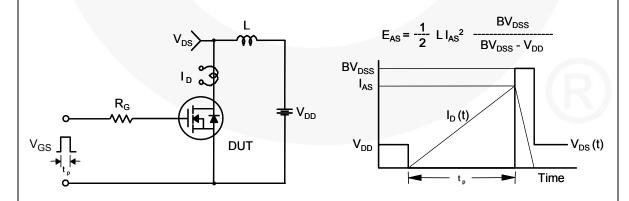
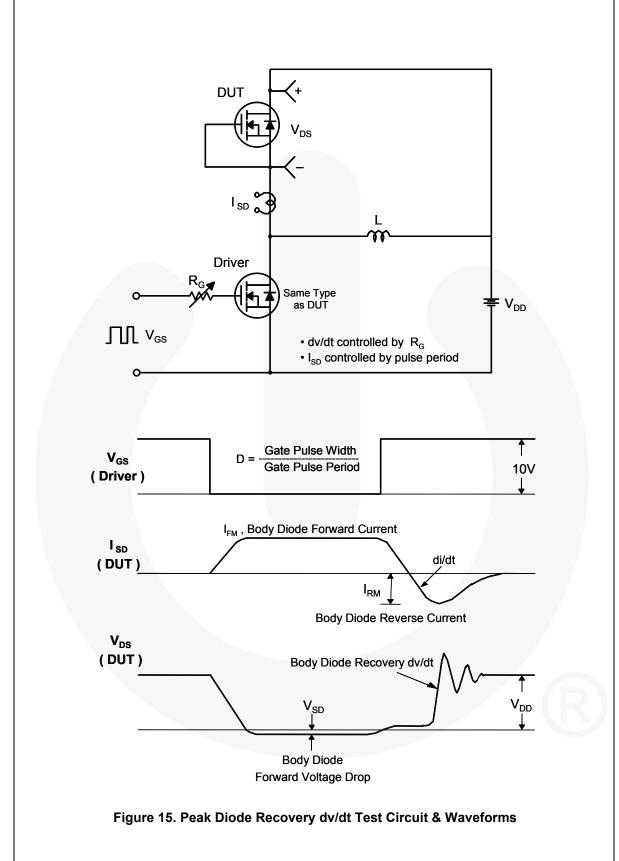


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



Mechanical Dimensions

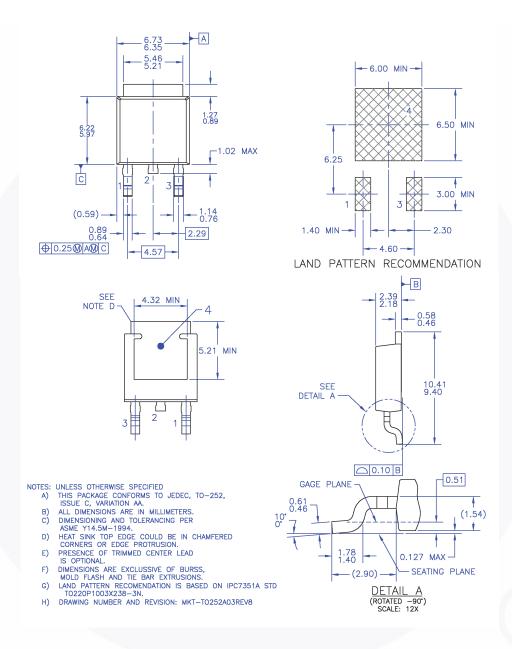


Figure 16. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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