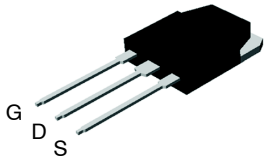
MOSFET – N-Channel, QFET

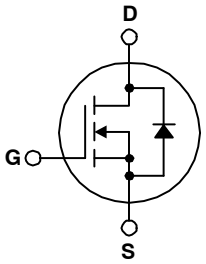
800 V, 12.6 A, 750 mΩ

FQA13N80-F109

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
800 V	750 mΩ @ 10 V	12.6 A



TO−3P−3LD
CASE 340BZ



N-CHANNEL MOSFET

Description

This N−Channel enhancement mode power MOSFET is produced using **onsemi**'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on−state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- 12.6 A, 800 V, $R_{DS(on)}$ = 750 mΩ (Max.) @ V_{GS} = 10 V, I_D = 6.3 A
- Low Gate Charge (Typ. 68 nC)
- Low C_{rss} (Typ. 30 pF)
- 100% Avalanche Tested
- This is Pb−Free and Halide Free Device

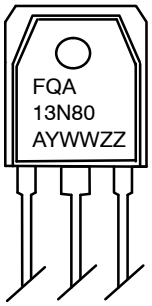
ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	800	V
I_D	Drain Current −Continuous (T_C = 25°C) −Continuous (T_C = 100°C)	12.6 8.0	A A
I_{DM}	Drain Current −Pulsed (Note 1)	50.4	A
V_{GSS}	Gate−Source Voltage	±30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	1100	mJ
I_{AR}	Avalanche Current (Note 1)	12.6	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	30	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.0	V/ns
P_D	Power Dissipation (T_C = 25°C) −Derate Above 25°C	300 2.38	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L = 13 mH, I_{AS} = 12.6 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25 °C.
3. I_{SD} ≤ 12.6 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25 °C.

MARKING DIAGRAM



FQA13N80	= Specific Device Code
A	= Assembly Location
YWW	= Date Code (Year & Week)
ZZ	= Assembly Lot

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case, Max.	0.42	°C/W
$R_{\theta CS}$	Thermal Resistance, Case−to−Sink, Typ.	0.24	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient, Max.	40	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	800	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.95	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	–	–	10	μA
		V_{DS} = 640 V, T_C = 125°C	–	–	100	μA
I_{GSSF}	Gate−Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage Current, Reverse	V_{GS} = −30 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 6.3 A	–	0.58	0.75	Ω
g_{FS}	Forward Transconductance	V_{DS} = 50 V, I_D = 6.3 A	–	13	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	2700	3500	pF
C_{oss}	Output Capacitance		–	275	360	pF
C_{rss}	Reverse Transfer Capacitance		–	30	39	pF
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 400 V, I_D = 12.6 A, R_G = 25 Ω (Note 4)	–	60	130	ns
t_r	Turn−On Rise Time		–	150	310	ns
$t_{d(off)}$	Turn-Off Delay Time		–	155	320	ns
t_f	Turn−Off Fall Time		–	110	230	ns
Q_g	Total Gate Charge	V_{DS} = 640 V, I_D = 12.6 A, V_{GS} = 10 V (Note 4)	–	68	88	nC
Q_{gs}	Gate−Source Charge		–	15	–	nC
Q_{gd}	Gate−Drain Charge		–	32	–	nC
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	12.6	A
I_{SM}	Maximum Pulsed Drain−Source Diode Forward Current		–	–	50.4	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 12.6 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 12.6 A, dI_F/dt = 100 A/μs	–	850	–	ns
Q_{rr}	Reverse Recovery Charge		–	11.3	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature.

TYPICAL CHARACTERISTICS

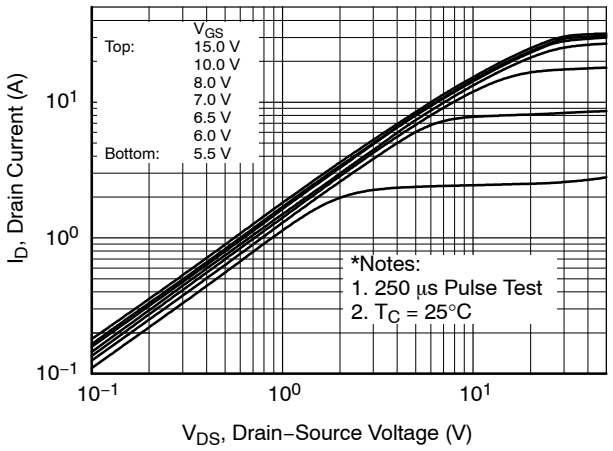


Figure 1. On−Region Characteristics

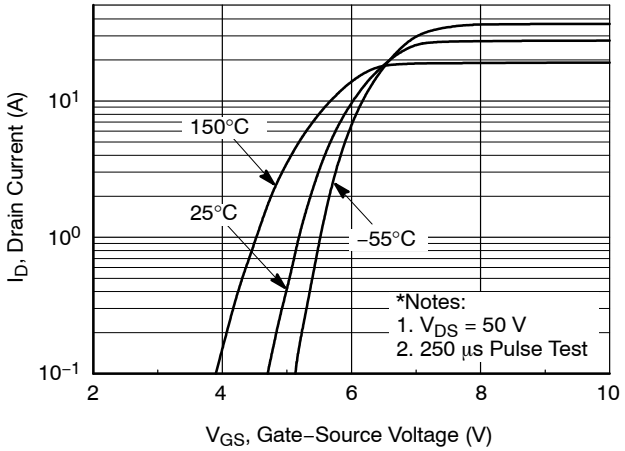


Figure 2. Transfer Characteristics

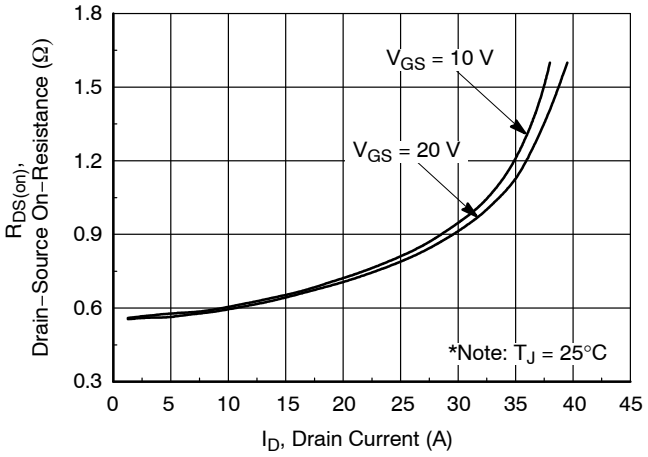


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

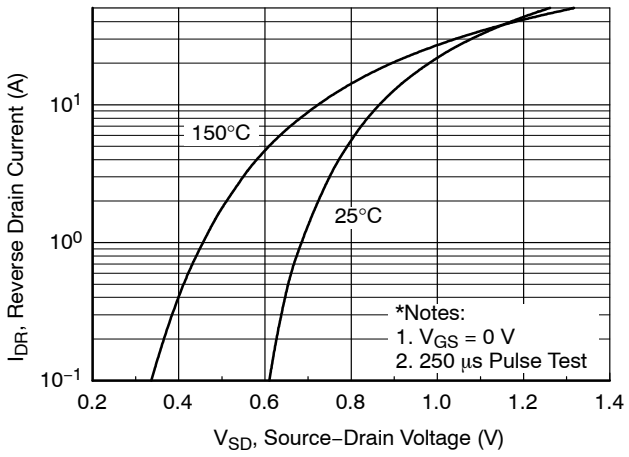


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

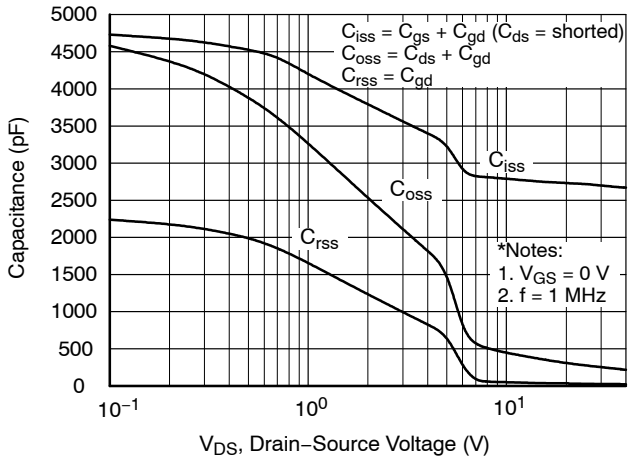


Figure 5. Capacitance Characteristics

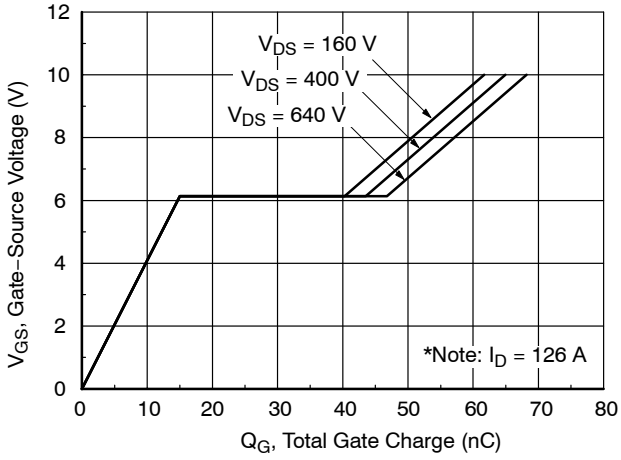


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS

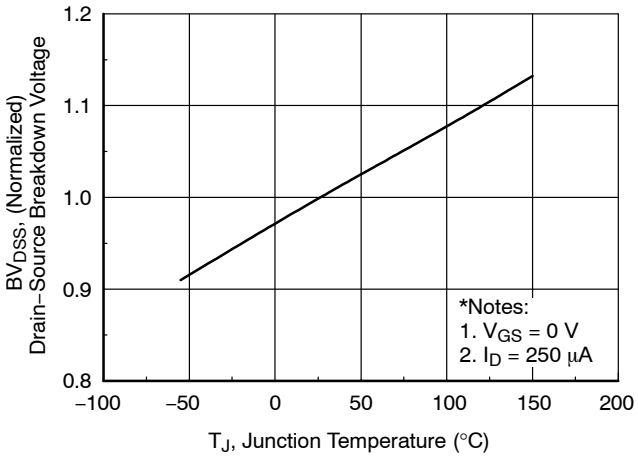


Figure 7. Breakdown Voltage Variation vs. Temperature

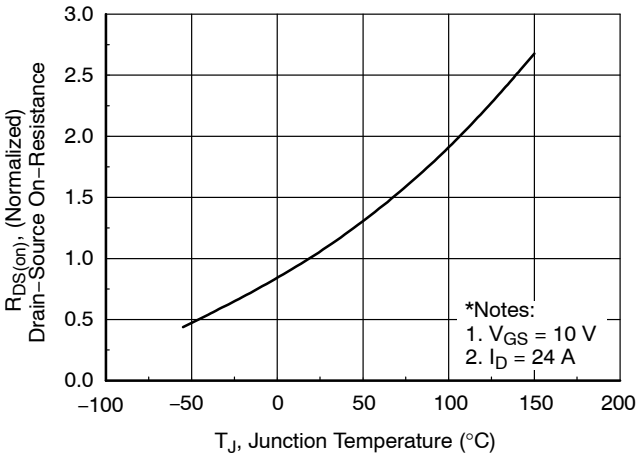


Figure 8. On−Resistance Variation vs. Temperature

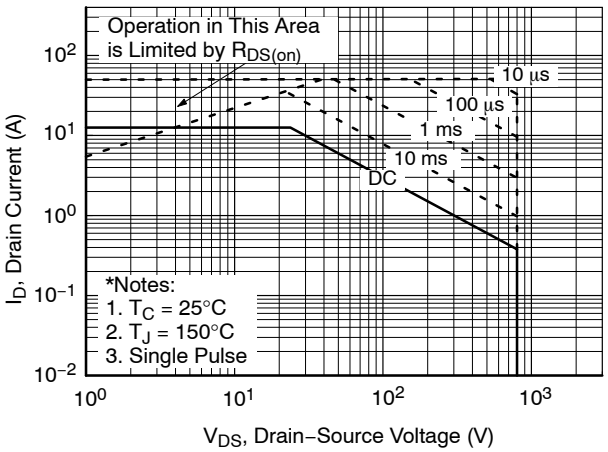


Figure 9. Maximum Safe Operating Area

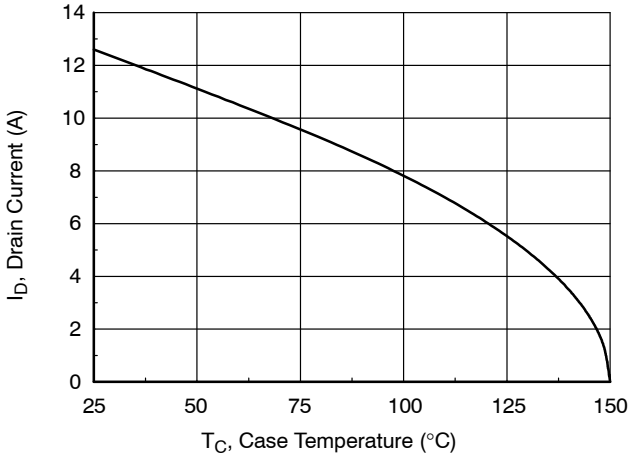


Figure 10. Maximum Drain Current vs. Case Temperature

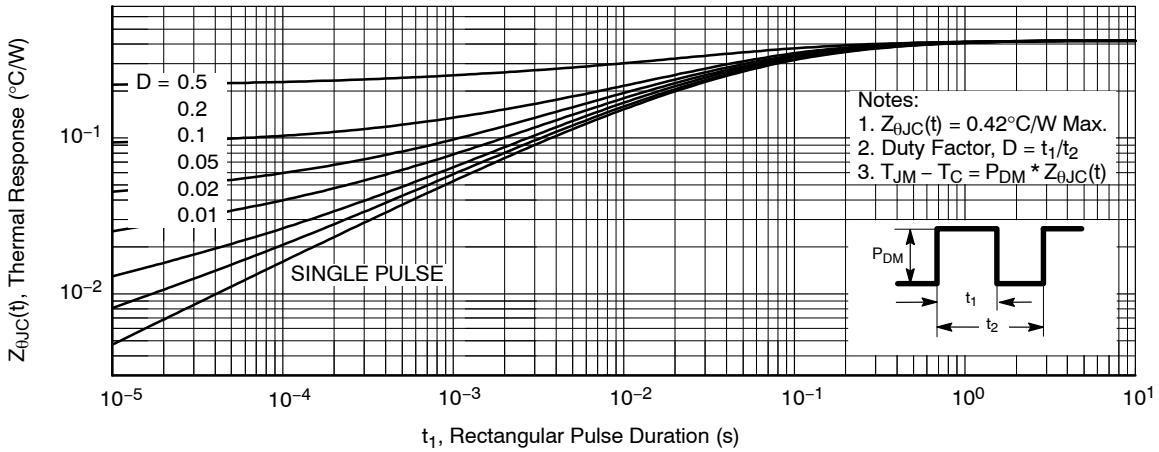


Figure 11. Transient Thermal Response Curve

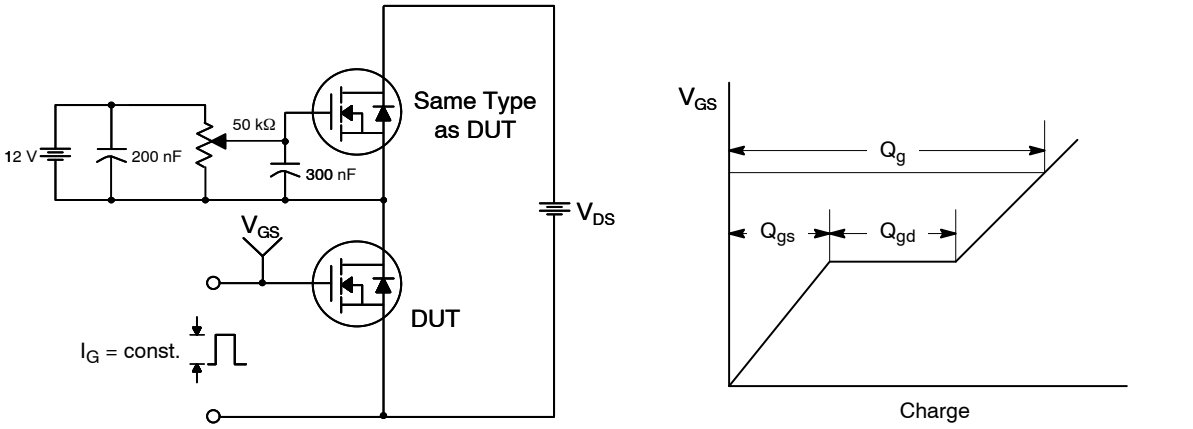


Figure 12. Gate Charge Test Circuit & Waveform

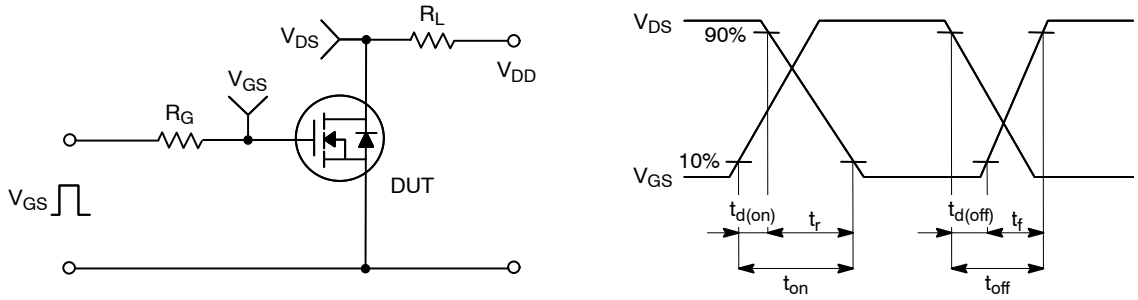


Figure 13. Resistive Switching Test Circuit & Waveforms

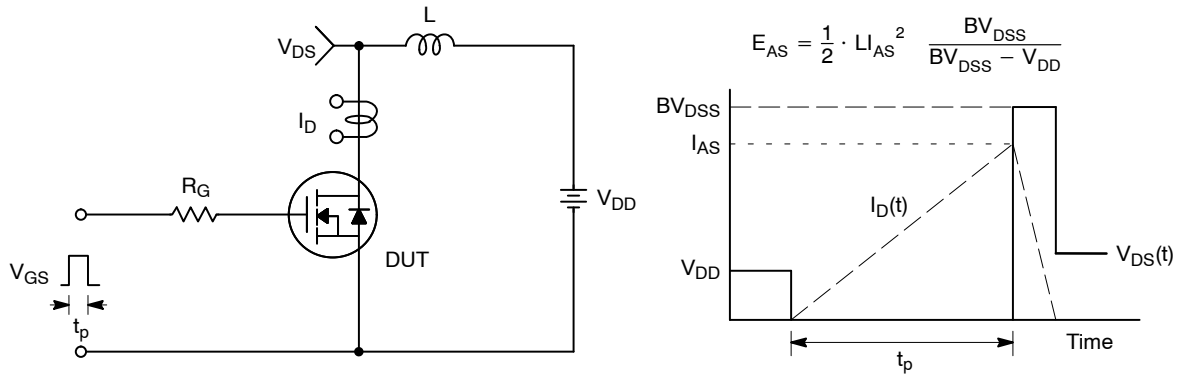


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

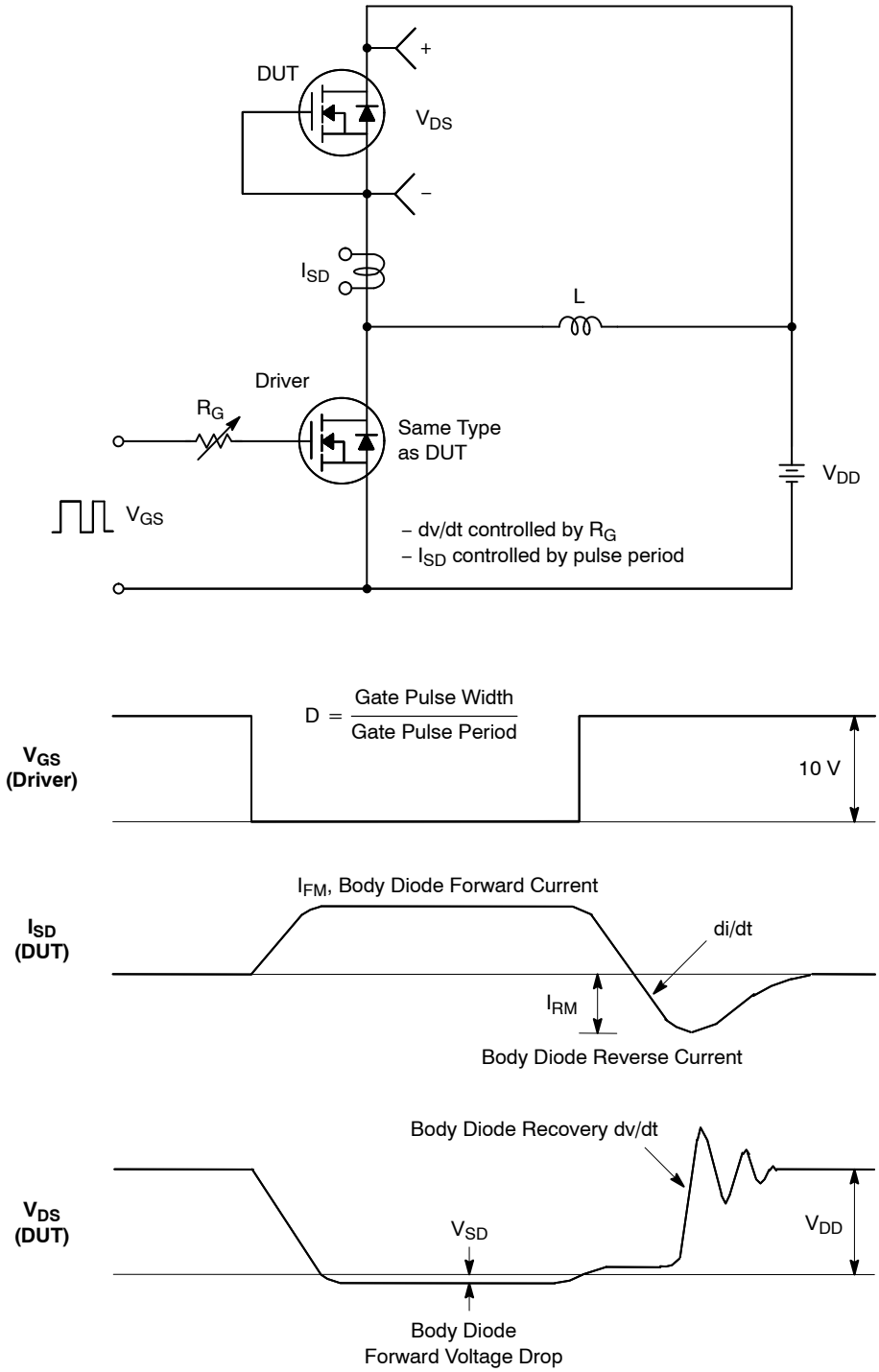


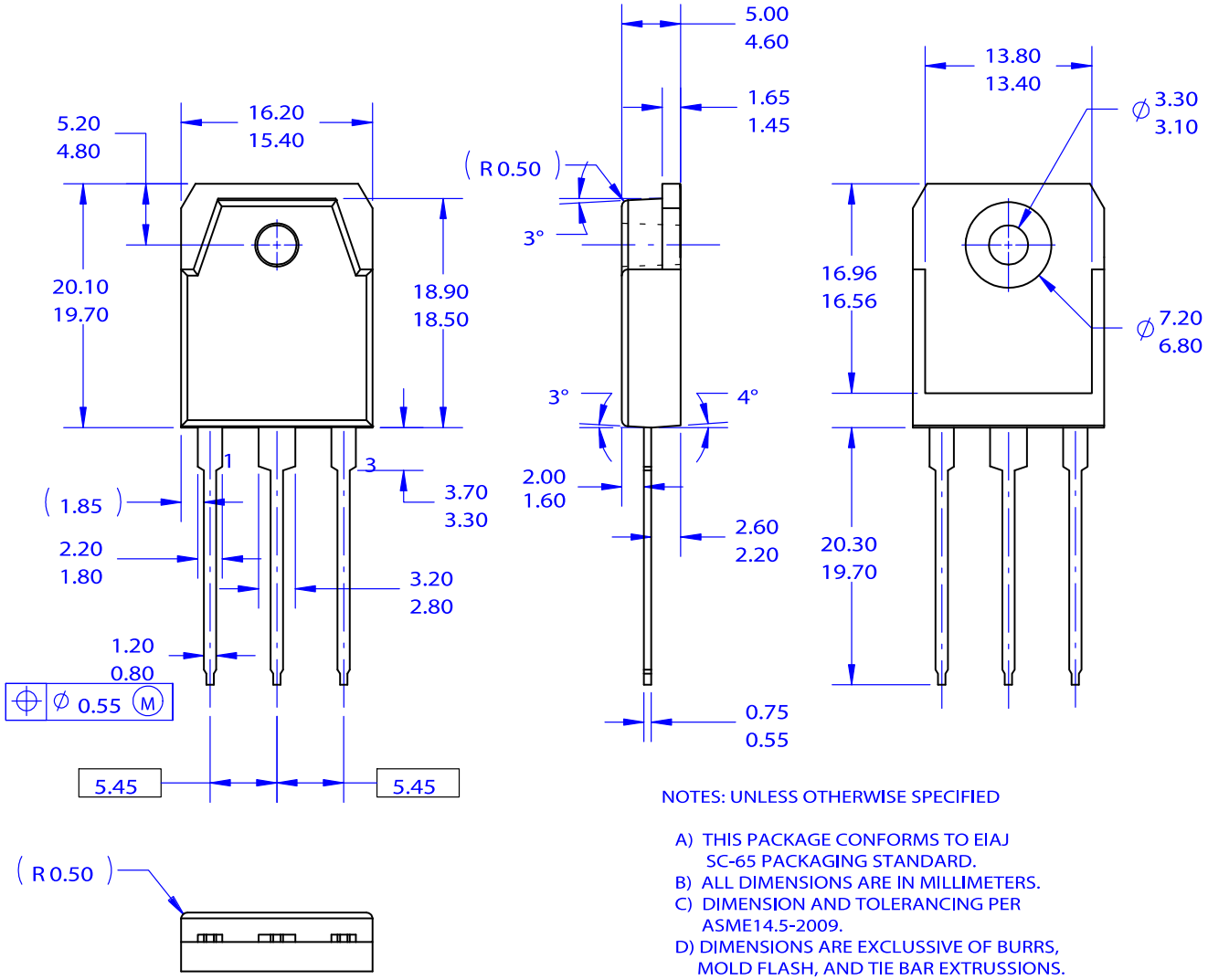
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Package Method	Reel Size	Tape Width	Quantity
FQA13N80−F109	FQA13N80	TO−3P−3LD	Tube	N/A	N/A	450 Units /Tube

TO−3P−3LD / EIAJ SC−65, ISOLATED
CASE 340BZ
ISSUE O

DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
D) DIMENSIONS ARE EXCLUSSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSSIONS.

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DESCRIPTION:	**TO−3P−3LD / EIAJ SC−65, ISOLATED**		**PAGE 1 OF 1**

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