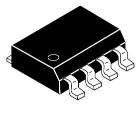
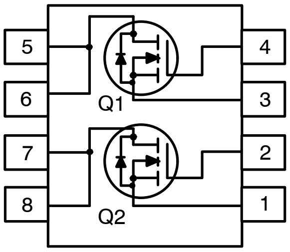
MOSFET – Dual, N-Channel, POWERTRENCH®, 80 V

FDS3890



SOIC8
CASE 751EB



General Description

This N−Channel MOSFET has been designed specifically to improve the overall efficiency of DC−DC converters using either synchronous or conventional switching PWM controllers.

These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable $R_{DS(ON)}$ specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC−DC power supply designs with higher overall efficiency.

Features

- 4.7 A, 80 V:
    - $R_{DS(ON)}$ = 44 mΩ @ V_{GS} = 10 V
    - $R_{DS(ON)}$ = 50 mΩ @ V_{GS} = 6 V
- Fast Switching Speed
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability
- Pb−Free and Halide Free

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted.)

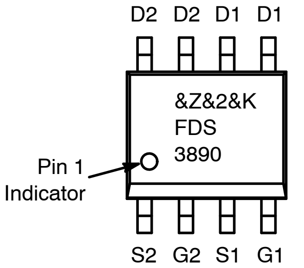
Symbol	Parameter	Ratings	Unit
V_{DSS}	Drain−Source Voltage	80	V
V_{GSS}	Gate−Source Voltage	±20	V
I_D	Drain Current Continuous (Note 1a) Pulsed	 4.7 20	A
P_D	Power Dissipation for Dual Operation	2	W
	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	 1.6 1.0 0.9	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +175	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	40	°C/W

MARKING DIAGRAM



&Z = Assembly Plant Code
&2 = Date Code (Year & Week)
&K = Lot Traceability Code
FDS3890 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping
FDS3890	SOIC8 (Pb−Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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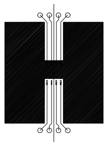
ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DRAIN−SOURCE AVALANCHE RATINGS (Note 2)						
W_{DSS}	Single Pulse Drain−Source Avalanche Energy	V_{DD} = 40 V, I_D = 4.7 A	–	–	175	mJ
I_{AR}	Maximum Drain−Source Avalanche Current		–	–	4.7	A
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	80	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	86	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 64 V, V_{GS} = 0 V	–	–	1	μA
I_{GSSF}	Gate−Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate−Body Leakage, Reverse	V_{GS} = −20 V, V_{DS} = 0 V	–	–	−100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 μA	2	2.3	4	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	−6	–	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = 10 V, I_D = 4.7 A V_{GS} = 6 V, I_D = 4.4 A V_{GS} = 10 V, I_D = 4.7 A, T_J = 125°C	– – –	34 37 60	44 50 82	mΩ
$I_{D(on)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	20	–	–	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 4.7 A	–	24	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 40 V, V_{GS} = 0 V, f = 1.0 MHz	–	1180	–	pF
C_{oss}	Output Capacitance		–	171	–	pF
C_{rss}	Reverse Transfer Capacitance		–	50	–	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 40 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	11	20	ns
t_r	Turn−On Rise Time		–	8	16	ns
$t_{d(off)}$	Turn−Off Delay Time		–	26	50	ns
t_f	Turn−Off Fall Time		–	12	25	ns
Q_g	Total Gate Charge	V_{DS} = 40 V, I_D = 4.7 A, V_{GS} = 10 V	–	25	35	nC
Q_{gs}	Gate−Source Charge		–	4.5	–	nC
Q_{gd}	Gate−Drain Charge		–	5.8	–	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		–	–	1.3	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 1.3 A (Note 2)	–	0.74	1.2	V

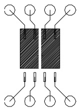
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

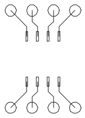
1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 1 in^2 pad of 2 oz. copper.



b) 125°C/W when mounted on a 0.04 in^2 pad of 2 oz. copper.



c) 135°C/W when mounted on a minimum pad.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL CHARACTERISTICS

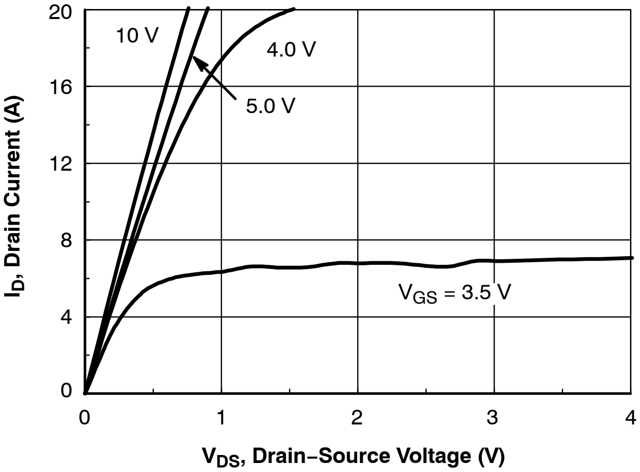


Figure 1. On−Region Characteristic

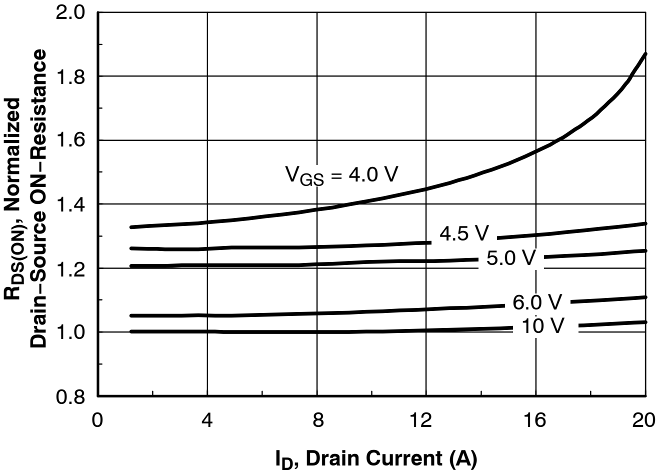


Figure 2. On−Resistance Variation with Drain Current and Gate Voltage

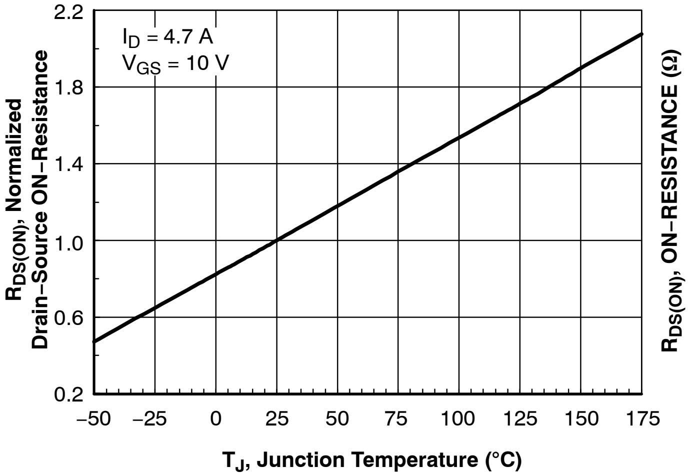


Figure 3. On−Resistance Variation with Temperature

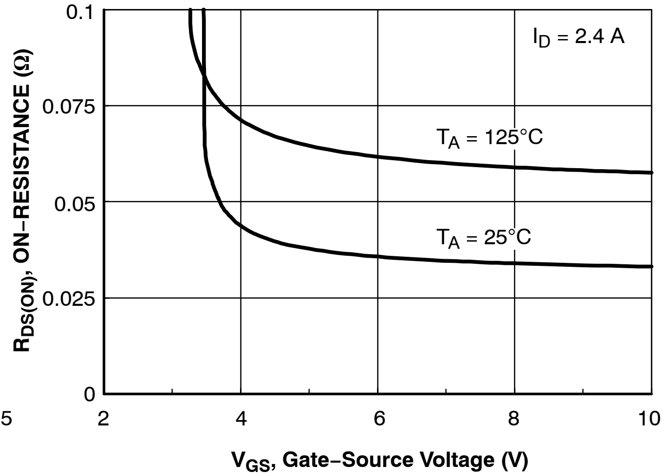


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

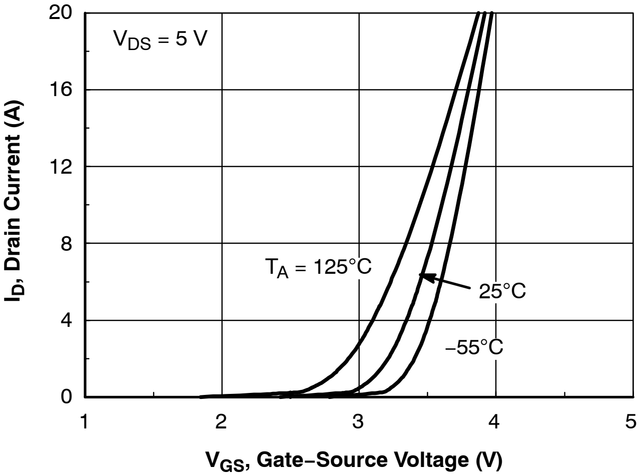


Figure 5. Transfer Characteristics

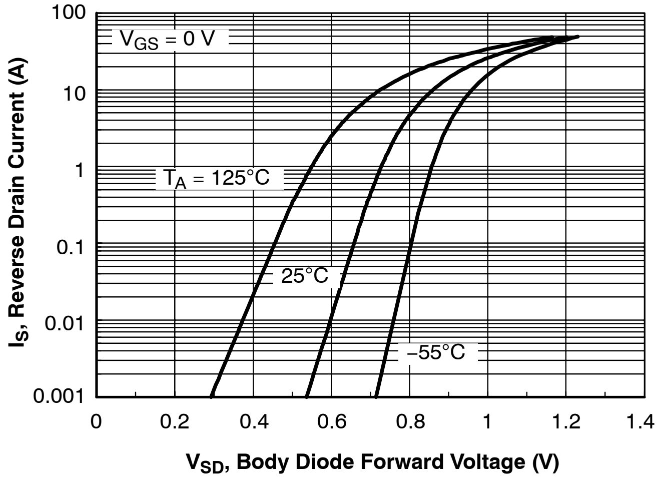


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (Continued)

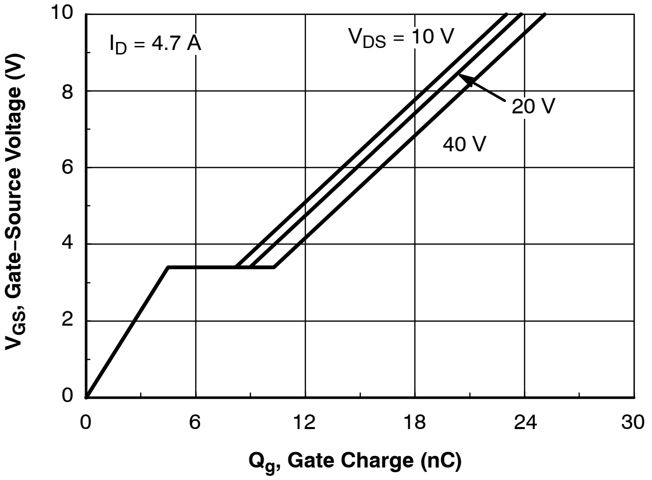


Figure 7. Gate−Charge Characteristics

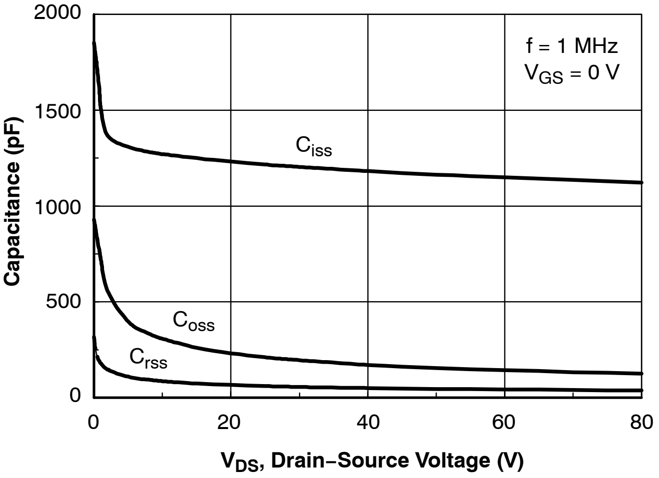


Figure 8. Capacitance Characteristics

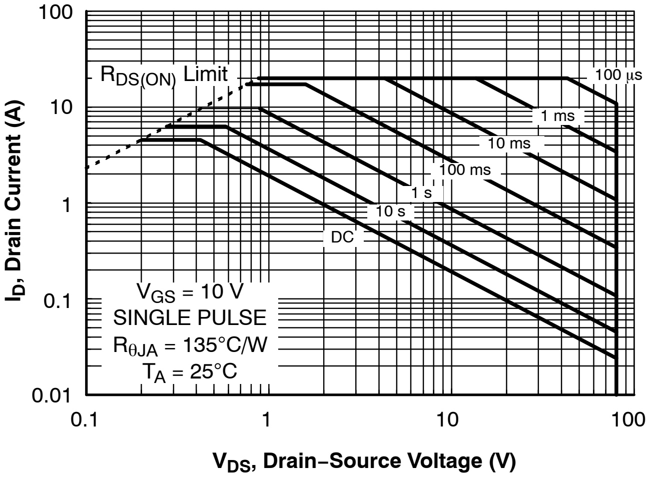


Figure 9. Maximum Safe Operating Area

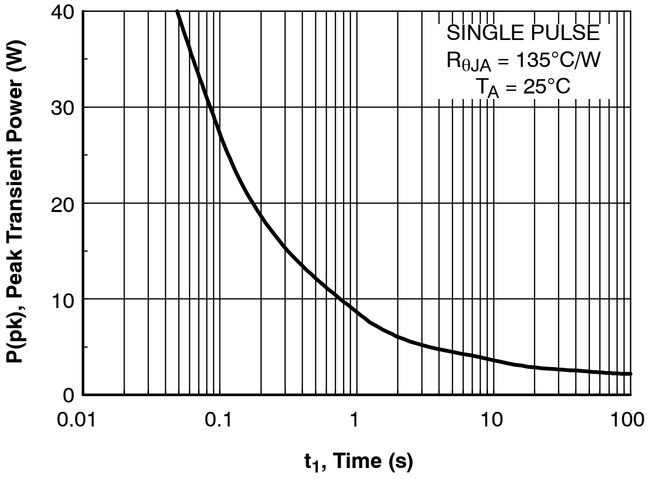


Figure 10. Single Pulse Maximum Power Dissipation

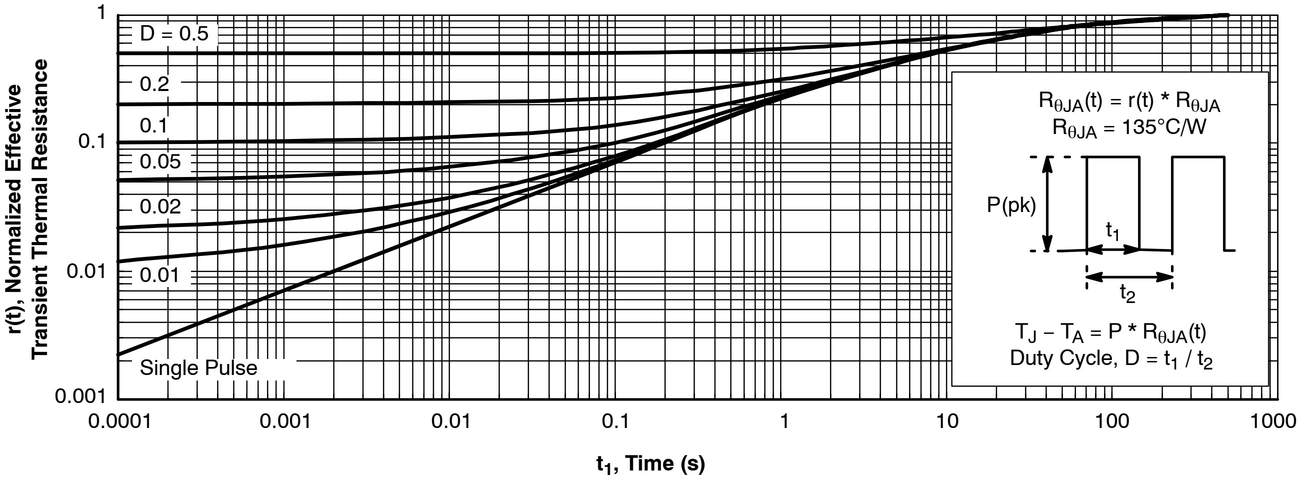


Figure 11. Transient Thermal Response Curve

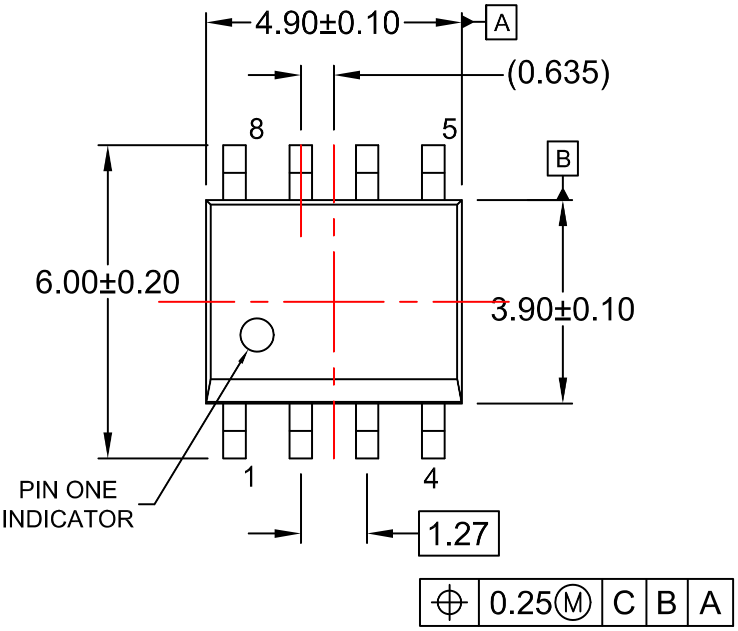
Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

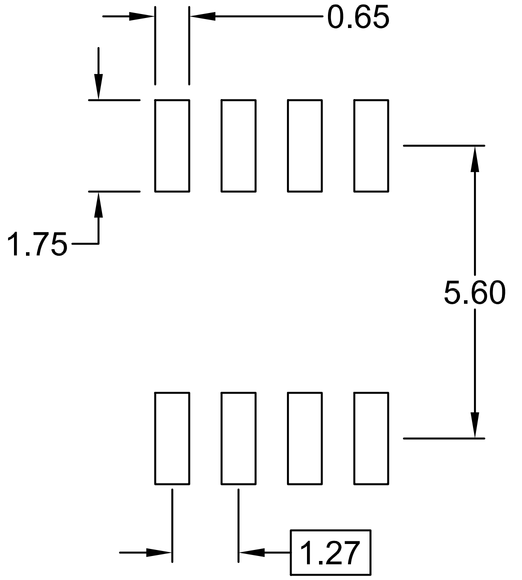
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

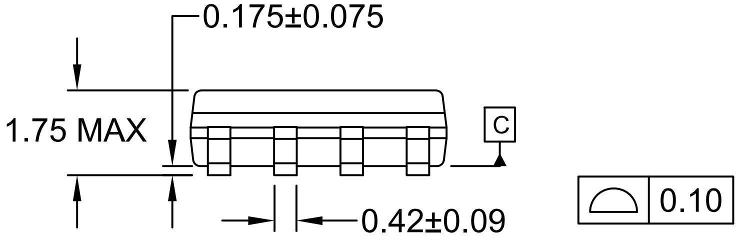
SOIC8
CASE 751EB
ISSUE A

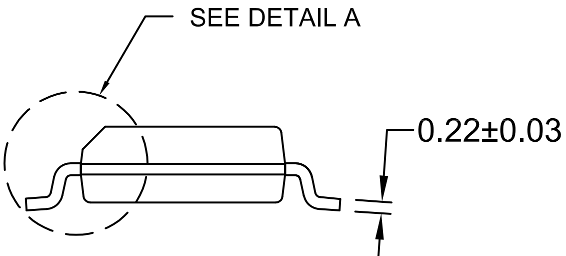
DATE 24 AUG 2017



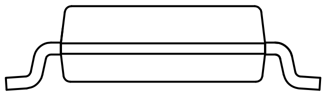


LAND PATTERN RECOMMENDATION

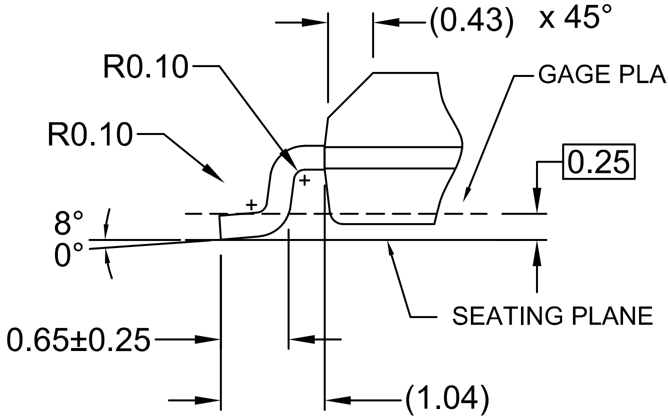




OPTION A - BEVEL EDGE



OPTION B - NO BEVEL EDGE



DETAIL A
SCALE: 2:1

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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