

# MOSFET – N-Channel, Shielded Gate POWERTRENCH®

100 V, 128 A, 4.5 mΩ

**FDP4D5N10C,  
FDPF4D5N10C**

## Description

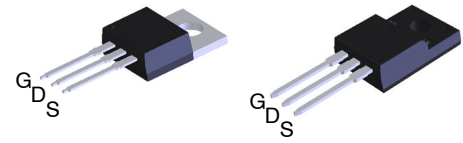
This N-Channel MV MOSFET is produced using onsemi's advanced PowerTrench process that incorporates Shielded Gate technology. This Process has been Optimized to minimize on-state resistance and yet maintain superior switching performance with best in class soft body diode.

## Features

- Max  $R_{DS(on)}$  = 4.5 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 100 A
- Extremely Low Reverse Recovery Charge,  $Q_{rr}$
- 100% UIL Tested
- This Device is Pb-Free Halide, Free and RoHS Compliant.

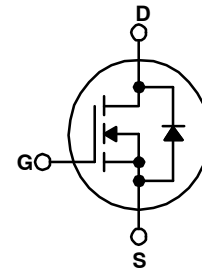
## Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

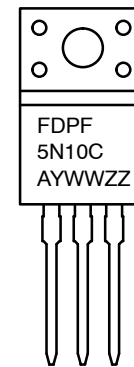


TO-220  
CASE 221A

TO-220 Fullpack, 3-Lead  
/ TO-220F-3SG  
CASE 221AT



## MARKING DIAGRAM



FDPF4D5N10C,  
FQD45N10C = Specific Device Code  
A = Assembly Location  
YWW = Date Code (Year and Week)  
ZZ = Assembly Lot Code

## ORDERING INFORMATION

Device	Package	Shipping†
FDPF4D5N10C	TO-220F (Pb-Free)	1000 Units / Tube
FDP4D5N10C	TO-220 (Pb-Free)	800 Units / Tube

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

# FDP4D5N10C,

## MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Ratings		Units
		FDP4D5N10C	FDPF4D5N10C	
$V_{DS}$	Drain to Source Voltage	100	100	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current – Continuous ( $T_C = 25^\circ\text{C}$ ) (Note 3) – Continuous ( $T_C = 100^\circ\text{C}$ ) (Note 3) – Pulsed (Note 1)	128* 91 512	128* 91 512	A
$E_{AS}$	Single Pulsed–Avalanche Energy (Note 2)	486		mJ
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	150	37.5	W
	Power Dissipation ( $T_A = 25^\circ\text{C}$ )	2.4	2.4	
$T_J, T_{STG}$	Operating and Storage Temperature Range	$-55$ to $+175$	$-55$ to $+175$	$^\circ\text{C}$

\*Drain current limited by maximum junction temperature. Package limitation current is 120 A.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

Symbol	Parameter	FDP4D5N10C	FDPF4D5N10C	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.0	4.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	62.5	62.5	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
--------	-----------	-----------------	-----	-----	-----	------

### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	53	–	mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 80 \text{ V}, T_J = 150^\circ\text{C}$	–	–	500	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	–	–	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 310 \mu\text{A}$	2.0	3.2	4.0	V
$R_{DS(on)}$	Static Drain to Source On–Resistance	$V_{GS} = 10 \text{ V}, I_D = 100 \text{ A}$	–	4.0	4.5	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 5 \text{ V}, I_D = 100 \text{ A}$	–	134	–	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	–	3615	5065	pF
$C_{oss}$	Output Capacitance		–	2330	3265	pF
$C_{rss}$	Reverse Transfer Capacitance		–	18	35	pF
$R_g$	Gate Resistance		0.1	1.1	2.2	S

### Switching Characteristics

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 50 \text{ V}, I_D = 100 \text{ A}, V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	–	29	47	ns
$t_r$	Rise Time		–	49	79	ns
$t_{d(off)}$	Turn–Off Delay Time		–	41	66	ns
$t_f$	Fall Time		–	13	24	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}, V_{DD} = 50 \text{ V}, I_D = 100 \text{ A}$	–	48	68	nC
$Q_{gs}$	Gate to Source Gate Charge		–	19	–	nC
$Q_{gd}$	Gate to Drain “Miller” Charge		–	9	–	nC
$Q_{oss}$	Output Charge	$V_{DD} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	–	150	–	nC

# FDP4D5N10C,

## ELECTRICAL CHARACTERISTICS (continued) ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Drain-Source Diode Characteristics</b>						
$I_S$	Maximum Continuous Drain to Source Diode Forward Current		–	–	128	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		–	–	512	A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 100\text{ A}$	–	1.0	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 50\text{ V},$ $I_F = 100\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$	–	82	132	ns
$Q_{rr}$	Reverse Recovery Charge		–	106	170	nC
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, V_{DD} = 50\text{ V},$ $I_F = 100\text{ A}, dI_F/dt = 300\text{ A}/\mu\text{s}$	–	71	114	ns
$Q_{rr}$	Reverse Recovery Charge		–	258	413	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### NOTES:

1. Pulsed  $I_d$  please refer to Figure "Forward Bias Safe Operating Area" for more details.
2.  $E_{AS}$  of 486 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{ mH}$ ,  $I_{AS} = 18\text{ A}$ ,  $V_{DD} = 100\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 58\text{ A}$ .
3. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

**TYPICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted)

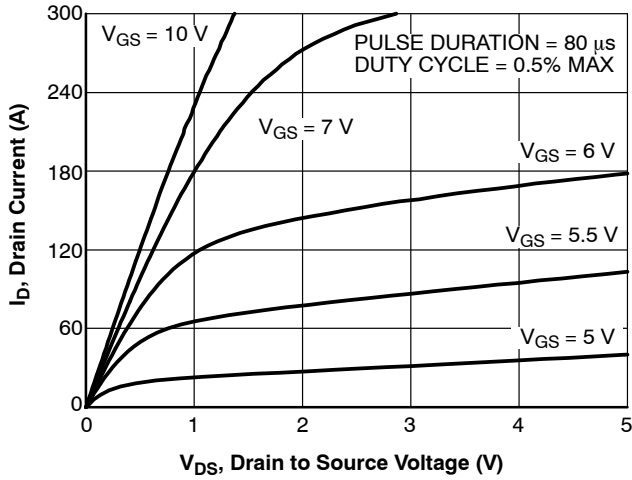


Figure 1. On-Region Characteristics

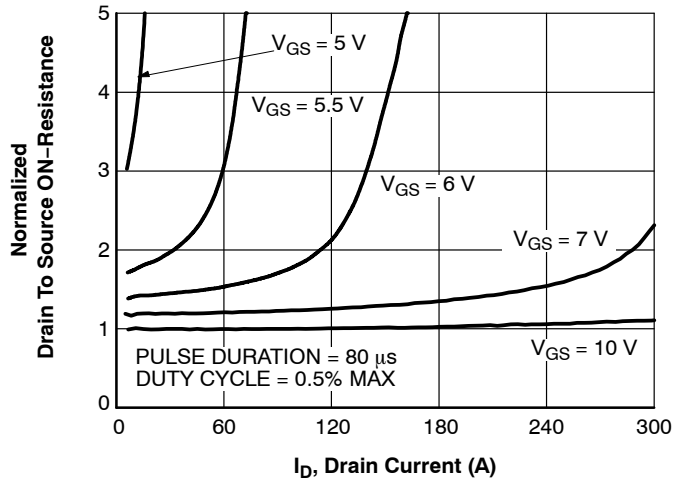


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

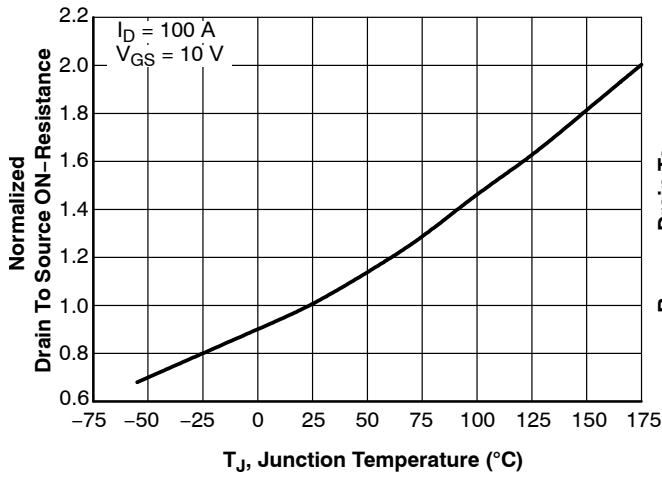


Figure 3. Normalized On Resistance vs. Junction Temperature

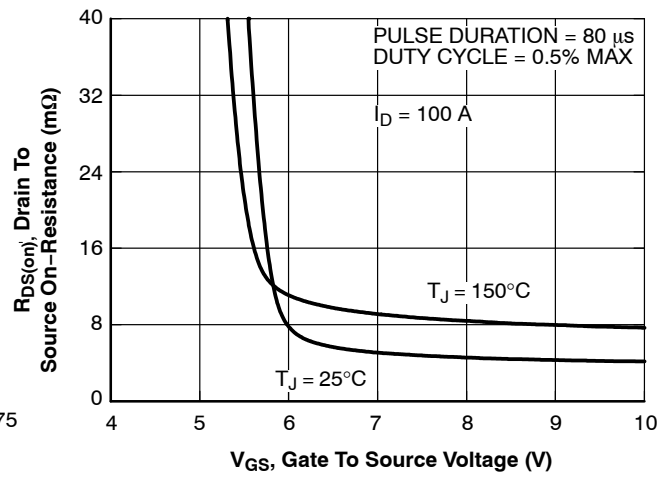


Figure 4. On-Resistance vs. Gate to Source Voltage

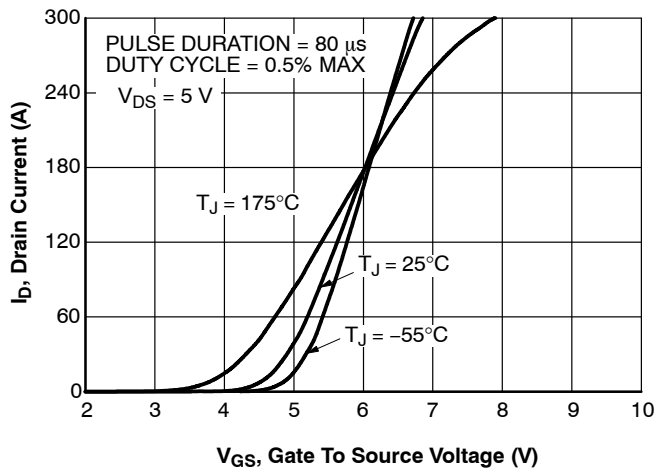


Figure 5. Transfer Characteristics

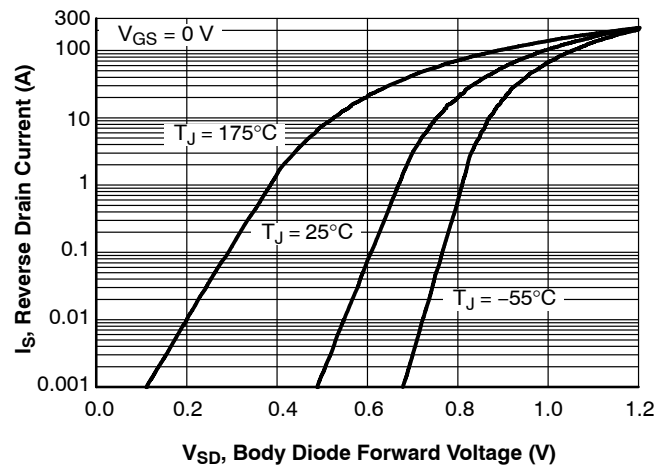


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

# FDP4D5N10C,

## TYPICAL CHARACTERISTICS (CONTINUED) ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

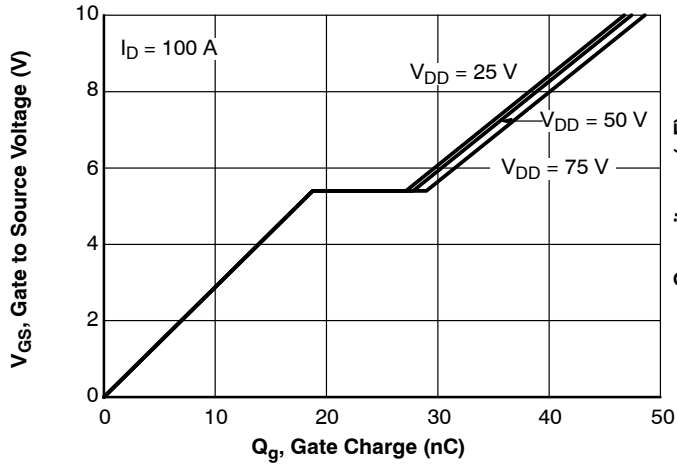


Figure 7. Gate Charge Characteristics

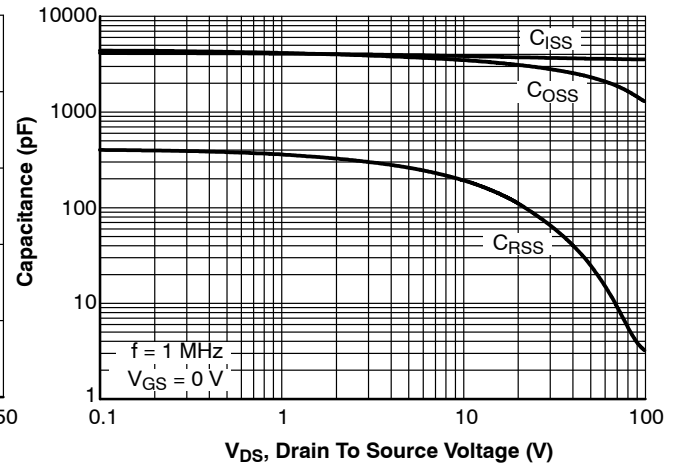


Figure 8. Capacitance vs Drain to Source Voltage

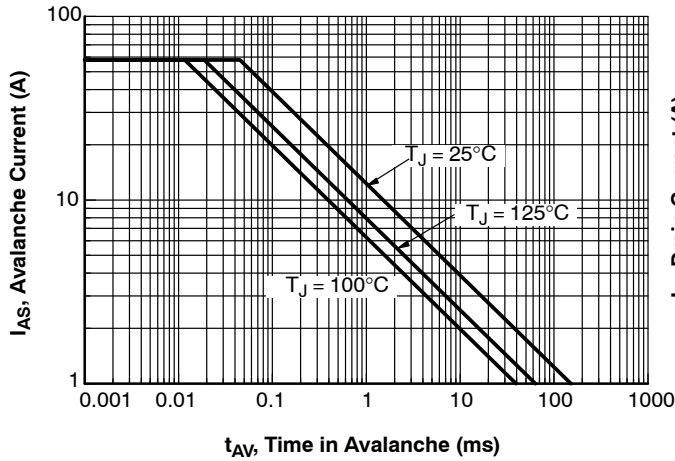


Figure 9. Unclamped Inductive Switching Capability

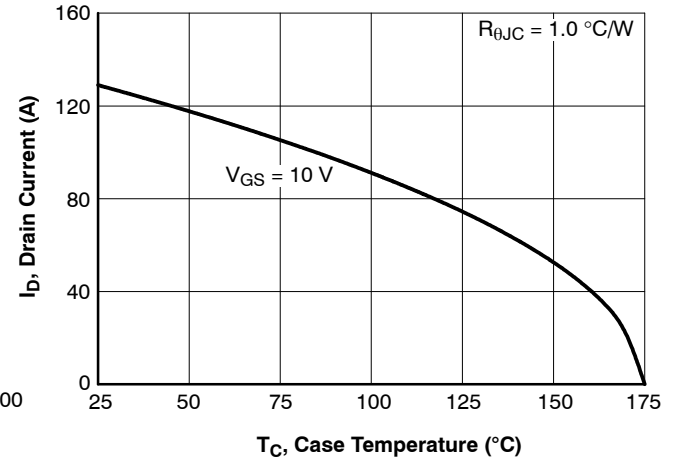


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

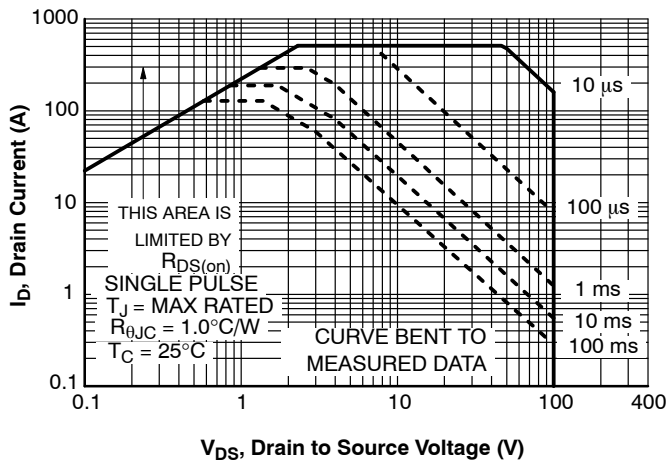


Figure 11. Forward Bias Safe Operating Area for FDP4D5N10C

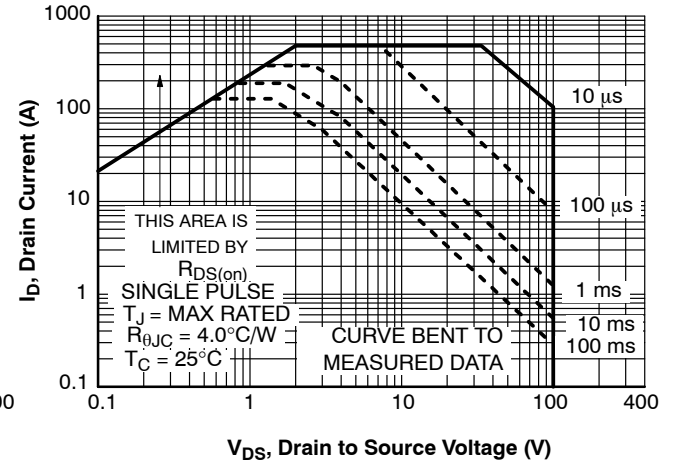


Figure 12. Forward Bias Safe Operating Area for FDP4D5N10C

# FDP4D5N10C,

## TYPICAL CHARACTERISTICS (CONTINUED) ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

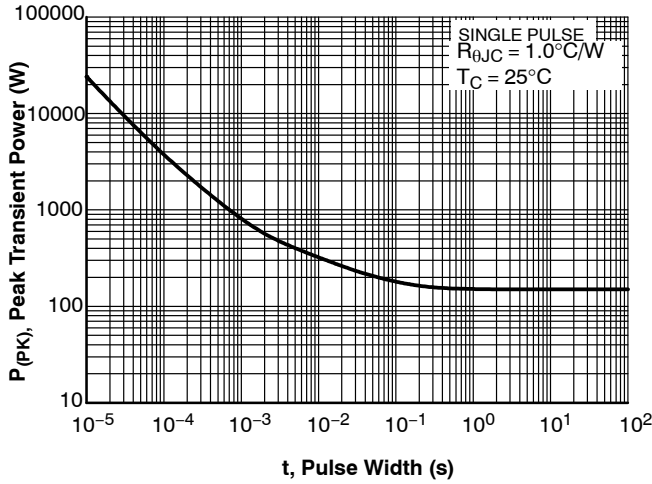


Figure 13. Single Pulse Maximum Power Dissipation for FDP4D5N10C

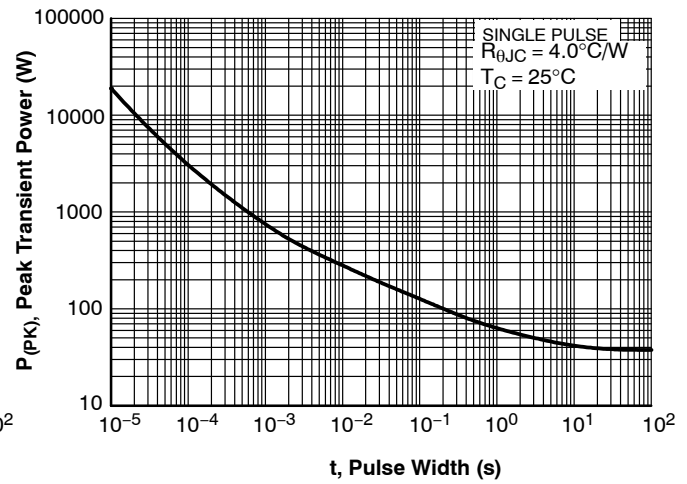


Figure 14. Single Pulse Maximum Power Dissipation for FDP4D5N10C

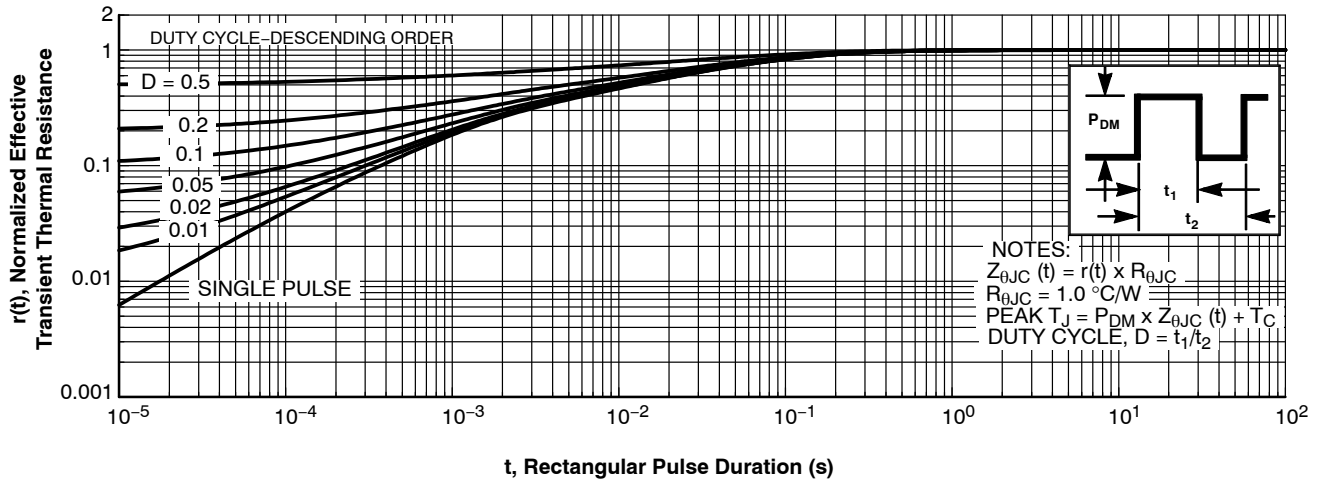


Figure 15. Junction-to-Case Transient Thermal Response Curve for FDP4D5N10C

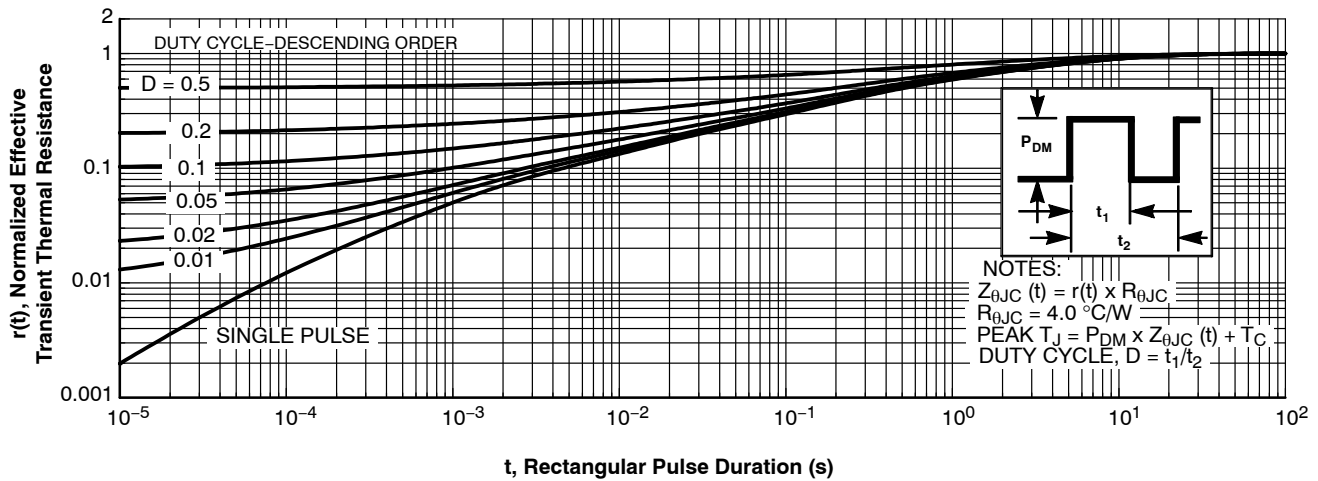
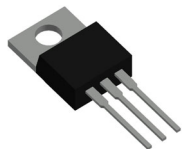


Figure 16. Junction-to-Case Transient Thermal Response Curve for FDP4D5N10C

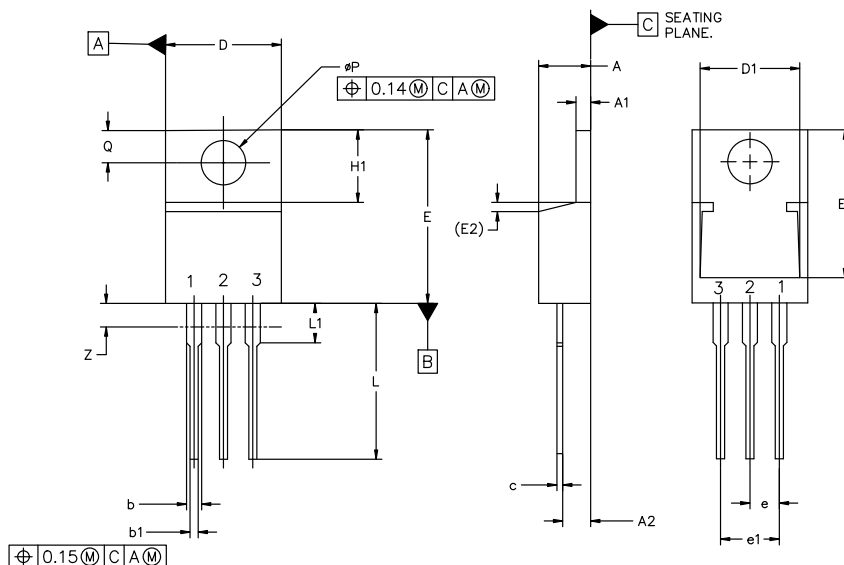


TO-220-3 10.10x15.12x4.45, 2.54P

CASE 221A

ISSUE AL

DATE 05 FEB 2025



MILLIMETERS			
DIM	MIN	NOM	MAX
A	4.07	4.45	4.83
A1	1.15	1.28	1.41
A2	2.04	2.42	2.79
b	1.15	1.34	1.52
b1	0.64	0.80	0.96
c	0.36	0.49	0.61
D	9.66	10.10	10.53
D1	8.43	8.63	8.83
E	14.48	15.12	15.75
E1	12.58	12.78	12.98
E2	1.27 REF		

MILLIMETERS			
DIM	MIN	NOM	MAX
e	2.42	2.54	2.66
e1	4.83	5.08	5.33
H1	5.97	6.22	6.47
L	12.70	13.49	14.27
L1	2.80	3.45	4.10
Q	2.54	2.79	3.04
øP	3.60	3.85	4.09
Z	---	---	3.48

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

STYLE 1:  
PIN 1. BASE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

STYLE 2:  
PIN 1. BASE  
2. EMITTER  
3. COLLECTOR  
4. EMITTER

STYLE 3:  
PIN 1. CATHODE  
2. ANODE  
3. GATE  
4. ANODE

STYLE 4:  
PIN 1. MAIN TERMINAL 1  
2. MAIN TERMINAL 2  
3. GATE  
4. MAIN TERMINAL 2

STYLE 5:  
PIN 1. GATE  
2. DRAIN  
3. SOURCE  
4. DRAIN

STYLE 6:  
PIN 1. ANODE  
2. CATHODE  
3. ANODE  
4. CATHODE

STYLE 7:  
PIN 1. CATHODE  
2. ANODE  
3. CATHODE  
4. ANODE

STYLE 8:  
PIN 1. CATHODE  
2. ANODE  
3. EXTERNAL TRIP/DELAY  
4. ANODE

STYLE 9:  
PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

STYLE 10:  
PIN 1. GATE  
2. SOURCE  
3. DRAIN  
4. SOURCE

STYLE 11:  
PIN 1. DRAIN  
2. SOURCE  
3. GATE  
4. SOURCE

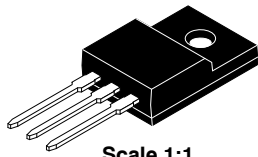
STYLE 12:  
PIN 1. MAIN TERMINAL 1  
2. MAIN TERMINAL 2  
3. GATE  
4. NOT CONNECTED

DOCUMENT NUMBER:	98ASB42148B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	TO-220-3 10.10x15.12x4.45, 2.54P	PAGE 1 OF 1

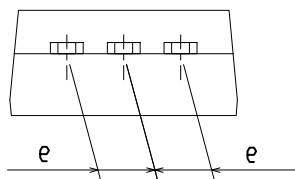
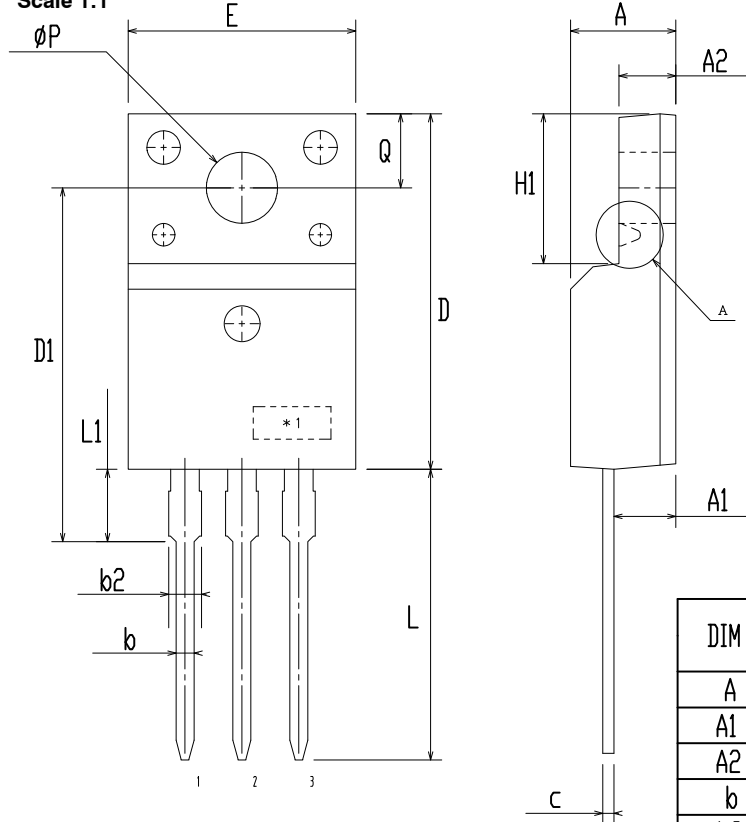
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**TO-220 Fullpack, 3-Lead / TO-220F-3SG**  
**CASE 221AT**  
**ISSUE B**

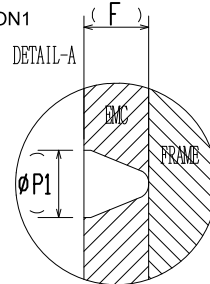
DATE 19 JAN 2021



Scale 1:1



OPTION1



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
Ø P	2.98	3.18	3.38
Ø P1	~	1.00	~
Q	3.20	3.30	3.40

**NOTES:**

A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009

B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCTIONS.

C. OPTION 1 - WITH SUPPORT PIN HOLE

OPTION 2 - NO SUPPORT PIN HOLE

<b>DOCUMENT NUMBER:</b>	<b>98AON67439E</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-220 FULLPACK, 3-LEAD / TO-220F-3SG</b>	<b>PAGE 1 OF 1</b>

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.



**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at  
[www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)