ON Semiconductor®
FDH3632 / FDP3632 / FDB3632
N-Channel PowerTrench® MOSFET
100 V, 80 A, 9 mΩ

Features
- $R_{DS(ON)} = 7.5$ mΩ (Typ.), $V_{GS} = 10$ V, $I_D = 80$ A
- $Q_g(tot) = 84$ nC (Typ.), $V_{GS} = 10$ V
- Low Miller Charge
- Low $Q_{rr}$, Body Diode
- UIS Capability (Single Pulse and Repetitive Pulse)
- RoHS Compliant

Applications
- Synchronous Rectification
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micro Solar Inverter

MOSFET Maximum Ratings $T_C = 25°C$ unless otherwise noted

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>$FDH3632 / FDP3632 / FDB3632$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSS}$</td>
<td>Drain to Source Voltage</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate to Source Voltage</td>
<td>$\pm 20$</td>
<td>V</td>
</tr>
</tbody>
</table>
| $I_D$ | Drain Current
Continuous ($T_C < 111°C, V_{GS} = 10$ V) | 80 | A |
| Continuous ($T_{amb} = 25°C, V_{GS} = 10$ V, $R_{JA} = 43°C/W$) | 12 | A |
| Pulsed | Figure 4 | A |
| $E_{AS}$ | Single Pulse Avalanche Energy (Note 1) | 337 | mJ |
| $P_D$ | Power dissipation | 310 | W |
| | Derate above 25°C | 2.07 | W/°C |
| $T_J, T_{STG}$ | Operating and Storage Temperature | -55 to 175 | °C |

Thermal Characteristics

| $R_{JUC}$ | Thermal Resistance Junction to Case, Max. TO-220, D²-PAK, TO-247 | 0.48 | °C/W |
| $R_{JUA}$ | Thermal Resistance Junction to Ambient, Max. TO-220 (Note 2) | 62 | °C/W |
| $R_{JUA}$ | Thermal Resistance Junction to Ambient D²-PAK, Max. 1in² copper pad area | 43 | °C/W |
| $R_{JUA}$ | Thermal Resistance Junction to Ambient, Max. TO-247 (Note 2) | 30 | °C/W |
## Package Marking and Ordering Information

<table>
<thead>
<tr>
<th>Device Marking</th>
<th>Device</th>
<th>Package</th>
<th>Reel Size</th>
<th>Tape Width</th>
<th>Quantity</th>
</tr>
</thead>
<tbody>
<tr>
<td>FDB3632</td>
<td>FDB3632</td>
<td>D²-PAK</td>
<td>330 mm</td>
<td>24 mm</td>
<td>800 units</td>
</tr>
<tr>
<td>FDP3632</td>
<td>FDP3632</td>
<td>TO-220</td>
<td>Tube</td>
<td>N/A</td>
<td>50 units</td>
</tr>
<tr>
<td>FDH3632</td>
<td>FDH3632</td>
<td>TO-247</td>
<td>Tube</td>
<td>N/A</td>
<td>30 units</td>
</tr>
</tbody>
</table>

## Electrical Characteristics \( T_c = 25^\circ C \) unless otherwise noted

### Off Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{B,DSS} )</td>
<td>Drain to Source Breakdown Voltage</td>
<td>( I_D = 250\mu A, V_{GS} = 0V )</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td>V</td>
</tr>
<tr>
<td>( I_{DSS} )</td>
<td>Zero Gate Voltage Drain Current</td>
<td>( V_{DS} = 80V )</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{GSS} )</td>
<td>Gate to Source Leakage Current</td>
<td>(</td>
<td>V_{GS}</td>
<td>= 20V )</td>
<td>-</td>
<td>-</td>
</tr>
</tbody>
</table>

### On Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{GS,(TH)} )</td>
<td>Gate to Source Threshold Voltage</td>
<td>( V_{GS} = V_{DS}, I_D = 250\mu A )</td>
<td>2</td>
<td>-</td>
<td>4</td>
<td>V</td>
</tr>
<tr>
<td>( r_{D,(ON)} )</td>
<td>Drain to Source On Resistance</td>
<td>( I_D = 80A, V_{GS} = 10V )</td>
<td>-</td>
<td>0.0075</td>
<td>0.009</td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td>( I_D = 40A, V_{GS} = 6V )</td>
<td>-</td>
<td>0.009</td>
<td>0.015</td>
<td>( \Omega )</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( I_D = 80A, V_{GS} = 10V, T_c = 175^\circ C )</td>
<td>-</td>
<td>0.018</td>
<td>0.022</td>
<td>( \Omega )</td>
<td></td>
</tr>
</tbody>
</table>

### Dynamic Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( C_{DSS} )</td>
<td>Input Capacitance</td>
<td>( V_{DS} = 25V, V_{GS} = 0V ), ( f = 1MHz )</td>
<td>-</td>
<td>6000</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>( C_{DSS} )</td>
<td>Output Capacitance</td>
<td>( V_{DS} = 25V, V_{GS} = 0V ), ( f = 1MHz )</td>
<td>-</td>
<td>820</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>( C_{RSS} )</td>
<td>Reverse Transfer Capacitance</td>
<td>( T_c = 150^\circ C )</td>
<td>-</td>
<td>200</td>
<td>-</td>
<td>pF</td>
</tr>
<tr>
<td>( Q_{g,(TOT)} )</td>
<td>Total Gate Charge at 10V</td>
<td>( V_{GS} = 0V ) to ( V_{DD} = 50V )</td>
<td>-</td>
<td>84</td>
<td>110</td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{g,(TH)} )</td>
<td>Threshold Gate Charge</td>
<td>( V_{GS} = 0V ) to ( 2V )</td>
<td>-</td>
<td>11</td>
<td>14</td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gs} )</td>
<td>Gate to Source Gate Charge</td>
<td>( I_D = 80A )</td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gs2} )</td>
<td>Gate Charge Threshold to Plateau</td>
<td>( I_g = 1.0mA )</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gd} )</td>
<td>Gate to Drain “Miller” Charge</td>
<td>( I_D = 80A )</td>
<td>-</td>
<td>20</td>
<td>-</td>
<td>nC</td>
</tr>
</tbody>
</table>

### Resistive Switching Characteristics \( V_{GS} = 10V \)

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( I_{ON} )</td>
<td>Turn-On Time</td>
<td>( V_{DD} = 50V, I_D = 80A )</td>
<td>-</td>
<td>-</td>
<td>102</td>
<td>ns</td>
</tr>
<tr>
<td>( I_{ON,(th)} )</td>
<td>Turn-On Delay Time</td>
<td>( V_{GS} = 10V, R_{GS} = 3.6\Omega )</td>
<td>-</td>
<td>30</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_r )</td>
<td>Rise Time</td>
<td>( V_{DD} = 50V, I_D = 80A )</td>
<td>-</td>
<td>39</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_{(OFF)} )</td>
<td>Turn-Off Delay Time</td>
<td>( V_{GS} = 10V, R_{GS} = 3.6\Omega )</td>
<td>-</td>
<td>96</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( t_f )</td>
<td>Fall Time</td>
<td>( I_D )</td>
<td>-</td>
<td>46</td>
<td>-</td>
<td>ns</td>
</tr>
<tr>
<td>( I_{OFF} )</td>
<td>Turn-Off Time</td>
<td>( I_D )</td>
<td>-</td>
<td>213</td>
<td>-</td>
<td>ns</td>
</tr>
</tbody>
</table>

### Drain-Source Diode Characteristics

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Test Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{SD} )</td>
<td>Source to Drain Diode Voltage</td>
<td>( I_{SD} = 80A )</td>
<td>-</td>
<td>-</td>
<td>1.25</td>
<td>V</td>
</tr>
<tr>
<td>( I_{rr} )</td>
<td>Reverse Recovery Time</td>
<td>( I_{SD} = 75A, dI_{SD}/dt = 100A/\mu s )</td>
<td>-</td>
<td>-</td>
<td>64</td>
<td>ns</td>
</tr>
<tr>
<td>( Q_{RR} )</td>
<td>Reverse Recovered Charge</td>
<td>( I_{SD} = 75A, dI_{SD}/dt = 100A/\mu s )</td>
<td>-</td>
<td>-</td>
<td>120</td>
<td>nC</td>
</tr>
</tbody>
</table>

**Notes:**

1: Starting \( T_c = 25^\circ C, L = 0.12mH, I_{AS} = 75A, V_{DD} = 80V \).
2: Pulse Width = 100s
Typical Characteristics \( T_C = 25^\circ C \) unless otherwise noted

Figure 1. Normalized Power Dissipation vs Ambient Temperature

Figure 2. Maximum Continuous Drain Current vs Case Temperature

Figure 3. Normalized Maximum Transient Thermal Impedance

Figure 4. Peak Current Capability
Typical Characteristics  $T_C = 25^\circ\text{C}$ unless otherwise noted

![Diagram](image1)

**Figure 5. Forward Bias Safe Operating Area**

![Diagram](image2)

**Figure 6. Unclamped Inductive Switching Capability**

![Diagram](image3)

**Figure 7. Transfer Characteristics**

![Diagram](image4)

**Figure 8. Saturation Characteristics**

![Diagram](image5)

**Figure 9. Drain to Source On Resistance vs Drain Current**

![Diagram](image6)

**Figure 10. Normalized Drain to Source On Resistance vs Junction Temperature**

NOTE: Refer to ON Semiconductor Application Notes AN7514 and AN7515
Typical Characteristics $T_C = 25^\circ C$ unless otherwise noted

**Figure 11.** Normalized Gate Threshold Voltage vs Junction Temperature

**Figure 12.** Normalized Drain to Source Breakdown Voltage vs Junction Temperature

**Figure 13.** Capacitance vs Drain to Source Voltage

**Figure 14.** Gate Charge Waveforms for Constant Gate Currents
Test Circuits and Waveforms

Figure 15. Unclamped Energy Test Circuit

Figure 16. Unclamped Energy Waveforms

Figure 17. Gate Charge Test Circuit

Figure 18. Gate Charge Waveforms

Figure 19. Switching Time Test Circuit

Figure 20. Switching Time Waveforms
**Thermal Resistance vs. Mounting Pad Area**

The maximum rated junction temperature, $T_{JM}$, and the thermal resistance of the heat dissipating path determine the maximum allowable device power dissipation, $P_{DM}$, in an application. Therefore the application’s ambient temperature, $T_A$ (°C), and thermal resistance $R_{θJA}$ (°C/W) must be reviewed to ensure that $T_{JM}$ is never exceeded.

Equation 1 mathematically represents the relationship and serves as the basis for establishing the rating of the part.

$$P_{DM} = \frac{(T_{JM} - T_A)}{R_{θJA}}$$  \hspace{1cm} (EQ. 1)

In using surface mount devices such as the TO-263 package, the environment in which it is applied will have a significant influence on the part’s current and maximum power dissipation ratings. Precise determination of $P_{DM}$ is complex and influenced by many factors:

1. Mounting pad area onto which the device is attached and whether there is copper on one side or both sides of the board.
2. The number of copper layers and the thickness of the board.
3. The use of external heat sinks.
4. The use of thermal vias.
5. Air flow and board orientation.
6. For non steady state applications, the pulse width, the duty cycle and the transient thermal response of the part, the board and the environment they are in.

ON Semiconductor provides thermal information to assist the designer’s preliminary application evaluation. Figure 21 defines the $R_{θJA}$ for the device as a function of the top copper (component side) area. This is for a horizontally positioned FR-4 board with 1oz copper after 1000 seconds of steady state power with no air flow. This graph provides the necessary information for calculation of the steady state junction temperature or power dissipation. Pulse applications can be evaluated using the ON Semiconductor device Spice thermal model or manually utilizing the normalized maximum transient thermal impedance curve.

Thermal resistances corresponding to other copper areas can be obtained from Figure 21 or by calculation using Equation 2 or 3. Equation 2 is used for copper area defined in inches square and equation 3 is for area in centimeter square. The area, in square inches or square centimeters is the top copper area including the gate and source pads.

$$R_{θJA} = 26.51 + \frac{19.84}{(0.262 + \text{Area})}$$  \hspace{1cm} (EQ. 2)

Area in Inches Squared

$$R_{θJA} = 26.51 + \frac{128}{(1.69 + \text{Area})}$$  \hspace{1cm} (EQ. 3)

Area in Centimeter Squared

---

**Figure 21. Thermal Resistance vs Mounting Pad Area**

- $R_{θJA} = 26.51 + 19.84/(0.262 + \text{Area})$  \hspace{1cm} (EQ. 2)
- $R_{θJA} = 26.51 + 128/(1.69 + \text{Area})$  \hspace{1cm} (EQ. 3)

- AREA, TOP COPPER AREA in² (cm²)
PSPICE Electrical Model

.SUBCKT FDB3632 2 1 3 ;  rev May 2002
CA 12 8 1.7e-9
Cb 15 14 2.5e-9
Cin 6 8 6.0e-9
Dbody 7 5 DbodyMOD
Dbreak 11 5 DbreakMOD
Dplcap 10 5 DplcapMOD
Ebreak 11 7 17 18 10 2.5
Eds 14 8 6 1
Egs 13 6 6 1
Evthres 6 21 19 8 1
Evtemp 20 6 18 22 1
It 5 17 1
Lgate 1 9 5.61e-9
Ldrain 2 5 10
Lsource 3 7 2.7e-9
RLgate 1 9 56.1
RLdrain 2 5 10
RLsource 3 7 27
Mmed 16 6 8 8 MmedMOD
Mstro 16 6 8 8 MstroMOD
Mweak 16 21 8 8 MweakMOD
Rbreak 17 18 RbreakMOD 1
Rdrain 50 16 RdrainMOD 3.8e-3
Rgate 9 20 1.1
RSLC1 5 51 RSLC1MOD 1.0e-6
RSLC2 5 50 1.0e3
Rsource 8 7 RsourceMOD 2.5e-3
Rvthres 22 8 RvthresMOD 1
Rvtemp 18 19 RvtempMOD 1
S1a 6 12 13 8 S1AMOD
S1b 13 12 13 8 S1BMOD
S2a 6 15 14 13 S2AMOD
S2b 13 15 14 13 S2BMOD
Vbat 22 19 DC 1
VL = 5.1 50 VALUE=((V(5,51)/ABS(V(5,51)))* (PWR(V(5,51)/(1e-6*350),3)))
.MODEL DbodyMOD D (IS=5.9e-11 N=1.07 RS=2.3e-3 TRS1=3.0e-3 TRS2=1.0e-6 + CJO=4e-9 M=0.59 TT=4.8e-8 XTI=4.2)
.MODEL DbreakMOD D (RS=0.17 TRS1=3.0e-3 TRS2=-8.9e-6)
.MODEL DplcapMOD D (CJO=15e-10 IS=1.0e-30 N=10 M=0.6)
.MODEL MmedMOD NMOS (VTO=4.1 KP=200 IS=1e-30 N=10 TOX=1 L=1u W=1u)
.MODEL MstroMOD NMOS (VTO=3.4 KP=10.0 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.1)
.MODEL MweakMOD NMOS (VTO=2.75 KP=0.05 IS=1e-30 N=10 TOX=1 L=1u W=1u RG=1.1e+1 RS=0.1)
.MODEL RbreakMOD RES (TC1=1.0e-3 TC2=1.7e-6)
.MODEL RdrainMOD RES (TC1=8.5e-3 TC2=2.8e-5)
.MODEL RSLC1MOD RES (TC1=2.0e-3 TC2=2.0e-6)
.MODEL RsourceMOD RES (TC1=4e-3 TC2=1e-6)
.MODEL RvthresMOD RES (TC1=4.0e-3 TC2=1.8e-5)
.MODEL RvtempMOD RES (TC1=4.4e-3 TC2=2.2e-6)
.MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 VNOFF=4 VOFF=2)
.MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 VNOFF=2 VOFF=4)
.MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 VNOFF=0.8 VOFF=-0.4)
.MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 VNOFF=0.4 VOFF=-0.8)
.ENDS

SABER Electrical Model

REV May 2002

template FDB3632 n2,n1,n3

electrical n2,n1,n3

\{ 
  var i iscl

  dp..model dbodymod = (isl=5.9e-11, nl=1.07, rs=2.3e-3, trs1=3.0e-3, trs2=1.0e-6, cijo=4e-9, m=0.58, tt=4.8e-8, xti=4.2)
  dp..model dbreakmod = (rs=0.17, trs1=3.0e-3, trs2=8.9e-6)
  dp..model dplcapmod = (cijo=15e-9, isl=10.0e-30, nl=10, m=0.6)
  m..model mstrongmod = (type=, vto=4.1, kp=200, is=1e-30, tox=1)
  m..model mmweakmod = (type=, vto=3.4, kp=0.05, is=1e-30, tox=0.1)
  sw_vcsp..model s1amod = (ron=1e-5, roff=0.1, von=1, voff=2)
  sw_vcsp..model s2amod = (ron=1e-5, roff=0.1, von=2, voff=4)
  sw_vcsp..model s2bmod = (ron=1e-5, roff=0.1, von=4, voff=8)

  c.ca n12 n8 = 1.7e-9
  c.cb n15 n14 = 2.5e-9
  c.cin n8 n8 = 6.0e-9

  dp..model dbody n7 n5 = model=dbodymod
  dp..model dbreak n5 n11 = model=dbreakmod
  dp..model dplcap n10 n5 = model=dplcapmod

  spe.ebreak n11 n7 n17 n18 = 102.5
  spe.ebreak n11 n7 n17 n18 = 102.5
  spe.ebreak n11 n7 n17 n18 = 102.5
  spe.ebreak n11 n7 n17 n18 = 102.5

  i.it n8 n17 = 1

  l.lgate n1 n9 = 5.61e-9
  l.ldrain n2 n5 = 1.0e-9
  l.lsourc e n3 n7 = 2.7e-9

  res.rigate n1 n9 = 56.1
  res.rdrain n2 n5 = 10
  res.rsource n3 n7 = 27

  m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
  m.mweak n16 n6 n8 n8 = model=mweakmod, l=1u, w=1u
  m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u

  res.rbreak n17 n18 = 1, tc1=1.0e-3, tc2=1.7e-6
  res.rdrain n50 n16 = 3.8e-3, tc1=8.5e-3, tc2=2.8e-5
  res.rigate n9 n20 = 1.1
  res.rslc1 n51 n50 = 1.0e6, tc1=2.0e-3, tc2=2.0e-6
  res.rslc2 n50 n50 = 1.0e3
  res.rsource n8 n7 = 2.5e-3, tc1=4e-3, tc2=1.0e-6
  res.rvtheres n22 n8 = 1, tc1=1.8e-3, tc2=1.8e-5
  res.rvtemp n18 n19 = 1, tc1=1.0e-3, tc2=2.2e-6
  sw_vcsp..model s1a n6 n12 n13 n8 = model=n1amod
  sw_vcsp..model s2a n6 n12 n13 n8 = model=n2amod
  sw_vcsp..model s2b n6 n12 n13 n8 = model=n2bmod
  sw_vcsp..model s2b n6 n12 n13 n8 = model=n2bmod

v.vbat n22 n19 = dc=1

equations { 
  i(n51->n50) += iscl
  iscl: v(n51,n51) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*(abs(v(n5,n51)*1e6/350)** 3)) } 
\}
**SPICE Thermal Model**

REV May 2002

FDB3632

CTHERM1 TH 6 7.5e-3
CTHERM2 6 5 8.0e-3
CTHERM3 5 4 9.0e-3
CTHERM4 4 3 2.4e-2
CTHERM5 3 2 3.4e-2
CTHERM6 2 TL 6.5e-2

RTERM1 TH 6 3.1e-4
RTERM2 6 5 2.5e-3
RTERM3 5 4 2.2e-2
RTERM4 4 3 8.1e-2
RTERM5 3 2 1.35e-1
RTERM6 2 TL 1.5e-1

**SABER Thermal Model**

SABER thermal model FDB3632
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 =7.5e-3
ctherm.ctherm2 6 5 =8.0e-3
ctherm.ctherm3 5 4 =9.0e-3
ctherm.ctherm4 4 3 =2.4e-2
ctherm.ctherm5 3 2 =3.4e-2
ctherm.ctherm6 2 tl =6.5e-2

ctherm.rtherm1 th 6 =3.1e-4
ctherm.rtherm2 6 5 =2.5e-3
ctherm.rtherm3 5 4 =2.2e-2
ctherm.rtherm4 4 3 =8.1e-2
ctherm.rtherm5 3 2 =1.35e-1
ctherm.rtherm6 2 tl =1.5e-1
}

www.onsemi.com
Figure 22. TO-247, Molded, 3 Lead, Jedec Variation AB

Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.
Mechanical Dimensions

Figure 23. TO-220, Molded, 3Lead, Jedeck Variation AB

Package drawings are provided as a service to customers considering ON Semiconductor components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact an ON Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of ON Semiconductor worldwide terms and conditions, specifically the warranty therein, which covers ON Semiconductor products.
Figure 24. 2LD, TO263, Surface Mount

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