

MOSFET – Dual, N-Channel, POWERTRENCH®

20 V, 3.8 A, 66 mΩ

FDME1024N2T

Description

This Device is Designed Specifically as a Single Package Solution for Dual Switching Requirement in cellular handset and other Ultra-Portable Applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses.

The MicroFET™ 1.6x1.6 Thin package offers Exceptional Thermal Performance for it's physical size and is well suited to switching and linear mode applications.

Features

- Max $R_{DS(on)}$ = 66 mΩ at $V_{GS} = 4.5$ V, $I_D = 3.4$ A
- Max $R_{DS(on)}$ = 86 mΩ at $V_{GS} = 2.5$ V, $I_D = 2.9$ A
- Max $R_{DS(on)}$ = 113 mΩ at $V_{GS} = 1.8$ V, $I_D = 2.5$ A
- Max $R_{DS(on)}$ = 160 mΩ at $V_{GS} = 1.5$ V, $I_D = 2.1$ A
- Low Profile 0.55 mm Maximum – in the New Package MicroFET 1.6x1.6 Thin
- Free From Halogenated Compounds and Antimony Oxides
- HBM ESD Protection Level > 1600 V (Note 3)
- These Devices is Pb-Free, Halide Free and is RoHS Compliant

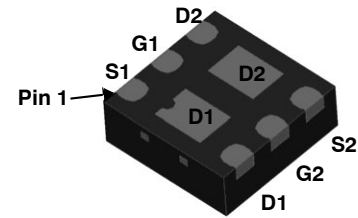
Typical Applications

- Baseband Switch
- Load Switch

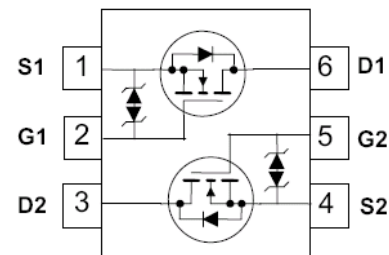
ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	± 8	V
I_D	Drain Current $T_A = 25^\circ\text{C}$ – Continuous (Note 1a) – Pulsed	3.8 6	A
P_D	Power Dissipation Single Operation $T_A = 25^\circ\text{C}$ (Note 1a)	1.4	W
	Power Dissipation Single Operation $T_A = 25^\circ\text{C}$ (Note 1b)	0.6	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	-55 to $+150$	$^\circ\text{C}$

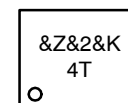
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



MicroFET
UDFN6 1.6X1.6, 0.5P
CASE 517DW



MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2-Digit Date-Code (Year & Week)
- &K = 2-Digit Lot Traceability Code
- 4T = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDME1024N2T	UDFN-6 (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FDME1024N2T

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance for, Junction to Ambient (Single Operation) (Note 1a)	90	°C/W
$R_{\theta JA}$	Thermal Resistance for, Junction to Ambient (Single Operation) (Note 1b)	195	°C/W

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	20	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	16	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	–3	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\ \text{V}$, $I_D = 3.4\ \text{A}$ $V_{GS} = 2.5\ \text{V}$, $I_D = 2.9\ \text{A}$, $V_{GS} = 1.8\ \text{V}$, $I_D = 2.5\ \text{A}$, $V_{GS} = 1.5\ \text{V}$, $I_D = 2.1\ \text{A}$, $V_{GS} = 4.5\ \text{V}$, $I_D = 3.4\ \text{A}$, $T_J = 125^\circ\text{C}$	– – – – –	55 68 85 106 76	66 86 113 160 112	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 4.5\ \text{V}$, $I_D = 3.4\ \text{A}$	–	9	–	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	225	300	pF
C_{oss}	Output Capacitance		–	40	55	pF
C_{rss}	Reverse Transfer Capacitance		–	25	40	pF

Switching Characteristics

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\ \text{V}$, $I_D = 1\ \text{A}$, $V_{GS} = 4.5\ \text{V}$, $R_{GEN} = 6\ \Omega$	–	4.5	10	ns
t_r	Rise Time		–	2	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	15	27	ns
t_f	Fall Time		–	1.7	10	ns
Q_g	Total Gate Charge	$V_{DD} = 10\ \text{V}$, $I_D = 3.4\ \text{A}$, $V_{GS} = 4.5\ \text{V}$	–	3	4.2	nC
Q_{gs}	Gate to Source Gate Charge		–	0.4	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	0.6	–	nC

Drain–Source Diode Characteristics and Maximum Ratings

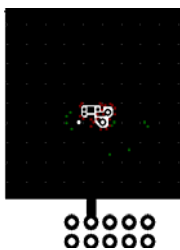
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}$, $I_S = 0.9\ \text{A}$ (Note 2)	–	0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 3.4\ \text{A}$, $di/dt = 100\ \text{A}/\mu\text{s}$	–	8.5	17	ns
Q_{rr}	Reverse Recovery Charge		–	1.4	10	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

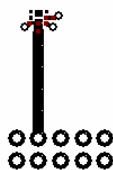
FDME1024NZT

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a).90 °C/W when mounted on
a 1 in² pad of 2 oz copper.



b).195 °C/W when mounted on a
minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2.0\%$
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

TYPICAL CHARACTERISTICS $T_C = 25^\circ\text{C}$ unless otherwise noted

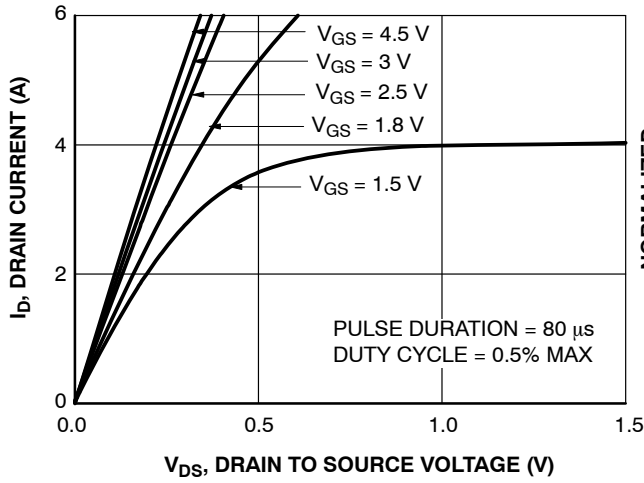


Figure 1. On-Region Characteristics

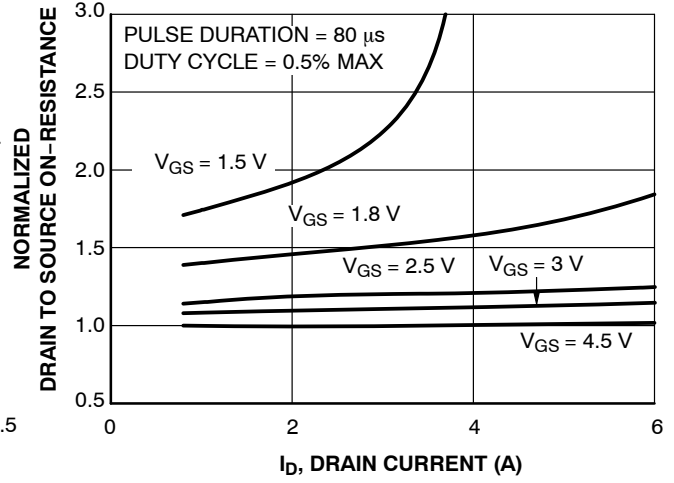


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

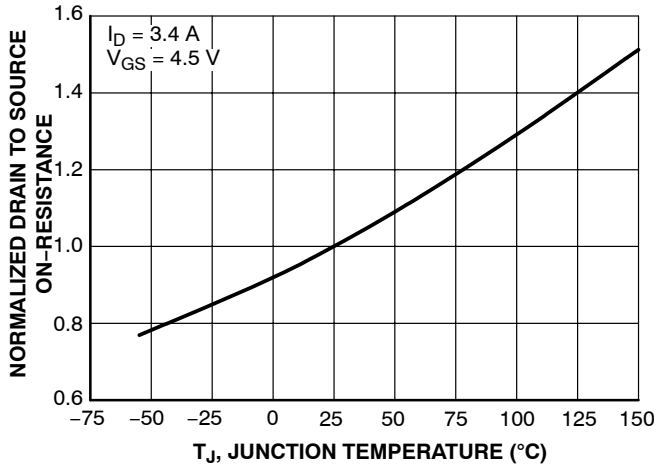


Figure 3. Normalized On-Resistance vs. Junction Temperature

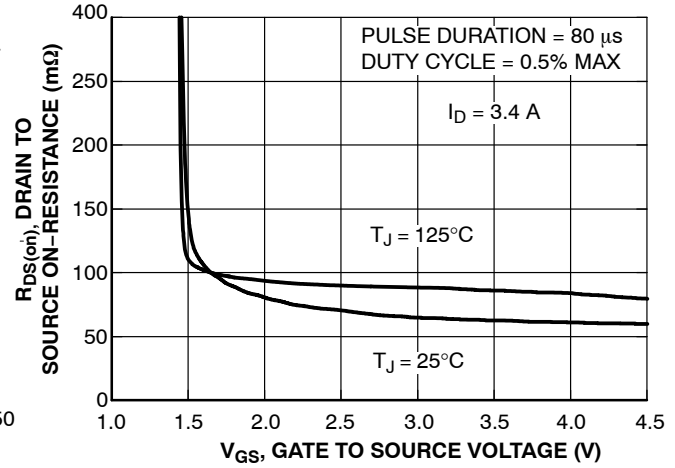


Figure 4. On-Resistance vs. Gate to Source Voltage

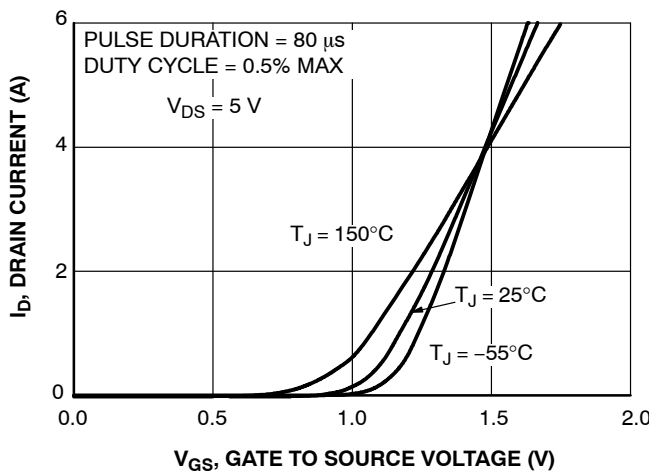


Figure 5. Transfer Characteristics

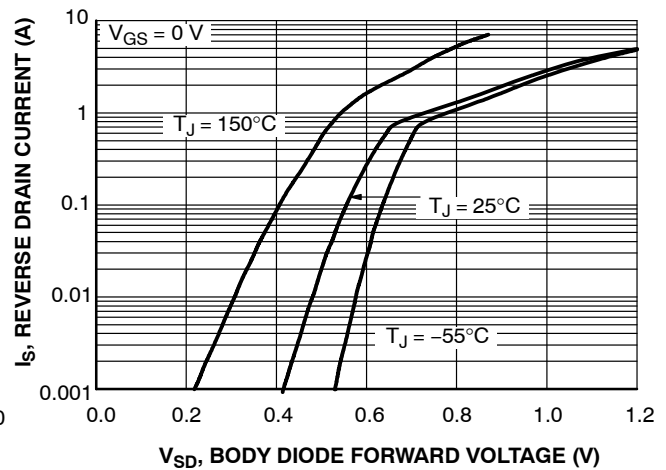


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS $T_C = 25^\circ\text{C}$ unless otherwise noted (CONTINUED)

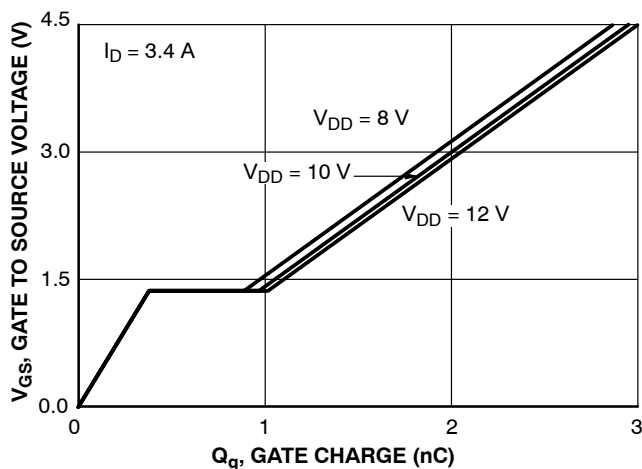


Figure 7. Gate Charge Characteristics

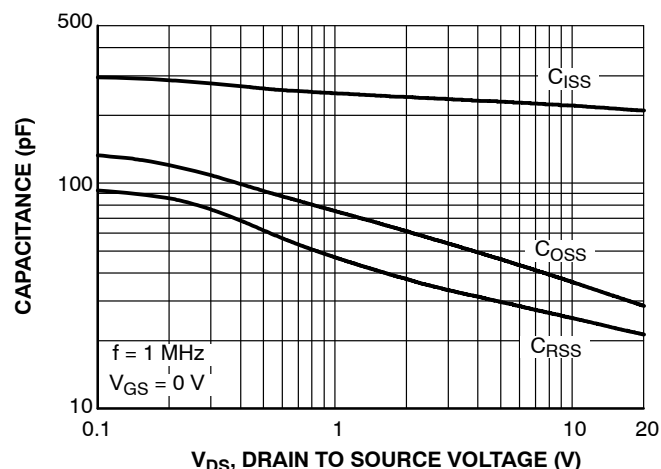


Figure 8. Capacitance vs Drain to Source Voltage

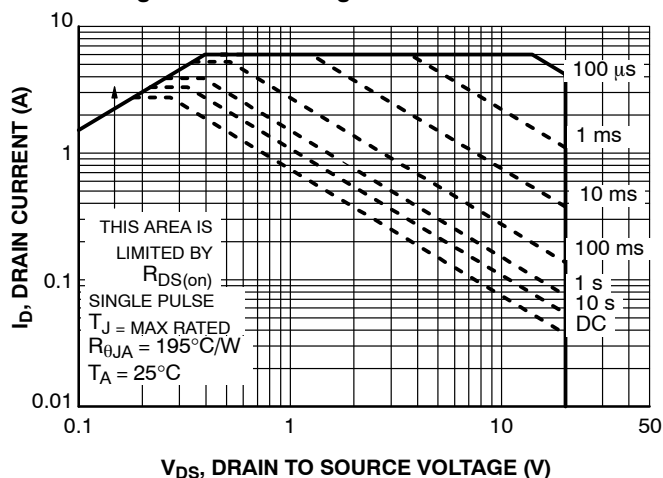


Figure 9. Forward Bias Safe Operating Area

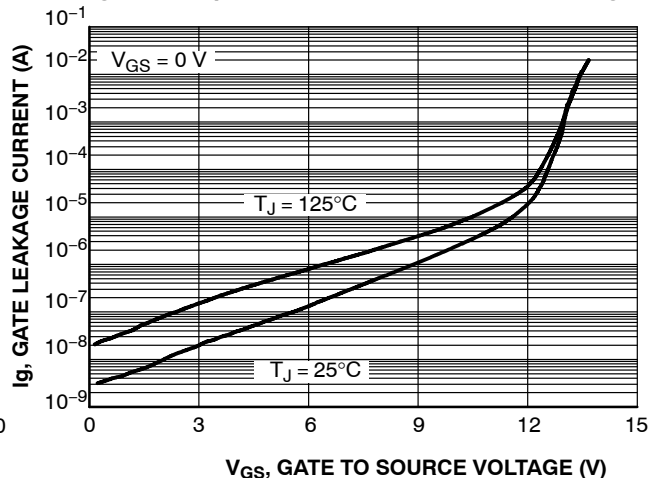


Figure 10. Gate Leakage Current vs Gate to Source Voltage

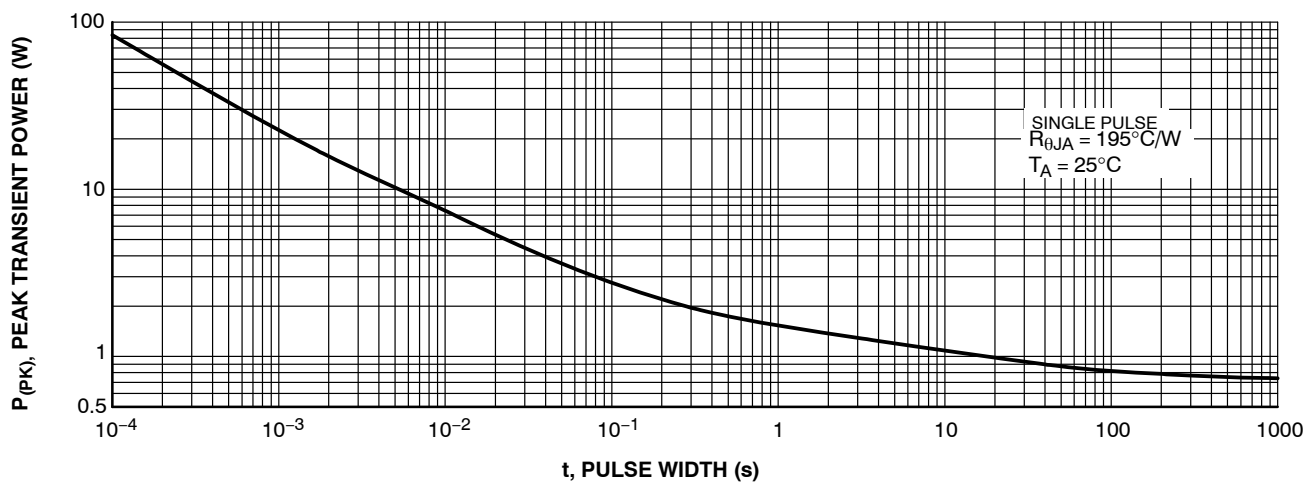


Figure 11. Single Pulse Maximum Power Dissipation

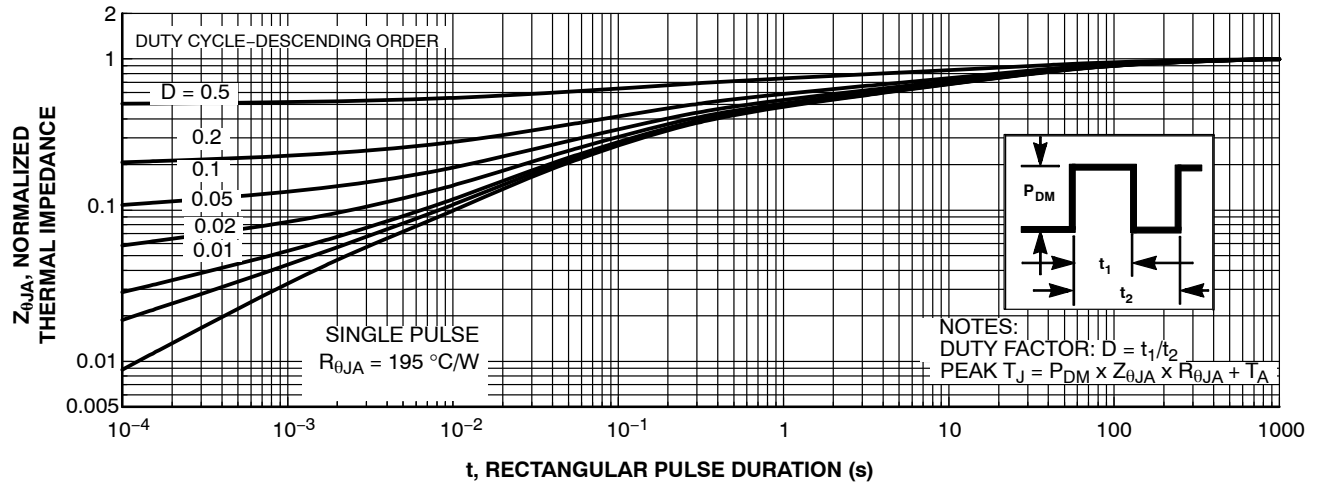
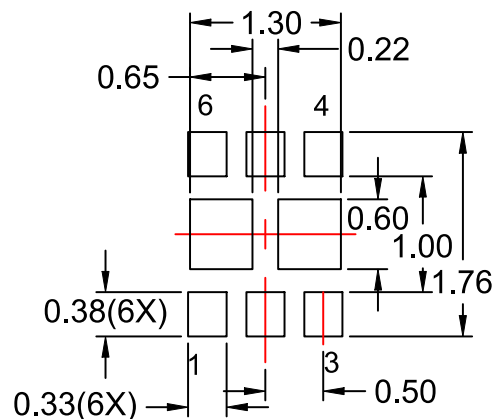
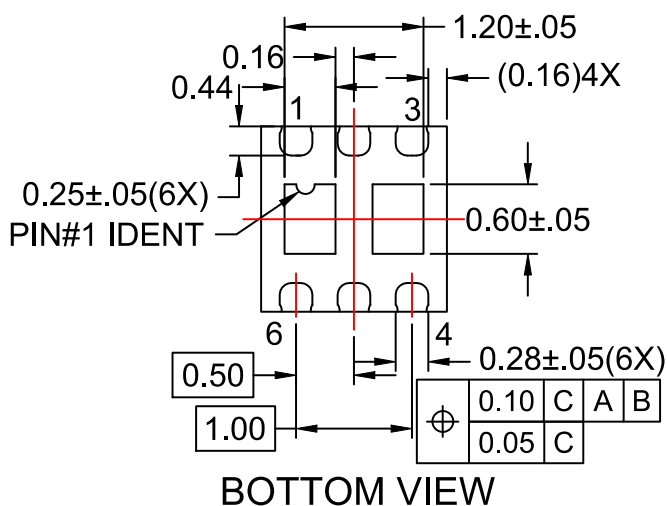
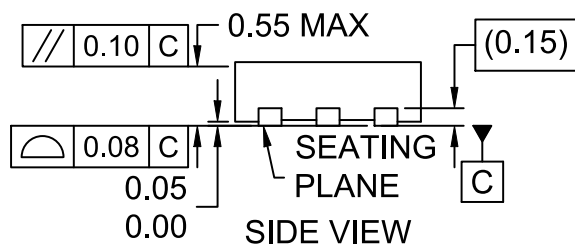
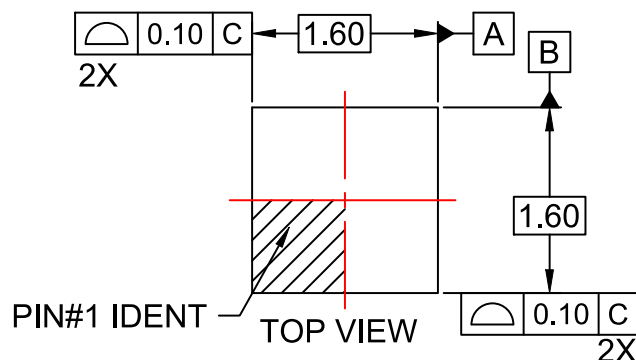
TYPICAL CHARACTERISTICS $T_C = 25^\circ\text{C}$ unless otherwise noted (CONTINUED)

Figure 12. Junction-to-Ambient Transient Thermal Response Curve

UDFN6 1.6x1.6, 0.5P
CASE 517DW
ISSUE 0

DATE 31 OCT 2016



RECOMMENDED LAND PATTERN

NOTES:

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- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
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