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FDMC7664

June 2014

N-Channel PowerTrench[®] MOSFET 30 V, 18.8 A, 4.2 m Ω

Features

- Max $r_{DS(on)} = 4.2 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 18.8 \text{ A}$
- Max $r_{DS(on)} = 5.5 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 16.1 \text{ A}$
- High performance technology for extremely low r_{DS(on)}
- Termination is Lead-free and RoHS Compliant

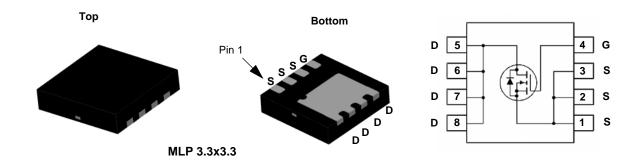


General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench® process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

Applications

- DC DC Buck Converters
- Notebook battery power management
- Load switch in Notebook



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			30	V
V _{GS}	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T _C = 25 °C		24	
I _D	-Continuous T _A = 25 °C		(Note 1a)	18.8	Α
	-Pulsed			60	
E _{AS}	Single Pulse Avalanche Energy		(Note 3)	188	mJ
D	Power Dissipation	T _C = 25 °C		45	W
P_{D}	Power Dissipation	T _A = 25 °C	(Note 1a)	2.3	VV
T _J , T _{STG}	Operating and Storage Junction Tempera	ture Range		-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.8	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	C/VV

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMC7664	FDMC7664	MLP 3.3x3.3	13 "	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		12		mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24 \text{ V}, V_{GS} = 0 \text{ V}$ $T_1 = 125 \text{ °C}$			1 250	μА
I _{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$			100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$	1.0	1.9	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μ A, referenced to 25 °C		-7		mV/°C
r _{DS(on)} Static Drain to Source On Resistance		V _{GS} = 10 V, I _D = 18.8 A		3.6	4.2	
	Static Drain to Source On Posistance	$V_{GS} = 4.5 \text{ V}, I_D = 16.1 \text{ A}$		4.5	5.5	mΩ
	V _{GS} = 10 V, I _D = 18.8 A T _J = 125 °C		4.4	5.4	11152	
9 _{FS}	Forward Transconductance	V _{DD} = 5 V, I _D = 18.8 A		115		S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 45 V V 0 V	3655	4865	pF
C _{oss}	Output Capacitance	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}$ f = 1 MHz	1100	1465	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	115	170	pF
R_g	Gate Resistance		0.8	2.2	Ω

Switching Characteristics

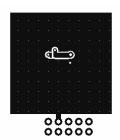
t _{d(on)}	Turn-On Delay Time		15	27	ns
t _r	Rise Time	V _{DD} = 15 V, I _D = 18.8 A	7	14	ns
t _{d(off)}	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	37	59	ns
t _f	Fall Time		6	12	ns
$Q_{g(TOT)}$	Total Gate Charge	V _{GS} = 0 V to 10 V	55	76	nC
Qg	Total Gate Charge	V _{GS} = 0 V to 4.5 V V _{DD} = 15 V	25	34	nC
Q _{gs}	Gate to Source Charge	I _D = 18.8 A	12		nC
Q_{gd}	Gate to Drain "Miller" Charge		6		nC

Drain-Source Diode Characteristics

V	Ven Source to Drain Dioge Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 18.8 \text{ A}$ (Note 2)	0.83	1.2	V
V SD		$V_{GS} = 0 \text{ V}, I_S = 1.9 \text{ A}$ (Note 2)	0.71	1.2	V
t _{rr}	Reverse Recovery Time	-I _F = 18.8 A, di/dt = 100 A/μs	41	65	ns
Q_{rr}	Reverse Recovery Charge	I _F = 18.8 A, αl/αl = 100 A/μs 20		35	nC

NOTES

1. R_{0,1A} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{0,1C} is guaranteed by design while R_{0,1C} is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper



b.125 °C/W when mounted on a minimum pad of 2 oz copper

- 2. Pulse Test: Pulse Width < 300 μ s, Duty cycle < 2.0 %.
- 3. E_{AS} of 188 mJ is based on starting T_J = 25 o C, L = 1 mH, I_{AS} = 19.4 A, V_{DD} = 27 V, V_{GS} = 10 V.

Typical Characteristics T_J = 25 °C unless otherwise noted

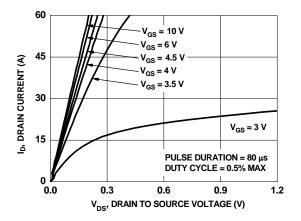


Figure 1. On Region Characteristics

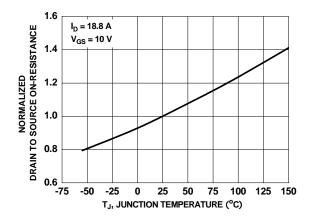


Figure 3. Normalized On Resistance vs. Junction Temperature

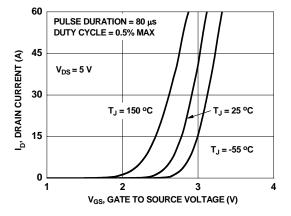


Figure 5. Transfer Characteristics

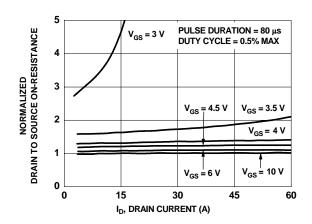


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

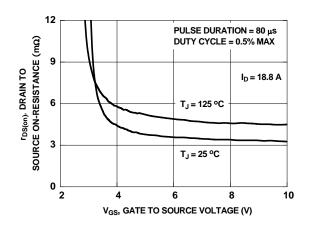


Figure 4. On-Resistance vs. Gate to Source Voltage

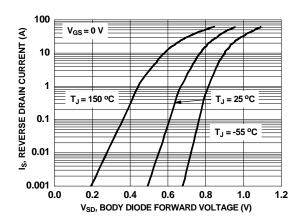


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25$ °C unless otherwise noted

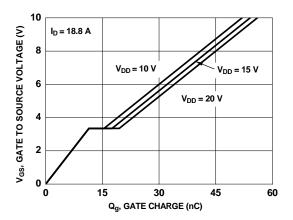


Figure 7. Gate Charge Characteristics

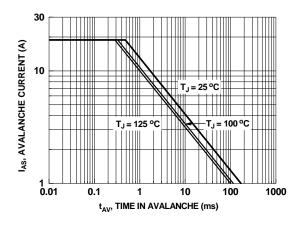


Figure 9. Unclamped Inductive Switching Capability

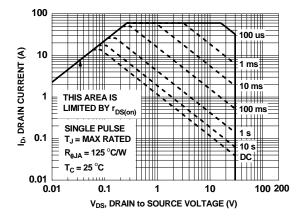


Figure 11. Forward Bias Safe Operating Area

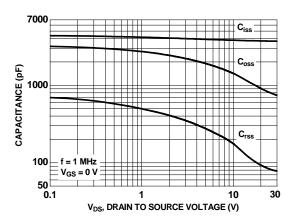


Figure 8. Capacitance vs. Drain to Source Voltage

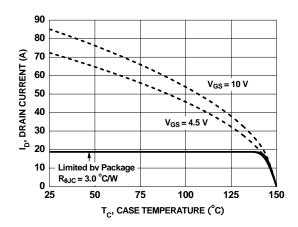


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

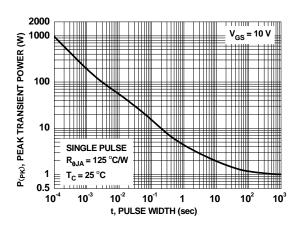


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25$ °C unless otherwise noted

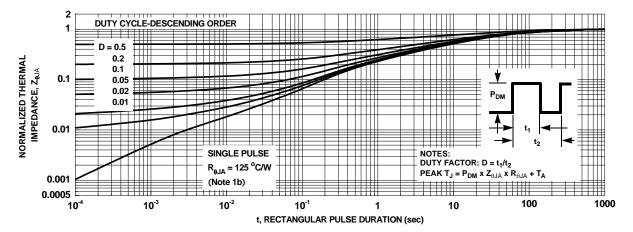
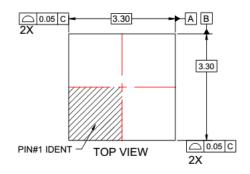
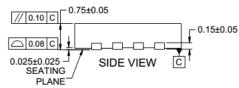
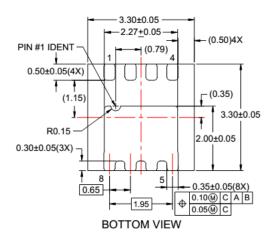


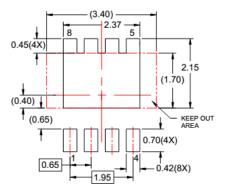
Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout









RECOMMENDED LAND PATTERN

NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.
- E. DRAWING FILENAME: MKT-MLP08Srev3.



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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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