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ON Semiconductor®

FDD5N50U

N-Channel UniFETTM Ultra FRFETTM MOSFET 500 V, 3 A, 2.0 Ω

Features

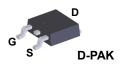
- $R_{DS(on)}$ = 1.65 Ω (Typ.) @ V_{GS} = 10 V, I_{D} = 1.5 A
- Low Gate Charge (Typ. 11 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- · RoHS Compliant

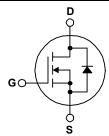
Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

Description

UniFETTM MOSFET is ON Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. UniFET Ultra FRFETTM MOSFET has much superior body diode reverse recovery performance. Its t_{rr} is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.





MOSFET Maximum Ratings $T_C = 25^{\circ}$ C unless otherwise noted.

Symbol	Parameter			FDD5N50UTM-WS	Unit	
V_{DSS}	Drain to Source Voltage			500	V	
V_{GSS}	Gate to Source Voltage			±30	V	
1	Drain Current	- Continuous (T _C = 25°C)		3	А	
ID	Drain Current	- Continuous (T _C = 100°C)		1.8	_ A	
I _{DM}	Drain Current	- Pulsed	(Note 1)	12	Α	
E _{AS}	Single Pulsed Avalanche En	ergy	(Note 2)	275	mJ	
I _{AR}	Avalanche Current		(Note 1)	3	Α	
E _{AR}	Repetitive Avalanche Energy	1	(Note 1)	4	mJ	
dv/dt	Peak Diode Recovery dv/dt		(Note 3)	4.5	V/ns	
Б	Dawer Dissination	(T _C = 25°C)		40	W	
P_{D}	Power Dissipation	- Derate Above 25°C		0.3	W/°C	
T _J , T _{STG}	Operating and Storage Temp	perature Range		-55 to +150	°C	
T_L	Maximum Lead Temperature	for Soldering, 1/8" from Case for 5 Sec	onds	300	°C	

Thermal Characteristics

Symbol	Parameter	FDD5N50UTM_WS	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	110	C/VV

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FDD5N50UTM-WS	FDD5N50U	DPAK	Tape and Reel	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
Off Charac	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V, T_J = 25^{\circ} C$	500	-	-	V
ΔBV _{DSS} / ΔΤ _J	Breakdown Voltage Temperature Coefficient	I_D = 250 μ A, Referenced to 25°C	-	0.6	-	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V	-	-	25	μА
		$V_{DS} = 400 \text{ V}, T_C = 125^{\circ}\text{C}$	-	-	250	μΑ
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V	-	-	±100	nA

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	3	-	5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 1.5 \text{ A}$	-	1.65	2.0	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 1.5 \text{ A}$	-	4	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	V 05.V.V 0.V	-	485	650	pF
C _{oss}	Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz	-	65	90	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	-	5	8	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 400 V, I _D = 5 A,	-	11	15	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	3	-	nC
Q_{gd}	Gate to Drain "Miller" Charge	(Note	4) _	5	-	nC

Switching Characteristics

t _{d(on)}	Turn-On Delay Time		-	14	38	ns
t _r		$V_{DD} = 250 \text{ V}, I_D = 5 \text{ A},$	-	21	52	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_G = 25 Ω	-	27	64	ns
t _f	Turn-Off Fall Time	(Note 4)	-	20	50	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	3	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current			-	12	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 3 A	-	-	1.6	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 5 A,	-	36	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	33	-	nC

Notes:

- 1: Repetitive rating: pulse width limited by maximum junction temperature.
- 2: L = 61 mH, I_{AS} = 3 A, V_{DD} = 50 V, R_G = 25 Ω , starting T_J = 25°C.
- 3: $I_{SD} \leq 3$ A, di/dt \leq 200 A/ μ s, $V_{DD} \leq$ BV $_{DSS}$, starting T_J = 25°C.
- 4: Essentially independent of operating temperature typical characteristics.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

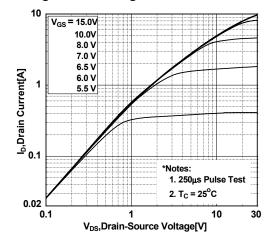


Figure 3. On-Resistance Variation vs.
Drain Current and Gate Voltage

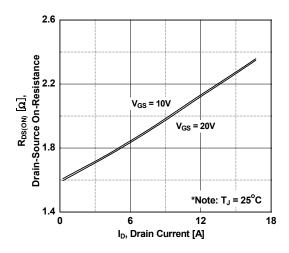


Figure 5. Capacitance Characteristics

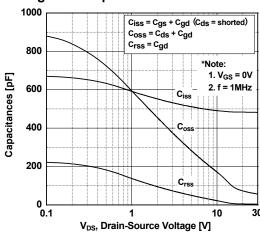


Figure 2. Transfer Characteristics

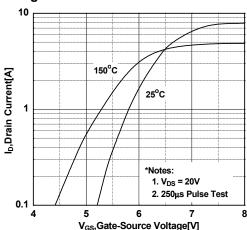


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

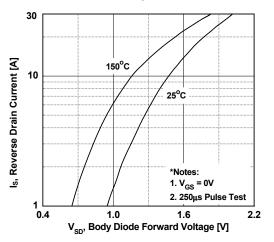
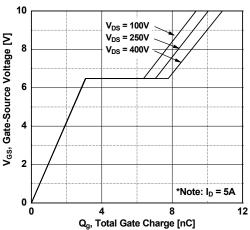


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

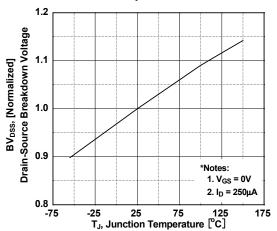


Figure 9. Maximum Drain Current vs. Case Temperature

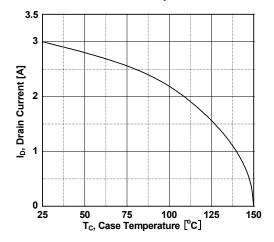


Figure 8. Maximum Safe Operating Area

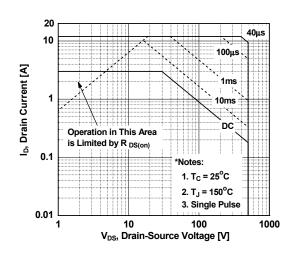
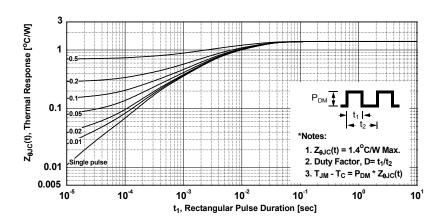


Figure 10. Transient Thermal Response Curve



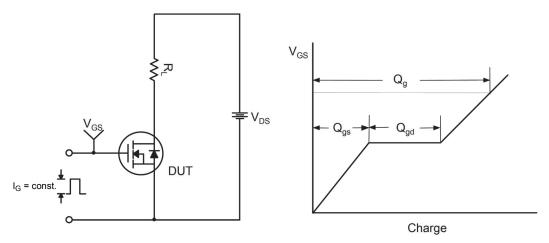


Figure 11. Gate Charge Test Circuit & Waveform

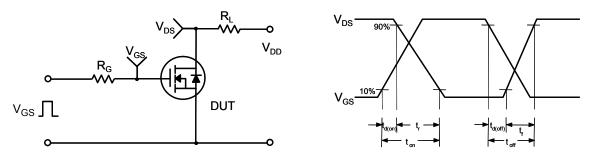


Figure 12. Resistive Switching Test Circuit & Waveforms

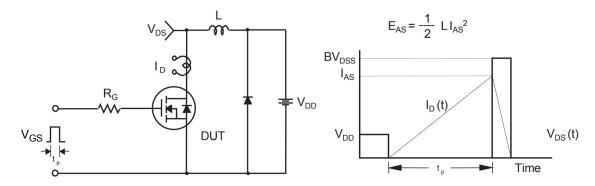


Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms

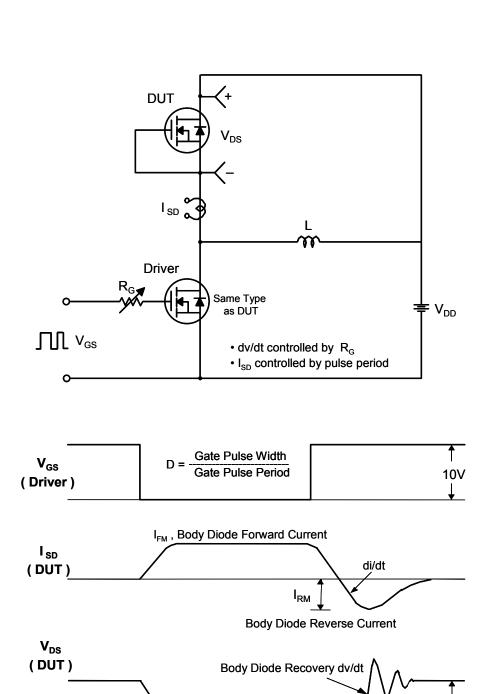


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Body Diode Forward Voltage Drop

Mechanical Dimensions

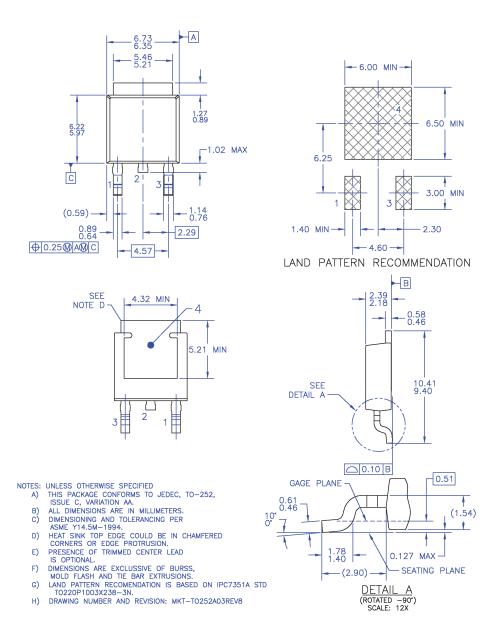


Figure 15. TO252 (D-PAK), Molded, 3-Lead, Option AA&AB

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