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March 2015

FCB290N80

N-Channel SuperFET® II MOSFET

800 V, 17 A, 0.29 Ω

Features

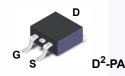
- $R_{DS(on)} = 0.259 \Omega (Typ.)$
- Ultra Low Gate Charge (Typ. Q_g = 58 nC)
- Low E_{oss} (Typ. 5.4 uJ @ 400V)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 240 pF)
- 100% Avalanche Tested
- · RoHS Compliant

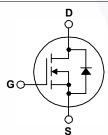
Applications

- · AC DC Power Supply
- · LED Lighting

Description

SuperFET® II MOSFET is Fairchild Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol		Parameter	FCB290N80	Unit
V _{DSS}	Drain to Source Voltage		800	V
V_{GSS}	Cata ta Cauraa Valtaria	- DC	±20	V
	Gate to Source Voltage	- AC (f > 1 H	Hz) ±30	V
	Dunin Comment	- Continuous (T _C = 25°C)	17	
I _D	Drain Current	- Continuous (T _C = 100°C)	10.8	A
I _{DM}	Drain Current	- Pulsed (Not	e 1) 42	Α
E _{AS}	Single Pulsed Avalanche Energy	(Not	e 2) 882	mJ
I _{AR}	Avalanche Current	(Not	e 1) 3.4	Α
E _{AR}	Repetitive Avalanche Energy	(Not	e 1) 2.12	mJ
	MOSFET dv/dt		100	\//n-
dv/dt	Peak Diode Recovery dv/dt	(Not	e 3) 20	V/ns
D	Davis Diagination	$(T_C = 25^{\circ}C)$	212	W
P_{D}	Power Dissipation - Derate Above 25°C		1.7	W/°C
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	οС
T _L	Maximum Lead Temperature for	Soldering, 1/8" from Case for 5 Seconds	300	οС

Thermal Characteristics

Symbol	Parameter	FCB290N80	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.59	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	°C/W
	Thermal Resistance, Junction to Ambient (1 in ² Pad of 2-oz Copper), Max.	40	

Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCB290N80	FCB290N80	D ² -PAK	Tape and Reel	330 mm	24 mm	800 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	lest Conditions	Min.	iyp.	Max.	Unit
Off Chara	cteristics					
BV _{DSS}	Drain to Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 1 \text{ mA}, T_J = 25^{\circ}\text{C}$	800	-	-	V
ΔBV _{DSS} / ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C	-	0.85	-	V/°C
1	Zero Gate Voltage Drain Current	$V_{DS} = 800 \text{ V}, V_{GS} = 0 \text{ V}$	1	-	25	
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 640 \text{ V}, V_{GS} = 0 \text{ V}, T_{C} = 125^{\circ}\text{C}$	1	-	250	μΑ
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	1	-	±10	μА

On Characteristics

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 1.7 \text{ mA}$	2.5	-	4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 8.5 \text{ A}$	-	0.259	0.290	Ω
9 _{FS}	Forward Transconductance	$V_{DS} = 20 \text{ V}, I_{D} = 8.5 \text{ A}$	-	20	-	S

Dynamic Characteristics

C _{iss}	Input Capacitance	400 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4 4	-\	2410	3205	pF
C _{oss}	Output Capacitance	V _{DS} = 100 V, V _{GS} = 0 V, f = 1 MHz	- \	75	100	pF
C _{rss}	Reverse Transfer Capacitance	1 - 1 1/11/12	-	0.36	-	pF
C _{oss}	Output Capacitance	$V_{DS} = 480 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	35	-	pF
C _{oss(eff.)}	Effective Output Capacitance	$V_{DS} = 0 V \text{ to } 480 V, V_{GS} = 0 V$	-	240	-	pF
Q _{g(tot)}	Total Gate Charge at 10V	V _{DS} = 640 V, I _D = 17 A,	-	58	75	nC
Q_{gs}	Gate to Source Gate Charge	V _{GS} = 10 V	-	11	-	nC
Q _{gd}	Gate to Drain "Miller" Charge	(Note 4)	-	22	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.75	-	Ω

Switching Characteristics

	_						
t _{d(on)}	Turn-On Delay Time			-	22	54	ns
t _r	Turn-On Rise Time	$V_{DD} = 400 \text{ V}, I_D = 17 \text{ A},$		-	14	38	ns
t _{d(off)}	Turn-Off Delay Time	V_{GS} = 10 V, R_g = 4.7 Ω		- /	61	132	ns
t _f	Turn-Off Fall Time		(Note 4)	-	2.6	15	ns

Drain-Source Diode Characteristics

Is	Maximum Continuous Drain to Source Diode Forward Current		-	-	17	Α
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current			-	42	Α
V_{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 17 A	-	-	1.2	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 17 A,	-	511	-	ns
Q _{rr}	Reverse Recovery Charge	$dI_F/dt = 100 A/\mu s$	-	12	-//	μС

Notes

- 1. Repetitive rating: pulse width limited by maximum junction temperature.
- 2. I $_{AS}$ = 3.4 A, R $_{G}$ = 25 Ω , starting T $_{J}$ = 25°C
- 3. I $_{SD} \leq$ 17 A, di/dt \leq 200 A/ μ s, V $_{DD} \leq$ BV $_{DSS}$, starting T $_{J}$ = 25°C
- 4. Essentially independent of operating temperature typical characteristic.

Typical Performance Characteristics

Figure 1. On-Region Characteristics

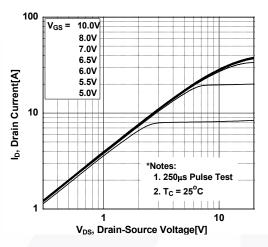


Figure 3. On-Resistance Variation vs.

Drain Current and Gate Voltage

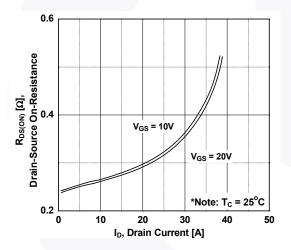


Figure 5. Capacitance Characteristics

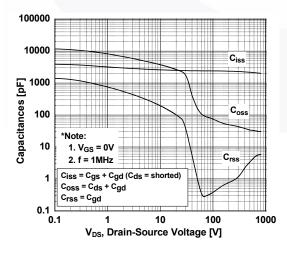


Figure 2. Transfer Characteristics

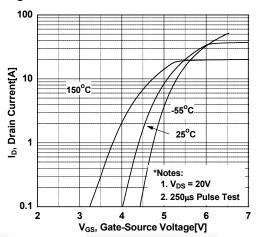


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

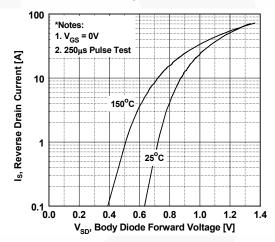
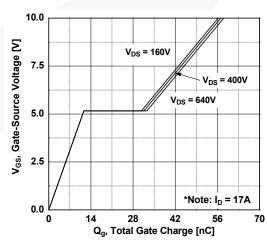


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

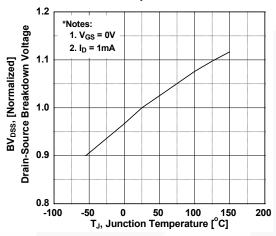


Figure 9. Maximum Safe Operating Area

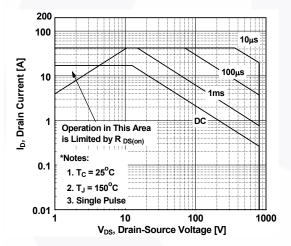


Figure 11. Eoss vs. Drain to Source Voltage

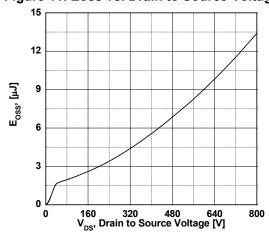


Figure 8. On-Resistance Variation vs. Temperature

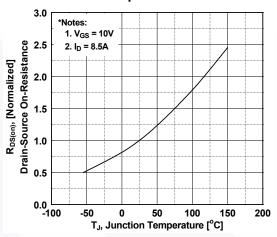
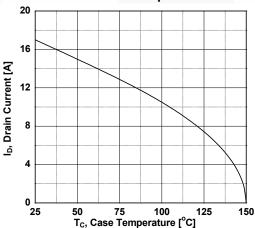
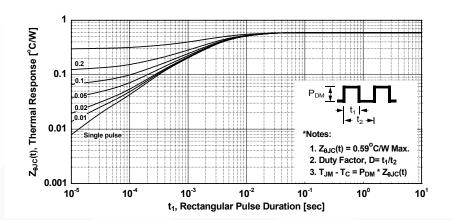


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 12. Transient Thermal Response Curve



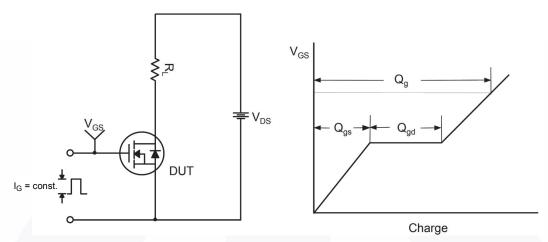


Figure 13. Gate Charge Test Circuit & Waveform

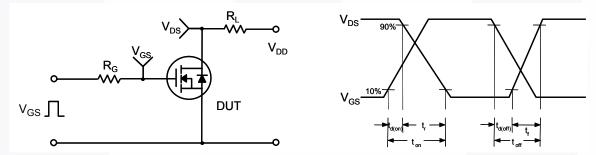


Figure 14. Resistive Switching Test Circuit & Waveforms

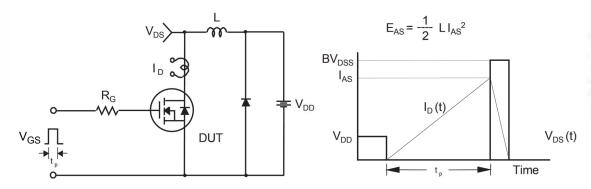


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

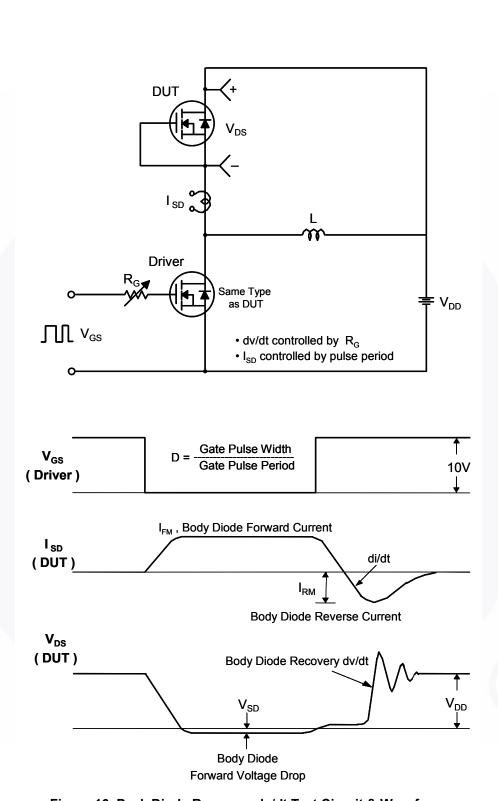
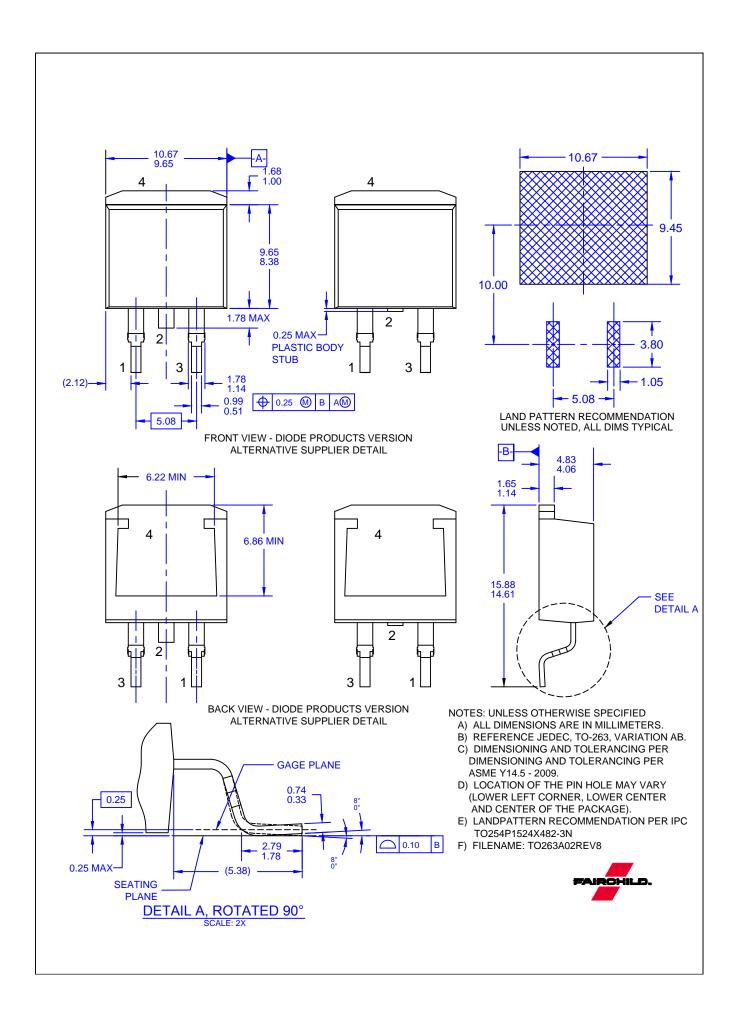


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms



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