Dual 2-A High-Speed, Low-Side Gate Drivers

FAN3226, FAN3227, FAN3228, FAN3229

SOIC8
CASE 751EB

MARKING DIAGRAM

$Y	= **onsemi** Logo Graphic
&Z	= Assembly Plant Code
&2	= 2−Digit Data Code (Year & Week)
&K	= 2−Digit Lot Run Traceability Code

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 20.

Description

The FAN3226−29 family of dual 2 A gate drivers is designed to drive N−channel enhancement−mode MOSFETs in low−side switching applications by providing high peak current pulses during the short switching intervals. The driver is available with either TTL or CMOS input thresholds. Internal circuitry provides an under−voltage lockout function by holding the output low until the supply voltage is within the operating range. In addition, the drivers feature matched internal propagation delays between A and B channels for applications requiring dual gate drives with critical timing, such as synchronous rectifiers. This enables connecting two drivers in parallel to effectively double the current capability driving a single MOSFET.

The FAN322X drivers incorporate MillerDrive™ architecture for the final output stage. This bipolar−MOSFET combination provides high current during the Miller plateau stage of the MOSFET turn−on/turn−off process to minimize switching loss, while providing rail−to−rail voltage swing and reverse current capability.

The FAN3226 offers two inverting drivers and the FAN3227 offers two non−inverting drivers. Each device has dual independent enable pins that default to ON if not connected. In the FAN3228 and FAN3229, each channel has dual inputs of opposite polarity, which allows configuration as non−inverting or inverting with an optional enable function using the second input. If one or both inputs are left unconnected, internal resistors bias the inputs such that the output is pulled low to hold the power MOSFET off.

Features

- Industry−Standard Pinouts
- 4.5−V to 18−V Operating Range
- 3−A Peak Sink/Source at V_{DD} = 12 V
- 2.4 A−Sink/1.6−A Source at V_{OUT} = 6 V
- Choice of TTL or CMOS Input Thresholds
- Four Versions of Dual Independent Drivers:
  - ♦ Dual Inverting + Enable (FAN3226)
  - ♦ Dual Non−Inverting + Enable (FAN3227)
  - ♦ Dual Inputs in Two Pin−Out Configurations:
    - − Compatible with FAN3225x (FAN3228)
    - − Compatible with TPS2814D (FAN3229)
- Internal Resistors Turn Driver Off If No Inputs
- MillerDrive Technology
- 12−ns/9−ns Typical Rise/Fall Times (1−nF Load)
- Under 20−ns Typical Propagation Delay Matched within 1 ns to the Other Channel
- Double Current Capability by Paralleling Channels

Features (Continued)

- 8−Lead SOIC Package
- Rated from −40°C to +125°C Ambient
- AEC−Q100 Qualified and PPAP Capable
- These are Pb−Free Devices

Applications

- Switch−Mode Power Supplies
- High−Efficiency MOSFET Switching
- Synchronous Rectifier Circuits
- DC−to−DC Converters
- Motor Control
- Servers
- Automotive−Qualified Systems

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PIN CONFIGURATIONS

Figure 1. Pin Configurations

PACKAGE OUTLINES

Figure 2. SOIC−8 (Top View)

THERMAL CHARACTERISTICS (Note 1)

Package	Θ_{JL} (Note 2)	Θ_{JT} (Note 3)	Θ_{JA} (Note 4)	Ψ_{JB} (Note 5)	Ψ_{JT} (Note 6)	Unit
8−Pin Small Outline Integrated Circuit (SOIC)	40	31	89	43	3.0	°C/W

1. Estimates derived from thermal simulation; actual values depend on the application.
2. Theta_JL (Θ_{JL}): Thermal resistance between the semiconductor junction and the bottom surface of all the leads (including any thermal pad) that are typically soldered to a PCB.
3. Theta_JT (Θ_{JT}): Thermal resistance between the semiconductor junction and the top surface of the package, assuming it is held at a uniform temperature by a top−side heatsink.
4. Theta_JA (Θ_{JA}): Thermal resistance between junction and ambient, dependent on the PCB design, heat sinking, and airflow. The value given is for natural convection with no heatsink using a 2S2P board, as specified in JEDEC standards JESD51−2, JESD51−5, and JESD51−7, as appropriate.
5. Psi_JB (Ψ_{JB}): Thermal characterization parameter providing correlation between semiconductor junction temperature and an application circuit board reference point for the thermal environment defined in Note 4. For the SOIC−8 package, the board reference is defined as the PCB copper adjacent to pin 6.
6. Psi_JT (Ψ_{JT}): Thermal characterization parameter providing correlation between the semiconductor junction temperature and the center of the top of the package for the thermal environment defined in Note 4.

PIN DEFINITIONS

Name	Description
ENA	*Enable Input for Channel A.* Pull pin LOW to inhibit driver A. ENA has TTL thresholds for both TTL and CMOS INx threshold.
ENB	*Enable Input for Channel B.* Pull pin LOW to inhibit driver B. ENB has TTL thresholds for both TTL and CMOS INx threshold.
GND	Ground. Common ground reference for input and output circuits.
INA	*Input to Channel A.*
INA+	*Non−Inverting Input to Channel A.* Connect to VDD to enable output.
INA−	*Inverting Input to Channel A.* Connect to GND to enable output.
INB	*Input to Channel B.*
INB+	*Non−Inverting Input to Channel B.* Connect to VDD to enable output.
INB−	*Inverting Input to Channel B.* Connect to GND to enable output.
OUTA	*Gate Drive Output A:* Held LOW unless required input(s) are present and VDD is above UVLO threshold.
OUTB	*Gate Drive Output B:* Held LOW unless required input(s) are present and VDD is above UVLO threshold.
$\overline{\text{OUTA}}$	*Gate Drive Output A* (inverted from the input): Held LOW unless required input is present and VDD is above UVLO threshold.
$\overline{\text{OUTB}}$	*Gate Drive Output B* (inverted from the input): Held LOW unless required input is present and VDD is above UVLO threshold.
VDD	*Supply Voltage*. Provides power to the IC.

Figure 3. Pin Configurations (Repeated)

OUTPUT LOGIC

FAN3226 (x = A or B)		
ENx	**INx**	**$\overline{\text{OUTx}}$**
0	0	0
0	1 (Note 7)	0
1 (Note 7)	0	1
1 (Note 7)	1 (Note 7)	0

FAN3227 (x = A or B)		
ENx	**INx**	**OUTx**
0	0 (Note 7)	0
0	1	0
1 (Note 7)	0 (Note 7)	0
1 (Note 7)	1	1

FAN3228 and FAN3229 (x = A or B)		
INx+	**INx−**	**OUTx**
0 (Note 7)	0	0
0 (Note 7)	1 (Note 7)	0
1	0	1
1	1 (Note 7)	0

7. Default input signal if no external connection is made.

BLOCK DIAGRAMS

Figure 4. FAN3226 Block Diagram

Figure 5. FAN3227 Block Diagram

Figure 6. FAN3228 Block Diagram

Figure 7. FAN3229 Block Diagram

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
V_{DD}	VDD to GND	−0.3	20.0	V
V_{EN}	ENA and ENB to GND	GND − 0.3	V_{DD} + 0.3	V
V_{IN}	INA, INA+, INA−, INB, INB+ and INB− to GND	GND − 0.3	V_{DD} + 0.3	V
V_{OUT}	OUTA and OUTB to GND	GND − 0.3	V_{DD} + 0.3	V
T_L	Lead Soldering Temperature (10 Seconds)	−	+260	°C
T_J	Junction Temperature	−55	+150	°C
T_{STG}	Storage Temperature	−65	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{DD}	Supply Voltage Range	4.5	18.0	V
V_{EN}	Enable Voltage ENA and ENB	0	V_{DD}	V
V_{IN}	Input Voltage INA, INA+, INA−, INB, INB+ and INB−	0	V_{DD}	V
T_A	Operating Ambient Temperature	−40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to +125°C unless otherwise noted. Currents are defined as positive into the device and negative out of the device.)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	Operating Range		4.5	−	18.0	V
I_{DD}	Supply Current, Inputs/EN Not Connected	TTL	−	0.75	1.20	mA
		CMOS (Note 8)	−	0.65	1.05	
V_{ON}	Turn−On Voltage	INA = ENA = V_{DD}, INB = ENB = 0 V	3.3	3.9	4.5	V
V_{OFF}	Turn−Off Voltage	INA = ENA = V_{DD}, INB = ENB = 0 V	3.1	3.7	4.3	V
INPUTS (TTL, FAN322XT) (Note 9)						
V_{INL_T}	INx Logic Low Threshold		0.8	1.2	−	V
V_{INH_T}	INx Logic High Threshold		−	1.6	2.0	V
V_{HYS_T}	TTL Logic Hysteresis Voltage		0.2	0.4	0.8	V
I_{INx_T}	Non−Inverting Input Current	IN = 0 V	−1.5	−	1.5	μA
I_{INx_T}	Non−Inverting Input Current	IN = V_{DD}	90	120	175	μA
I_{INx_T}	Inverting Input Current	IN = 0 V	−175	−120	−90	μA
I_{INx_T}	Inverting Input Current	IN = V_{DD}	−1.5	−	1.5	μA
INPUTS (FAN322xC) (Note 9)						
V_{INL_C}	INx Logic Low Threshold		30	38	−	%V_{DD}
V_{INH_C}	INx Logic High Threshold		−	55	70	%V_{DD}
V_{HYS_C}	CMOS Logic Hysteresis Voltage		−	17	−	%V_{DD}
I_{INx_T}	Non−Inverting Input Current	IN = 0 V	−1.5	−	1.5	μA
I_{INx_T}	Non−Inverting Input Current	IN = V_{DD}	90	120	175	μA

ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V and T_J = −40°C to +125°C unless otherwise noted. Currents are defined as positive into the device and negative out of the device.) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{INx_T}	Inverting Input Current	IN = 0 V	−175	−120	−90	μA
I_{INx_T}	Inverting Input Current	IN = V_{DD}	−1.5	–	1.5	μA
ENABLE (FAN3226C, FAN3226T, FAN3227C, FAN3227T)						
V_{ENL}	Enable Logic Low Threshold	EN from 5 V to 0 V	0.8	1.2	–	V
V_{ENH}	Enable Logic High Threshold	EN from 0 V to 5 V	–	1.6	2.0	V
V_{HYS_T}	TTL Logic Hysteresis Voltage		–	0.4	–	V
R_{PU}	Enable Pull−up Resistance		–	100	–	kΩ
t_{D3}	EN to Output Propagation Delay (Note 11)	0 V to 5 V EN, 1 V/ns Slew Rate	8	19	35	ns
t_{D4}		5 V to 0 V EN, 1 V/ns Slew Rate	8	18	35	ns
OUTPUTS						
I_{SINK}	OUT Current, Mid−Voltage, Sinking (Note 10)	OUT at V_{DD} / 2, C_{LOAD} = 0.1 μF, f = 1 kHz	–	2.4	–	A
I_{SOURCE}	OUT Current, Mid−Voltage, Sourcing (Note 10)	OUT at V_{DD} / 2, C_{LOAD} = 0.1 μF, f = 1 kHz	–	−1.6	–	A
I_{PK_SINK}	OUT Current, Peak, Sinking (Note 10)	C_{LOAD} = 0.1 μF, f = 1 kHz	–	3	–	A
I_{PK_SOURCE}	OUT Current, Peak, Sourcing (Note 10)	C_{LOAD} = 0.1 μF, f = 1 kHz	–	−3	–	A
t_{RISE}	Output Rise Time (Note 11)	C_{LOAD} = 1000 pF	–	12	22	ns
t_{FALL}	Output Fall Time (Note 11)	C_{LOAD} = 1000 pF	–	9	17	ns
I_{RVS}	Output Reverse Current Withstand (Note 10)		–	500	–	mA
FAN322xT, FAN322xC						
t_{D1}	Output Propagation Delay, CMOS Inputs (Note 12)	CMOS Input	7	15	33	ns
t_{D2}		CMOS Input	6	15	42	ns
t_{D1}	Output Propagation Delay, TTL Inputs (Note 12)	TTL Input	9	19	34	ns
t_{D2}		TTL Input	9	18	32	ns
$t_{DEL.MATCH}$	Propagation Matching Between Channels (Note 12)	INA = INB, OUTA and OUTB at 50% Point	–	2	4	ns
V_{OH}	High Level Output Voltage	V_{OH} = V_{DD} − V_{OUT}, I_{OUT}= −1 mA	–	15	35	mV
V_{OL}	Low Level Output Voltage	I_{OUT}= 1 mA	–	10	25	mV

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

8. Lower supply current due to inactive TTL circuitry.
9. EN inputs have modified TTL thresholds; refer to the ENABLE section.
10. Not tested in production.
11. *See Timing Diagrams of Figure 10 and Figure 11.*
12. *See Timing Diagrams of Figure 8 and Figure 9.*

TIMING DIAGRAMS

Figure 8. Non−Inverting (EN HIGH or Floating)

Figure 9. Inverting (EN HIGH or Floating)

Figure 10. Non−Inverting (IN HIGH)

Figure 11. Inverting (IN LOW)

TYPICAL PERFORMANCE CHARACTERISTICS

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

Figure 12. I_{DD} (Static) vs. Supply Voltage (Note 13)

Figure 13. I_{DD} (Static) vs. Supply Voltage (Note 13)

Figure 14. I_{DD} (Static) vs. Supply Voltage (Note 13)

Figure 15. I_{DD} (No−Load) vs. Frequency

Figure 16. I_{DD} (No−Load) vs. Frequency

Figure 17. I_{DD} (1 nF Load) vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

Figure 18. I_{DD} (1 nF Load) vs. Frequency

Figure 19. I_{DD} (Static) vs. Temperature (Note 13)

Figure 20. I_{DD} (Static) vs. Temperature (Note 13)

Figure 21. I_{DD} (Static) vs. Temperature (Note 13)

Figure 22. Input Thresholds vs. Supply Voltage

Figure 23. Input Thresholds vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

Figure 24. Input Threshold % vs. Supply Voltage

Figure 25. Input Thresholds vs. Temperature

Figure 26. Input Thresholds vs. Temperature

Figure 27. UVLO Thresholds vs. Temperature

Figure 28. UVLO Thresholds vs. Temperature

Figure 29. Propagation Delay vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

Figure 30. Propagation Delay vs. Supply Voltage

Figure 31. Propagation Delay vs. Supply Voltage

Figure 32. Propagation Delay vs. Supply Voltage

Figure 33. Propagation Delays vs. Temperature

Figure 34. Propagation Delays vs. Temperature

Figure 35. Propagation Delays vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

Figure 36. Propagation Delays vs. Temperature

Figure 37. Fall Time vs. Supply Voltage

Figure 38. Rise Time vs. Supply Voltage

Figure 39. Rise and Fall Times vs. Temperature

Figure 40. Rise / Fall Waveforms with 1 nF Load

Figure 41. Rise / Fall Waveforms with 10 nF Load

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Typical characteristics are provided at 25°C and V_{DD} = 12 V unless otherwise noted)

Figure 42. Quasi−Static Source Current with V_{DD} = 12 V

Figure 43. Quasi−Static Sink Current with V_{DD} = 12 V

Figure 44. Quasi−Static Source Current with V_{DD} = 8 V

Figure 45. Quasi−Static Sink Current with V_{DD} = 8 V

13. For any inverting inputs pulled LOW, non−inverting inputs pulled HIGH, or outputs driven HIGH; static I_{DD} increases by the current flowing through the corresponding pull−up/down resistor, shown in Figure 4.

TEST CIRCUIT

Figure 46. Quasi−Static I_{OUT} / V_{OUT} Test Circuit

APPLICATIONS INFORMATION

Input Thresholds

Each member of the FAN322x driver family consists of two identical channels that may be used independently at rated current or connected in parallel to double the individual current capacity. In the FAN3226 and FAN3227, channels A and B can be enabled or disabled independently using ENA or ENB, respectively. The EN pin has TTL thresholds for parts with either CMOS or TTL input thresholds. If ENA and ENB are not connected, an internal pull−up resistor enables the driver channels by default. If the channel A and channel B inputs and outputs are connected in parallel to increase the driver current capacity, ENA and ENB should be connected and driven together.

The FAN322x family offers versions in either TTL or CMOS input thresholds. In the FAN322xT, the input thresholds meet industry−standard TTL−logic thresholds independent of the V_{DD} voltage, and there is a hysteresis voltage of approximately 0.4 V. These levels permit the inputs to be driven from a range of input logic signal levels for which a voltage over 2 V is considered logic high. The driving signal for the TTL inputs should have fast rising and falling edges with a slew rate of 6 V/µs or faster, so a rise time from 0 to 3.3 V should be 550 ns or less. With reduced slew rate, circuit noise could cause the driver input voltage to exceed the hysteresis voltage and retrigger the driver input, causing erratic operation.

In the FAN322xC, the logic input thresholds are dependent on the V_{DD} level and, with V_{DD} of 12 V, the logic rising edge threshold is approximately 55% of V_{DD} and the input falling edge threshold is approximately 38% of $_{VDD}$. The CMOS input configuration offers a hysteresis voltage of approximately 17% of V_{DD}. The CMOS inputs can be used with relatively slow edges (approaching DC) if good decoupling and bypass techniques are incorporated in the system design to prevent noise from violating the input voltage hysteresis window. This allows setting precise timing intervals by fitting an R−C circuit between the controlling signal and the IN pin of the driver. The slow rising edge at the IN pin of the driver introduces a delay between the controlling signal and the OUT pin of the driver.

Static Supply Current

In the I_{DD} (static) typical performance characteristics (see Figure 12 – Figure 14 and Figure 19 – Figure 21), the curve is produced with all inputs / enables floating (OUT is low) and indicates the lowest static IDD current for the tested configuration. For other states, additional current flows through the 100 kΩ resistors on the inputs and outputs shown in the block diagram of each part (see Figure 4 – Figure 7). In these cases, the actual static I_{DD} current is the value obtained from the curves plus this additional current.

MillerDrive Gate−Drive Technology

FAN322x gate drivers incorporate the MillerDrive architecture shown in Figure 47. For the output stage, a combination of bipolar and MOS devices provide large currents over a wide range of supply voltage and temperature variations. The bipolar devices carry the bulk of the current as OUT swings between 1/3 to 2/3 V_{DD} and the MOS devices pull the output to the high or low rail.

The purpose of the MillerDrive architecture is to speed up switching by providing high current during the Miller plateau region when the gate−drain capacitance of the MOSFET is being charged or discharged as part of the turn−on/turn−off process.

For applications that have zero voltage switching during the MOSFET turn−on or turn−off interval, the driver supplies high peak current for fast switching even though the Miller plateau is not present. This situation often occurs in synchronous rectifier applications because the body diode is generally conducting before the MOSFET is switched on.

The output pin slew rate is determined by V_{DD} voltage and the load on the output. It is not user adjustable, but a series resistor can be added if a slower rise or fall time at the MOSFET gate is needed.

Figure 47. Miller Drive Output Architecture

Under−Voltage Lockout (UVLO)

The FAN322x startup logic is optimized to drive ground−referenced N−channel MOSFETs with an under−voltage lockout (UVLO) function to ensure that the IC starts up in an orderly fashion. When V_{DD} is rising, yet below the 3.9 V operational level, this circuit holds the output low, regardless of the status of the input pins. After the part is active, the supply voltage must drop 0.2 V before the part shuts down. This hysteresis helps prevent chatter when low V_{DD} supply voltages have noise from the power switching. This configuration is not suitable for driving high−side P−channel MOSFETs because the low output voltage of the driver would turn the P−channel MOSFET on with V_{DD} below 3.9 V.

V_{DD} Bypass Capacitor Guidelines

To enable this IC to turn a device on quickly, a local high−frequency bypass capacitor C_{BYP} with low ESR and ESL should be connected between the V_{DD} and GND pins with minimal trace length. This capacitor is in addition to bulk electrolytic capacitance of 10 μF to 47 μF commonly found on driver and controller bias circuits.

A typical criterion for choosing the value of C_{BYP} is to keep the ripple voltage on the V_{DD} supply to ≤5%. This is often achieved with a value ≥20 times the equivalent load capacitance C_{EQV}, defined here as Q_{GATE}/V_{DD}. Ceramic capacitors of 0.1 μF to 1 μF or larger are common choices, as are dielectrics, such as X5R and X7R with good temperature characteristics and high pulse current capability.

If circuit noise affects normal operation, the value of C_{BYP} may be increased to 50−100 times the C_{EQV}, or C_{BYP} may be split into two capacitors. One should be a larger value, based on equivalent load capacitance, and the other a smaller value, such as 1−10 nF mounted closest to the V_{DD} and GND pins to carry the higher frequency components of the current pulses. The bypass capacitor must provide the pulsed current from both of the driver channels and, if the drivers are switching simultaneously, the combined peak current sourced from the C_{BYP} would be twice as large as when a single channel is switching.

Layout and Connection Guidelines

The FAN3226−26 family of gate drivers incorporates fast−reacting input circuits, short propagation delays, and powerful output stages capable of delivering current peaks over 2 A to facilitate voltage transition times from under 10 ns to over 150 ns. The following layout and connection guidelines are strongly recommended:

- Keep high−current output and power ground paths separate logic and enable input signals and signal ground paths. This is especially critical when dealing with TTL−level logic thresholds at driver inputs and enable pins.
- Keep the driver as close to the load as possible to minimize the length of high−current traces. This reduces the series inductance to improve high−speed switching, while reducing the loop area that can radiate EMI to the driver inputs and surrounding circuitry.
- If the inputs to a channel are not externally connected, the internal 100 kΩ resistors indicated on block diagrams command a low output. In noisy environments, it may be necessary to tie inputs of an unused channel to V_{DD} or GND using short traces to prevent noise from causing spurious output switching.
- Many high−speed power circuits can be susceptible to noise injected from their own output or other external sources, possibly causing output re−triggering. These effects can be obvious if the circuit is tested in breadboard or non−optimal circuit layouts with long input, enable, or output leads. For best results, make connections to all pins as short and direct as possible.
- The FAN322x is compatible with many other industry−standard drivers. In single input parts with enable pins, there is an internal 100 kΩ resistor tied to V_{DD} to enable the driver by default; this should be considered in the PCB layout.
- The turn−on and turn−off current paths should be minimized, as discussed in the following section.

Figure 48 shows the pulsed gate drive current path when the gate driver is supplying gate charge to turn the MOSFET on. The current is supplied from the local bypass capacitor, C_{BYP}, and flows through the driver to the MOSFET gate and to ground. To reach the high peak currents possible, the resistance and inductance in the path should be minimized. The localized C_{BYP} acts to contain the high peak current pulses within this driver−MOSFET circuit, preventing them from disturbing the sensitive analog circuitry in the PWM controller.

Figure 48. Current Path for MOSFET Turn−On

Figure 49 shows the current path when the gate driver turns the MOSFET off. Ideally, the driver shunts the current directly to the source of the MOSFET in a small circuit loop. For fast turn−off times, the resistance and inductance in this path should be minimized.

Figure 49. Current Path for MOSFET Turn−Off

Truth Table of Logic Operation

The FAN3228/FAN3229 truth table indicates the operational states using the dual−input configuration. In a non−inverting driver configuration, the IN− pin should be a logic low signal. If the IN− pin is connected to logic high, a disable function is realized, and the driver output remains low regardless of the state of the IN+ pin.

Table 1. TRUTH TABLE OF LOGIC OPERATION

IN+	IN−	OUT
0	0	0
0	1	0
1	0	1
1	1	0

In the non−inverting driver configuration in Figure 50, the IN− pin is tied to ground and the input signal (PWM) is applied to IN+ pin. The IN− pin can be connected to logic high to disable the driver and the output remains low, regardless of the state of the IN+ pin.

Figure 50. Dual−Input Driver Enabled, Non−Inverting Configuration

In the inverting driver application in Figure 51, the IN+ pin is tied high. Pulling the IN+ pin to GND forces the output low, regardless of the state of the IN− pin.

Figure 51. Dual−Input Driver Enabled, Inverting Configuration

Operational Waveforms

At power−up, the driver output remains low until the V_{DD} voltage reaches the turn−on threshold. The magnitude of the OUT pulses rises with V_{DD} until steady−state V_{DD} is reached. The non−inverting operation illustrated in Figure 52 shows that the output remains low until the UVLO threshold is reached, the output is in−phase with the input.

Figure 52. Non−Inverting Startup Waveforms

For the inverting configuration of Figure 51, startup waveforms are shown in Figure 53. With IN+ tied to V_{DD} and the input signal applied to IN−, the OUT pulses are inverted with respect to the input. At power−up, the inverted output remains low until the V_{DD} voltage reaches the turn−on threshold, then it follows the input with inverted phase.

Figure 53. Inverting Startup Waveforms

Thermal Guidelines

Gate drivers used to switch MOSFETs and IGBTs at high frequencies can dissipate significant amounts of power. It is important to determine the driver power dissipation and the resulting junction temperature in the application to ensure that the part is operating within acceptable temperature limits.

The total power dissipation in a gate driver is the sum of two components, P_{GATE} and $P_{DYNAMIC}$:

$$P_{TOTAL} = P_{GATE} + P_{DYNAMIC} \quad \text{(eq. 1)}$$

Gate Driving Loss: The most significant power loss results from supplying gate current (charge per unit time) to switch the load MOSFET on and off at the switching frequency. The power dissipation that results from driving a MOSFET at a specified gate−source voltage, V_{GS}, with gate charge, Q_G, at switching frequency, f_{SW}, is determined by:

$$P_{GATE} = Q_G \cdot V_{GS} \cdot f_{SW} \cdot n \quad \text{(eq. 2)}$$

n is the number of driver channels in use (1 or 2).

Dynamic Pre−drive / Shoot−through Current: A power loss resulting from internal current consumption under dynamic operating conditions, including pin pull−up / pull−down resistors, can be obtained using the "I_{DD} (No−Load) vs. Frequency" graphs in Typical Performance Characteristics to determine the current $I_{DYNAMIC}$ drawn from V_{DD} under actual operating conditions:

$$P_{DYMANIC} = I_{DYNAMIC} \cdot V_{DD} \cdot n \quad \text{(eq. 3)}$$

Once the power dissipated in the driver is determined, the driver junction rise with respect to circuit board can be evaluated using the following thermal equation, assuming ψ_{JB} was determined for a similar thermal design (heat sinking and air flow):

$$T_J = P_{TOTAL} \cdot \Psi_{JB} + T_B \quad \text{(eq. 4)}$$

where:

T_J = driver junction temperature;

ψ_{JB} = (psi) thermal characterization parameter relating temperature rise to total power dissipation; and

T_B = board temperature in location as defined in the Thermal Characteristics table.

In the forward converter with synchronous rectifier shown in the typical application diagrams, the FDMS8660S is a reasonable MOSFET selection. The gate charge for each SR MOSFET would be 60 nC with $V_{GS} = V_{DD} = 7$ V. At a switching frequency of 500 kHz, the total power dissipation is:

$$P_{GATE} = 60\ \text{nC} \cdot 7\ \text{V} \cdot 500\ \text{kHz} \cdot 2 = 0.42\ \text{W} \quad \text{(eq. 5)}$$

$$P_{DYNAMIC} = 3\ \text{mA} \cdot 7\ \text{V} \cdot 2 = 0.042\ \text{W} \quad \text{(eq. 6)}$$

$$P_{TOTAL} = 0.46\ \text{W} \quad \text{(eq. 7)}$$

The SOIC−8 has a junction−to−board thermal characterization parameter of ψ_{JB} = 43°C/W. In a system application, the localized temperature around the device is a function of the layout and construction of the PCB along with airflow across the surfaces. To ensure reliable operation, the maximum junction temperature of the device must be prevented from exceeding the maximum rating of 150°C; with 80% derating, T_J would be limited to 120°C. Rearranging Equation 4 determines the board temperature required to maintain the junction temperature below 120°C:

$$T_B = T_J - P_{TOTAL} \cdot \Psi_{JB} \quad \text{(eq. 8)}$$

$$T_B = 120°\text{C} - 0.46\ \text{W} \cdot 43°\text{C/W} = 100°\text{C} \quad \text{(eq. 9)}$$

Consider tradeoffs between reducing overall circuit size with junction temperature reduction for increased reliability.

TYPICAL APPLICATION DIAGRAMS

Figure 54. Forward Converter with Synchronous Rectification

Figure 55. Primary−Side Dual Driver in a Push−Pull Converter

Figure 56. Phase−Shifted Full−Bridge with Two Gate Drive Transformers (Simplified)

ORDERING INFORMATION

Part Number	Logic	Input Threshold	Package	Shipping†
FAN3226TMX−F085	Dual Inverting Channels + Dual Enable	TTL	SOIC−8	2,500 / Tape & Reel
FAN3227TMX−F085	Dual Non−Inverting Channels + Dual Enable	TTL	SOIC−8	2,500 / Tape & Reel

DISCONTINUED (Note 14)

FAN3226CMX−F085	Dual Inverting Channels + Dual Enable	CMOS	SOIC−8	2,500 / Tape & Reel
FAN3227CMX−F085	Dual Non−Inverting Channels + Dual Enable	CMOS	SOIC−8	2,500 / Tape & Reel
FAN3228CMX−F085	Dual Channels of Two−Input / One−Output Drivers, Pin Configuration 1	CMOS	SOIC−8	2,500 / Tape & Reel
FAN3229CMX−F085	Dual Channels of Two−Input / One−Output Drivers, Pin Configuration 2	CMOS	SOIC−8	2,500 / Tape & Reel
FAN3228TMX−F085	Dual Channels of Two−Input / One−Output Drivers, Pin Configuration 1	TTL	SOIC−8	2,500 / Tape & Reel
FAN3229TMX−F085	Dual Channels of Two−Input / One−Output Drivers, Pin Configuration 2	TTL	SOIC−8	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

14. **DISCONTINUED:** These devices are not recommended for new design. Please contact your **onsemi** representative for information. The most current information on these devices may be available on www.onsemi.com.

Table 2. RELATED PRODUCTS

Type	Part Number	Gate Drive (Note 15) (Sink/Src)	Input Threshold	Logic	Package
Dual 2 A	FAN3216T	+2.4 A / −1.6 A	TTL	Dual Inverting Channels	SOIC8
Dual 2 A	FAN3217T	+2.4 A / −1.6 A	TTL	Dual Non−Inverting Channels	SOIC8
Dual 2 A	FAN3226C	+2.4 A / −1.6 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8
Dual 2 A	FAN3226T	+2.4 A / −1.6 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8
Dual 2 A	FAN3227C	+2.4 A / −1.6 A	CMOS	Dual Non−Inverting Channels + Dual Enable	SOIC8
Dual 2 A	FAN3227T	+2.4 A / −1.6 A	TTL	Dual Non−Inverting Channels + Dual Enable	SOIC8
Dual 2 A	FAN3228C	+2.4 A / −1.6 A	CMOS	Dual Channels of Two−Input/One−Output, Pin Config.1	SOIC8
Dual 2 A	FAN3228T	+2.4 A / −1.6 A	TTL	Dual Channels of Two−Input/One−Output, Pin Config.1	SOIC8
Dual 2 A	FAN3229C	+2.4 A / −1.6 A	CMOS	Dual Channels of Two−Input/One−Output, Pin Config.2	SOIC8
Dual 2 A	FAN3229T	+2.4 A / −1.6 A	TTL	Dual Channels of Two−Input/One−Output, Pin Config.2	SOIC8
Dual 2 A	FAN3268T	+2.4 A / −1.6 A	TTL	20 V Non−Inverting Channel (NMOS) and Inverting Channel (PMOS) + Dual Enables	SOIC8
Dual 4 A	FAN3213T	+2.5 A / −1.8 A	TTL	Dual Inverting Channels	SOIC8
Dual 4 A	FAN3214T	+2.5 A / −1.8 A	TTL	Dual Non−Inverting Channels	SOIC8
Dual 4 A	FAN3223C	+4.3 A / −2.8 A	CMOS	Dual Inverting Channels + Dual Enable	SOIC8
Dual 4 A	FAN3223T	+4.3 A / −2.8 A	TTL	Dual Inverting Channels + Dual Enable	SOIC8
Dual 4 A	FAN3224C	+4.3 A / −2.8 A	CMOS	Dual Non−Inverting Channels + Dual Enable	SOIC8
Dual 4 A	FAN3224T	+4.3 A / −2.8 A	TTL	Dual Non−Inverting Channels + Dual Enable	SOIC8, SOIC8−EP
Dual 4 A	FAN3225C	+4.3 A / −2.8 A	CMOS	Dual Channels of Two−Input/One−Output	SOIC8
Dual 4 A	FAN3225T	+4.3 A / −2.8 A	TTL	Dual Channels of Two−Input/One−Output	SOIC8
Single 9 A	FAN3121C	+9.7 A / −7.1 A	CMOS	Single Inverting Channel + Enable	SOIC8
Single 9 A	FAN3121T	+9.7 A / −7.1 A	TTL	Single Inverting Channel + Enable	SOIC8
Single 9 A	FAN3122C	+9.7 A / −7.1 A	CMOS	Single Non−Inverting Channel + Enable	SOIC8
Single 9 A	FAN3122T	+9.7 A / −7.1 A	TTL	Single Non−Inverting Channel + Enable	SOIC8, SOIC8−EP

15. Typical currents with OUTx at 6 V and V_{DD} = 12 V.
16. Thresholds proportional to an externally supplied reference voltage.

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SOIC8
CASE 751EB
ISSUE A

DATE 24 AUG 2017

LAND PATTERN RECOMMENDATION

OPTION A - BEVEL EDGE

OPTION B - NO BEVEL EDGE

DETAIL A
SCALE: 2:1

NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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