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Application of SiC MOSFETs

On the Effect of Threshold Shift of SiC MOSFETs

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APPLICATION NOTE

Introduction

Among the Wide Band Gap materials silicon carbide (SiC) is by far the most mature one. The raw wafer quality has greatly improved over the last years with significant reduction of micro pipes and dislocations. Silicon carbide devices can work at high temperatures, are very robust and offer both low conduction and switching losses. The high thermal conductivity makes SiC also a perfect choice for high power applications, when good cooling is required.

Compared to silicon switches, silicon carbide MOSFETs inherit some specific characteristics like the shift of gate threshold a designer should be aware of. This effect will be explained in this application note.

Driving the Gate

Despite the lower drift layer resistance of SiC MOSFETs compared to silicon, their lower carrier mobility results in higher channel resistance. For that reason SiC MOSFETs require higher gate-source voltage of 18−20 V to get into saturated mode with low on resistance. Note, that SiC MOSFETs are not compatible with standard silicon MOSFET drive conditions of 10 V and will also not reach fully saturated state when used as a retrofit for IGBTs with the typically used 15 V gate drive level!

SiC MOSFETs have a lower specific on resistance compared to Si MOSFETs with same voltage rating and therefore smaller die size for the same R_{DSon}. As the internal gate resistance is a function of the gate electrode’s sheet resistance and the die area, the gate resistance will be larger. Due to the smaller die size, capacitance values typically are also smaller, which partially compensates for the higher internal gate resistance. However, in order to achieve fast slew rates with lower switching losses, lower external gate resistor values need to be used, compared to silicon devices. To avoid unintended switching under dynamic conditions it is also highly recommended to use a negative gate drive of −3 V to −5 V for the off state.

Threshold Shift of SiC MOSFETs

If a positive gate-source voltage is applied to the device in order to turn it on by forming a channel, the electrons get attracted to the positive potential at the Si/SiO2 interface. A small concentration of the electrons will get injected into the oxide and caught by traps (resp. crystal defects) created during the oxidation process of SiO2, when creating the gate oxide layer. While moving through the oxide layer due to the electric field a fraction of the electrons get trapped in the interface traps. This leads to negatively charged centers requiring a larger potential difference in order to turn ON the device. This effect is fully reversible; applying a negative gate bias will move out the electrons out of the traps and bring back the gate threshold to the initial value. Similarly will V_{TH} decrease due to trapped holes, when a negative bias is applied [1].

During static long term reliability tests like HTGB the maximum shift will occur. At the beginning the V_{TH} shift will be bigger asymptotically reaching a maximum value, when the majority of charge traps will be occupied. It has to be pointed out, that V_{TH} shift of SiC devices is a pure physical effect and does not impact device reliability in any way. The maximum shift at the end of in HTGB testing will be in the range of 300 mV in positive and up to 150 mV direction [2].

For automotive qualification according AEC−Q101 a V_{TH} shift of less than ±20% for silicon switches is required to pass in order to make sure the gate oxide is stable. This threshold is likely not applicable to wide band gap devices. Since there is high interest from the automotive industry to use SiC devices in EV/HEV systems, it is expected, that the AEC committee will update the qualification requirements accordingly, considering the physics of wide band gap devices.

Measurements of early ON Semiconductor samples in comparison to devices from competition are shown in Figure 1.

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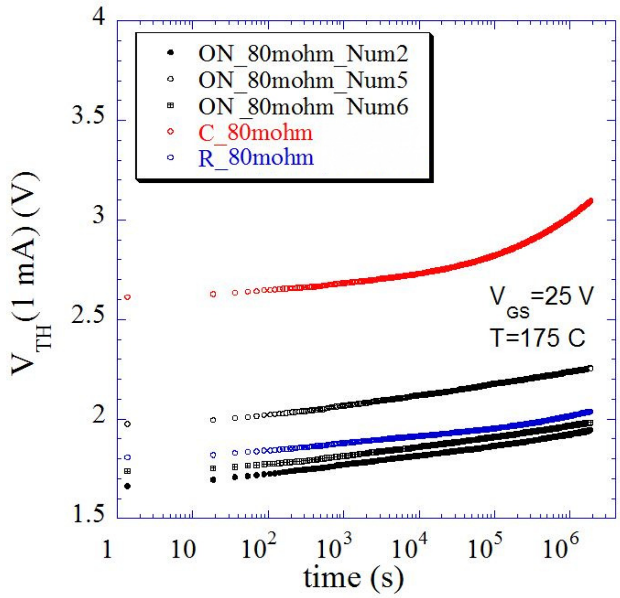

Figure 1. V_{TH} Shift Comparison with V_{GS} = 25 V @ T_C = 175°C

In a switch mode application the V_{GS} shift is dependent on the modulation index resp. the effective V_{GS}. For that reason in a real application using PWM switching, like a SMPS or onboard charger, the effect of gate threshold shift will be much smaller than in a static long term reliability test like HTGB [3].

Conclusion

SiC MOSFETs have lower turn-off losses, lower conduction losses and lower gate charge compared to silicon devices. On the other hand, their moderate transconductance combined with low threshold require higher gate voltage levels with fast rise and fall times in order to reach fully saturated state and to prevent from unintended switching. The lower gate charge aggravate the risk of overshoot and ringing requiring special attention to gate drive layout and load parasitics, especially when replacing a silicon switch with a SiC MOSFET in a given design.

Using the recommended drive levels specified in the datasheet, the shift of threshold will have neither impact on the operation performance of a power system nor its reliability.

References

[1] Mrinak K. Das, et al., “SiC MOSFET reliability update”, Material Sci. Forum 717, 2012
[2] Karaventzas, Vasilios Dimitrris, et al., “Reliability assessment of SiC Power MOSFETs From The End Users Perspective”, IEEE, 2016
[3] Fayyaz, Asad, “High temperature pulsed gate robustness testing of SiC power MOSFETs,” Microelectronics Reliability, July 2015.

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