AND9437/D

CMOS 8-BIT MICROCONTROLLER

LC870K00 SERIES USER'S MANUAL

ON Semiconductor®

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APPLICATION NOTE

Microcontroller Business Unit
ON Semiconductor

May 2016 - Rev. 0

Publication Order Number :
AND9437/D

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1. Overview

1.1 Overview

The LC870K00 series is an 8-bit microcontroller that, centered around a CPU running at a minimum bus cycle time of 83.3 ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM (onboard programmable), 384-byte RAM, two sophisticated 16-bit timers/counters (may be divided into 8-bit timers), two 8-bit timers with a prescaler, a base timer, a synchronous SIO interface, a UART (full duplex), a 12-bit 5-channel AD converter with a 12-/8-bit resolution selector, eight analog comparators, two AMP circuits, an IGBT control circuit (PPG×1), a watchdog timer, a system clock frequency divider, an internal reset circuit, and 21-source 10-vector interrupt feature.

1.2 Features

● Flash ROM

- Capable of onboard programming with a supply voltage range of 4.5 to 5.5V
- 128-byte block erase possible
- Writing in two-byte units
- 8192 × 8 bits (flash ROM)

● RAM

- 384 × 9 bits

● Minimum bus cycle time

- 83.3 ns (12MHz, VDD = 4.5 to 5.5V)

Note: The bus cycle time here refers to the ROM read speed.

● Minimum instruction cycle time (Tcyc)

- 250 ns (12MHz, VDD = 4.5 to 5.5V)

● Ports

- Normal withstand voltage I/O ports
  Ports whose input/output can be specified in 1-bit units: 9 (P00 to P07, P30)
- Dedicated PPG port: 1 (PPGO)
- Dedicated amplifier/comparator I/O ports: 9 (CMP1IA, CMP1IB, CMP2I, CMP4I, CMP45I, CMP5I, CMP6I, AMP1I, AMP2O)
- Reset pin 1 ($\overline{\text{RES}}$)
- Dedicated on-chip debugger pin 1 (OWP0)
- Regulator output pin 1 (VDC)
- Power pins 2 (VSS1, VDD1)

● Timers

- Timer 0: 16-bit timer/counter with a capture register

  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels

  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)

  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)

  Mode 3: 16-bit counter (with a 16-bit capture register)

- Timer 1: 16-bit timer/counter

  Mode 0: 8-bit timer with an 8-bit prescaler + 8-bit timer/counter

  Mode 2: 16-bit timer/counter with an 8-bit prescaler

  Mode 3: 16-bit timer with an 8-bit prescaler

- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Base timer

  <1> The clock can be selected from the system clock and timer 0 prescaler output.

  <2> An interrupt can be generated at five different time intervals.

● Analog comparators: 8 channels

- CMP1: "+" and "–" input pins.

  The output is for generating the timing for PPG output and capture timer input (INT2)
- CMP2: "+" input pin.

  "–" input is internal Vref (option: 5/12, 6/12, 7/12 VDD).

  The output sets the interrupt flag (CMP2).
- CMP3: "+" input is the output of AMP1.

  "–" input is the internal Vref (option: 1/6, 2/6, 3/6, 4/6VDD)

  The output is for PPG output control (turning off only the current cycle) and capture trigger at pulse on time, and sets the interrupt flag (CMP3).
- CMP4: "+" and "–" input pins.

  The output is for PPG output control (forced off).
- CMP5: "–" input pin.

  "+" input is also connected to the "–" input pin for CMP4.

  The output is for PPG output control (forced off).
- CMP6: "+" input pin.

  "–" input is the internal Vref (register setting: 1/6, 2/6, 3/6, 4/6 VDD)

  The output is for PPG output control (forced off) and sets the interrupt flag (CMP6).
- CMP7: "+" input is also connected to the "+" input pin for CMP2.

  "–" input is the internal Vref (option: 6/12, 7/12, 8/12 VDD).

  The output is for PPG output control (forced off) and sets the interrupt flag (CMP7).
- CMP8: "+" input is also connected to the "+" input pin for CMP3.

  "–" input is the internal Vref (register setting: 1/6, 2/6, 3/6, 4/6 VDD).

  The output is capture trigger at pulse on time and sets the interrupt flag (CMP8).

● AMP circuits: 2 channels

- AMP1: The gain (6×/8×/10×) can be selected as an option.

  Input pin (AMP1I)

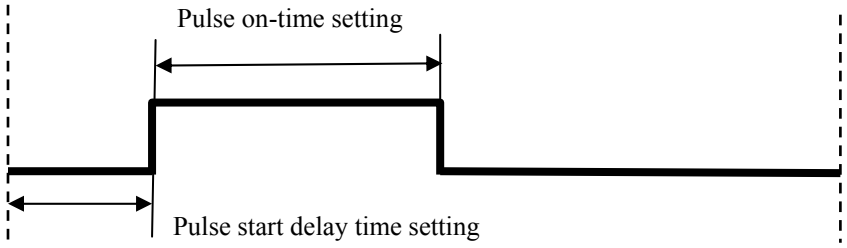
  The output is connected to CMP3 input, CMP8 input, and AMP2 input.
- AMP2: The gain (1×, 2×, or 4×) can be switched based on the register settings.

  Input is AMP 1 output.

  Output pin (AMP2O)

● IGBT control circuit (PPG2): 1 channel

- Output synchronization signal switching: Register setting (1 pulse output/continuous CMP1-output-synchronized pulse output)
- Duty control: Pulse start delay time with respect to synchronization signal and pulse on-time set by a register
- PPG output control through CMP3 to CMP7 output
- Surge detection through CMP4/5/6 output
- CMP1 output: For pulse signal timing detection
- Output polarity switching: Selectable as an option



● SIO

- SIO1: 8-bit asynchronous/synchronous serial interface

  Mode 0: Synchronous 8-bit serial I/O (2-wire configuration, 2 to 512 Tcyc transfer clock)

  Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 Tcyc transfer clock)

  Mode 3: Bus mode 2 (start detection, 8 data bits, stop detection)

● UART1

- Full duplex
- 7/8/9 data bits selectable
- 1 stop bit (2 bits in continuous data transmission)
- Built-in baudrate generator

● AD converter: 12 bits × 5 channels

- 12-/8-bit AD converter resolution selectable

● Remote control receiver circuit (multiplexed with P07/INT3/T0IN pin)

- Noise rejection function (noise filter time constant selectable from 1Tcyc/32Tcyc/128Tcyc)

● Clock output function

1) Capable of generating a clock output with a frequency of $\frac{1}{1}$, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$, or $\frac{1}{64}$ of the source oscillator clock selected as the system clock.

● Watchdog timer

- Capable of generating an internal reset signal on an overflow of a timer that runs on the internal low-speed RC oscillator clock (30 kHz).
- WDT operation on entry into HALT or HOLD mode can be selected from three modes (count operation continue, operation stop, and operation stop while retaining the count value).

● Interrupts

- 21 sources, 10 vector addresses

  <1> Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt request of the level equal to or lower than the current interrupt is not accepted.

  <2> When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the lowest vector address takes precedence.

No.	Vector	Level	Interrupt Source
1	00003H	X or L	CMP2/CMP7
2	0000BH	X or L	CMP3/CMP8
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7/CMP1TO
10	0004BH	H or L	CMP6/surge detection

- Priority levels: X > H > L
- When interrupts of the same level occur at the same time, the interrupt with the lowest vector address is given priority.

● Subroutine stack levels: Up to 192 levels (The stack is allocated in RAM.)

● High-speed multiplication/division instructions

- 16 bits × 8 bits (5 Tcyc execution time)
- 24 bits × 16 bits (12 Tcyc execution time)
- 16 bits ÷ 8 bits (8 Tcyc execution time)
- 24 bits ÷ 16 bits (12 Tcyc execution time)

● Oscillator circuits

- Internal oscillator circuits

  <1> Low-speed RC oscillator circuit: For system clock/watchdog timer (30 kHz)

  <2> Medium-speed RC oscillator circuit: For system clock (1 MHz)

  <3> High-speed RC oscillator circuit: For system clock/PPG clock (24 MHz)

  * The 12 MHz clock signal that is obtained by dividing the source clock by 2 is used as the system clock.

● System clock frequency dividing function

- Capable of running on low current.
- The minimum instruction cycle can be selected from among 250ns, 500ns, 1μs, 2μs, 4μs, 8μs, 16μs, 32μs, and 64μs (12 MHz main clock used).

● Internal reset circuit

- Power-on reset (POR) function

  <1> POR reset is generated only when power is turned on.

  <2> The POR release level can be selected from 5 levels (2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) by setting options.

- Low-voltage detection reset (LVD) function

  <1> LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.

  <2> The use/non-use of the LVD function and the low voltage detection level (5 levels: 2.31V, 2.51V, 2.81V, 3.79V, and 4.28V) can be selected by setting options.

● Standby function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.

  (1) The oscillator does not stop automatically.

  (2) There are three ways of releasing HALT mode.

  <1> Low level input to the reset pin

  <2> Generating a reset by the watchdog timer or low-voltage detection

  <3> Generating an interrupt

- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.

  (1) All RC oscillators automatically stop operation.

  (2) There are three ways of releasing HOLD mode.

  <1> Low level input to the reset pin

  <2> Generating a reset by the watchdog timer or low-voltage detection

  <3> Establishing an interrupt source at INT2 or INT4

● On-chip debugger function

- Supports software debugging with the IC mounted on the target board.

● Data security function (flash version only)

- Protects the program data stored in flash memory from unauthorized read or copy.

  Note: This data security function does not necessarily provide absolute data security.

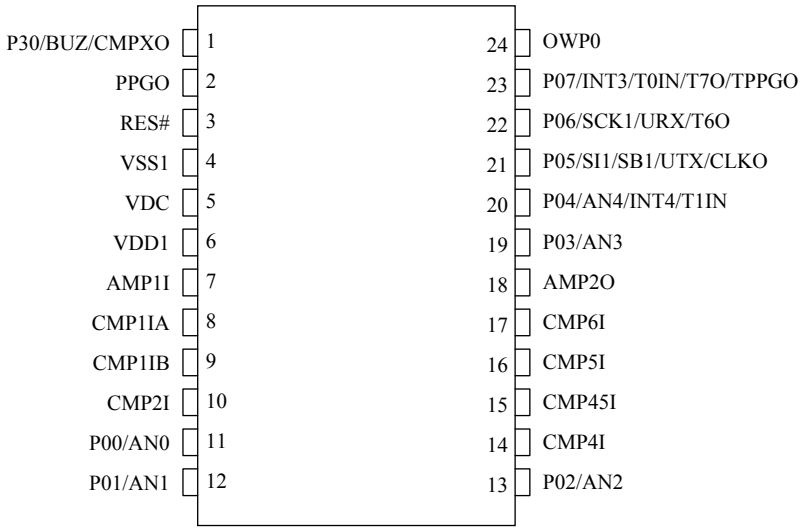
● Package form

- DIP24S (lead-free product)

● Development tools

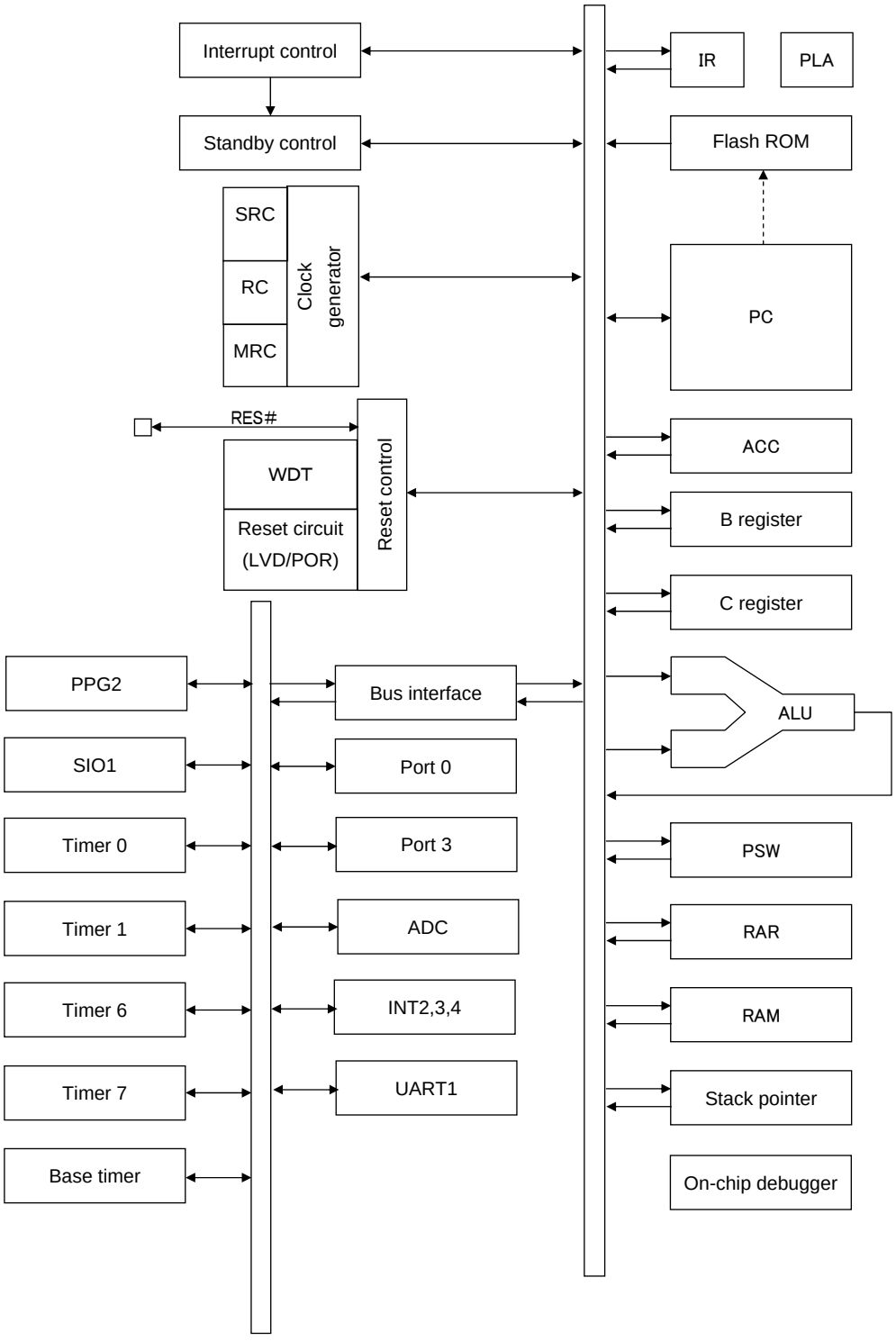
- On-chip debugger: TCB87 Type C + LC87F0K08A

1.3 Pinout



DIP24S (Pb-Free product)

1.4 System Block Diagram

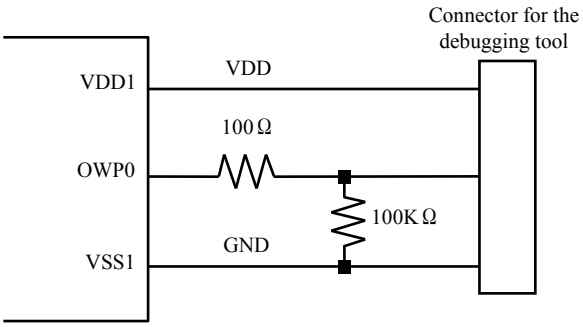


1.5 Pin Functions

<table>
<tr><th>Pin</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>VSS1</td><td>−</td><td>Power supply pin (-)</td><td>No</td></tr>
<tr><td>VDD1</td><td>−</td><td>Power supply pin (+)</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O can be specified in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units
• Pin functions
P04: INT4 input/HOLD release input t/timer 1 event input/
Timer 0L capture input/timer 0H capture input
P05: SIO1 data input/ bus I/O / UART transmit/system clock output
P06: SIO1 clock I/O /UART receive/timer 6 toggle output
P07: INT3 input (input with noise filter)/timer 0 event input/
Timer 0H capture input/timer 7 toggle output/
PPGO output for monitoring signals
P00 (AN0) to P04 (AN4): AD conversion input port
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT3</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
<tr><td>INT4</td><td>○</td><td>○</td><td>○</td><td>×</td><td>×</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30</td><td></td><td>• 1-bit I/O port
• I/O can be specified in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units
• Pin functions
P30: Buzzer output/comparator output</td><td>Yes</td></tr>
<tr><td>AMP1I</td><td>I</td><td>AMP1 input for PPG</td><td>No</td></tr>
<tr><td>AMP2O</td><td>O</td><td>AMP2 output for PPG</td><td>No</td></tr>
<tr><td>CMP1IA</td><td>I</td><td>Comparator 1 input(-) for PPG</td><td>No</td></tr>
<tr><td>CMP1IB</td><td>I</td><td>Comparator 1 input(+) for PPG</td><td>No</td></tr>
<tr><td>CMP2I</td><td>I</td><td>Comparator 2 input(+) and comparator 7 input(+) for PPG</td><td>No</td></tr>
<tr><td>CMP4I</td><td>I</td><td>Comparator 4 input(+) for PPG</td><td>No</td></tr>
<tr><td>CMP45I</td><td>I</td><td>Comparator 4 input(-) and comparator 5 input(+) for PPG</td><td>No</td></tr>
<tr><td>CMP5I</td><td>I</td><td>Comparator 5 input(-) for PPG</td><td>No</td></tr>
<tr><td>CMP6I</td><td>I</td><td>Comparator 6 input(+) for PPG</td><td>No</td></tr>
<tr><td>PPGO</td><td>O</td><td>PPG output</td><td>Yes</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input/internal reset output</td><td>No</td></tr>
<tr><td>OWP0</td><td>I/O</td><td>Dedicated debugger pin</td><td>No</td></tr>
<tr><td>VDC</td><td>O</td><td>Regulator output pin</td><td>No</td></tr>
</table>

1.6 On-chip Debugger Pin Connection Requirements

Install and connect a limiting resistor (100Ω) to the on-chip debugger dedicated pin (OWP0) on the user board and pull the pin down (100KΩ). It is recommended to install a dedicated connector to accept the cable to the debugging tool (TCB87 Type C). The connector must accommodate three lines, i.e., VSS1, OWP0, and VDD1.



1.7 Recommended Unused Pin Connections

Pin	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P30	Open	Output low
AMP1I, CMP1IA, CMP1IB, CMP2I, CMP4I, CMP45I, CMP5I, CMP6I	Pulled low with a resistor of 100kΩ or less	-
AMP2O	Open	-

1.8 Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in output mode.

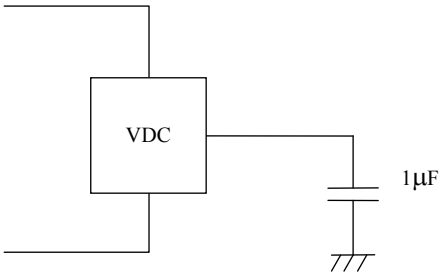
Port	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable
P30		2	N-channel open drain	Programmable
PPGO	—	1	CMOS	No
		2	N-channel open drain	No

1.9 User Option Table

Option Name	Option to be Applied on	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	○	1 bit	CMOS
				N-channel open drain
	P30	○	1 bit	CMOS
				N-channel open drain
	PPGO	○	-	CMOS
				N-channel open drain
PPG output polarity	PPGO	○	-	Inversion
				No inversion
AMP1 gain	-	○	-	6×
				8×
				10×
CMP2 Vref	-	○	-	5/12VDD
				6/12VDD
				7/12VDD
CMP3 Vref	-	○	-	1/6VDD
				2/6VDD
				3/6VDD
				4/6VDD
CMP7 Vref	-	○	-	6/12VDD
				7/12VDD
				8/12VDD
PPG on-time	Upper limit value of PPG on-time	○	-	080h
				100h
				180h
				200h
				280h
				300h
				380h
				400h
				480h
				500h
				580h
				600h
				680h
				700h
				780h
				7FFh
Low-voltage detection reset function	Detection function	○	-	Enable: Use
				Disable: Non-use
	Detection level	○	-	5-level
Power-on reset function	Power-on reset level	○	-	5-level

1.10 Regulator Output Pin Connection

The regulator output pin (VDC) must be connected to a capacitor (1 μF) on the user's board.

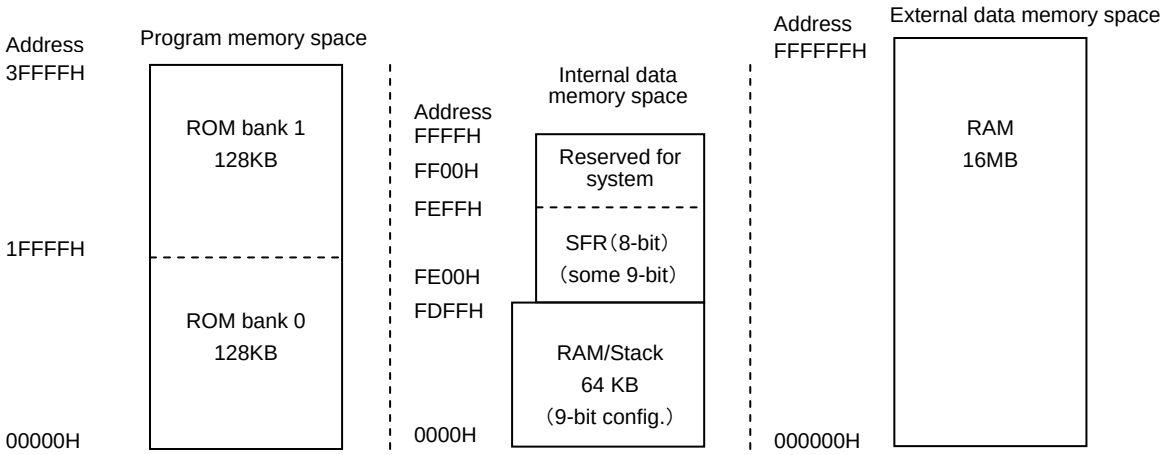


2. Internal Configuration

2.1 Memory Space

This series of microcontrollers has the following three types of memory space:

1) Program memory space: 256K bytes (128K bytes × 2 banks)
2) Internal data memory space: 64K bytes (0000H to FDFFH out of 0000H to FFFFH is shared with the stack area.)
3) External data memory space: 16M bytes



Note: SFR is the area in which special function registers such as the accumulator are allocated (see Appendix A-I).

Figure 2.1.1 Types of Memory Space

2.2 Program Counter (PC)

The program counter (PC) is made up of 17 bits and a bank flag BNK. The value of BNK determines the bank. The low-order 17 bits of the PC allows linear access to the 128K ROM space in the current bank.

Normally, the PC advances automatically in the current bank on each execution of an instruction. Bank switching is accomplished by executing a Return instruction after pushing necessary addresses onto the stack. When executing a branch or subroutine instruction, when accepting an interrupt, or when a reset is generated, the value corresponding to each operation is loaded into the PC.

Table 2.2.1 lists the values that are loaded into the PC when the respective operations are performed.

Table 2.2.1 Values Loaded in the PC

Operation			PC Value	BNK Value
Inter-rupt	Reset		00000H	0
	CMP2/CMP7		00003H	0
	CMP3/CMP8		0000BH	0
	INT2/T0L/INT4		00013H	0
	INT3/base timer		0001BH	0
	T0H		00023H	0
	T1L/T1H		0002BH	0
	UART1 receive		00033H	0
	SIO1/UART1 transmit		0003BH	0
	ADC/T6/T7/CMP1TO		00043H	0
	CMP6/surge detection		0004BH	0
Unconditional branch instructions		JUMP a17	PC=a17	Unchanged
		BR r12	PC=PC+2+r12[-2048 to +2047]	Unchanged
Conditional branch instructions		BE, BNE, DBNZ, DBZ, BZ, BNZ, BZW, BNZW, BP, BN, BPC	PC=PC+nb+r8[-128 to +127] nb: Number of instruction bytes	Unchanged
Call instructions		CALL a17	PC=a17	Unchanged
		RCALL r12	PC=PC+2+r12[-2048 to +2047]	Unchanged
		RCALLA	PC=PC+1+Areg[0 to +255]	Unchanged
Return instructions		RET, RETI	PC16 to 08=(SP) PC07 to 00=(SP-1) (SP) denotes the contents of RAM address designated by the value of the stack pointer SP.	BNK is set to bit 8 of (SP-1).
Standard instructions		NOP, MOV, ADD, …	PC=PC+nb nb: Number of instruction bytes	Unchanged

2.3 Program Memory (ROM)

This series of microcontrollers has a program memory space of 256K bytes but the size of the ROM that is actually incorporated in the microcontroller varies with the type of the microcontroller. The ROM table look-up instruction (LDC) can be used to reference all ROM data within the bank. Of the ROM space, the 256 bytes in ROM bank 0 (1FF00H to 1FFFFH for this series) are reserved as the option area. Consequently, this area is not available as a program area.

2.4 Internal Data Memory (RAM)

This series of microcontrollers has an internal data memory space of 64K bytes but the size of the RAM that is actually incorporated in the microcontroller varies with the type of the microcontroller. Nine bits are used to access addresses 0000H to FDFFH of the 128K ROM space and 8 or 9 bits are used to access addresses FE00H to FFFFH. The 9th bit of RAM is implemented by bit 1 of the PSW and can be read and written.

The 128 bytes of RAM from 0000H to 007FH are paired to form 64 2-byte indirect address registers. The bit length of these indirect registers is normally 16 bits (8 bits × 2). When they are used by the ROM table look-up instruction (LDC), however, their bit length is set to 17 bits (9 high-order bits + 8 low-order bits).

As shown in Figure 2.4.1, the available instructions vary depending on the RAM address. The efficiency of the ROM used and a higher execution speed can be attempted using these instructions properly.

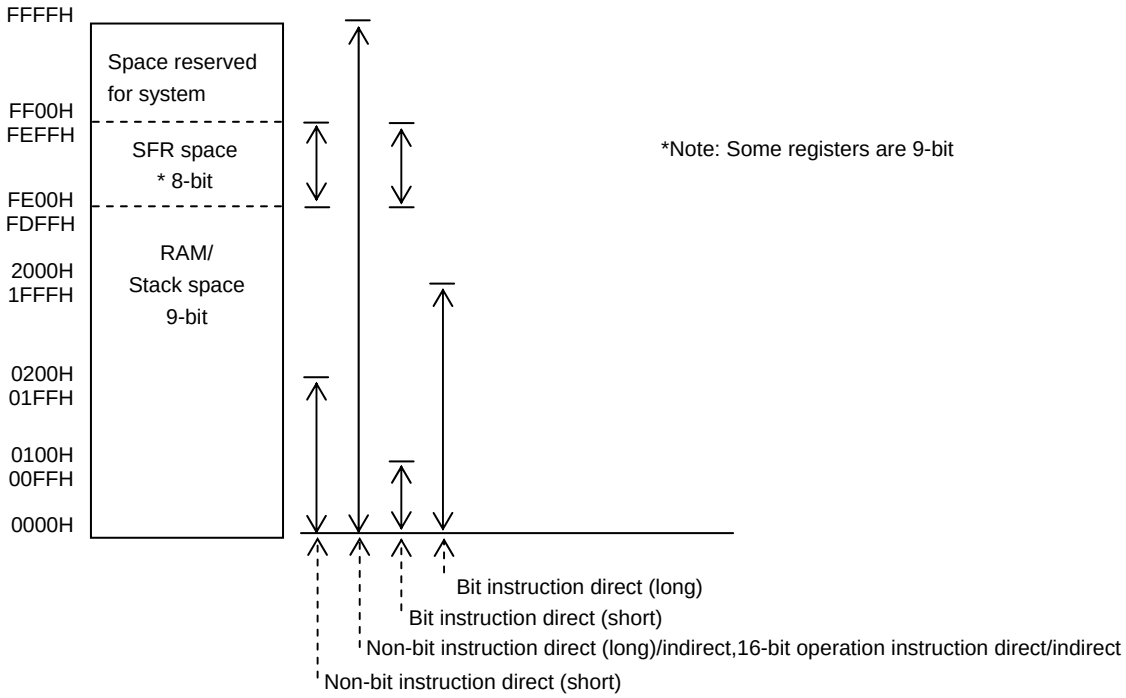


Figure 2.4.1 RAM Addressing Map

When the value of the PC is stored in RAM during the execution of a subroutine call instruction or interrupt, assuming that SP represents the current value of the stack pointer, the value of BNK and the low-order 8 bits of the (17-bit) PC are stored in RAM address SP + 1 and the high-order 9 bits in SP + 2, after which SP is set to SP + 2.

2.5 Accumulator/A Register (ACC/A)

The accumulator (ACC), also called the A register, is an 8-bit register that is used for data computation, transfer, and I/O processing. It is allocated to address FE00H of the internal data memory space and initialized to 00H on a reset.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE00	0000 0000	R/W	AREG	AREG7	AREG6	AREG5	AREG4	AREG3	AREG2	AREG1	AREG0

2.6 B Register (B)

The B register is combined with the ACC to form a 16-bit arithmetic register during the execution of a 16-bit arithmetic instruction. During a multiplication or division instruction, the B register is used with the ACC and C register to store the results of computation. In addition, during an external memory access instruction (LDX or STX), the B register designates the high-order 8 bits of the 24-bit address.
The B register is allocated to address FE01H of the internal data memory space and initialized to 00H on a reset.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE01	0000 0000	R/W	BREG	BREG7	BREG6	BREG5	BREG4	BREG3	BREG2	BREG1	BREG0

2.7 C Register (C)

The C register is used with the ACC and B register to store the results of computation during the execution of a multiplication or division instruction. In addition, during a C register offset indirect instruction, the C register stores the offset data (-128 to +127) to the contents of an indirect register.
The C register is allocated to address FE02H of the internal data memory space and initialized to 00H on a reset.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE02	0000 0000	R/W	CREG	CREG7	CREG6	CREG5	CREG4	CREG3	CREG2	CREG1	CREG0

2.8 Program Status Word (PSW)

The program status word (PSW) is made up of flags that indicate the status of computation results, a flag to access the 9th bit of RAM, and a flag to designate the bank during the LDCW instruction. The PSW is allocated to address FE06H of the internal data memory space and initialized to 00H on a reset.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE06	0000 0000	R/W	PSW	CY	AC	PSWB5	PSWB4	LDCBNK	OV	P1	PARITY

CY (bit 7): Carry flag

CY is set (to 1) when a carry occurs as the result of a computation and cleared (to 0) when no carry occurs. There are following 4 types of carries:

1) Carry resulting from an addition
2) Borrow resulting from a subtraction
3) Borrow resulting from a comparison
4) Carry resulting from a rotation

There are some instructions that do not affect this flag at all.

AC (bit 6): Auxiliary carry flag

AC is set (to 1) when a carry or borrow occurs in bit 3 (bit 3 of the high-order byte during a 16-bit computation) as the result of an addition or subtraction and cleared (to 0) otherwise.

There are some instructions that do not affect this flag at all.

PSWB5, PSWB4 (bits 5 and 4): User bits

These bits can be read and written through instructions. They can be used by the user freely.

LDCBNK (bit 3): Bank flag for the table look-up instruction (LDCW)

This bit designates the ROM bank to be specified when reading the program ROM with a table look-up instruction.

(0: ROM-ADR = 0 to 1FFFF, 1: ROM-ADR = 20000 to 3FFFF)

OV (bit 2): Overflow flag

OV is set (to 1) when an overflow occurs as the result of an arithmetic operation and cleared (to 0) otherwise. An overflow occurs in the following cases:

1) When MSB is used as the sign bit and when the result of negative number + negative number or negative number – positive number is a positive number
2) When MSB is used as the sign bit and when the result of positive number + positive number or positive number – negative number is a negative number

3) When the high-order 8 bits of a 16 bits × 8 bits multiplication is nonzero
4) When the high-order 16 bits of a 24 bits × 16 bits multiplication is nonzero
5) When the divisor of a division is 0

There are some instructions that do not affect this flag at all.

P1 (bit 1): RAM bit 8 data flag

P1 is used to manipulate bit 8 of 9-bit internal data RAM (0000H to FDFFH). Its behavior varies depending on the instruction executed. See Table 2.4.1 for details.

PARITY (bit 0): Parity flag

This bit shows the parity of the accumulator (A register). The parity flag is set (to 1) when there is an odd number of 1's in the A register. It is cleared (to 0) when there is an even number of 1's.

2.9 Stack Pointer (SP)

LC870000 series microcontrollers can use RAM addresses 0000H to FDFFH as a stack area. The size of RAM, however, varies depending on the microcontroller type. The SP is 16 bits long and made up of two registers: SPL (at address FE0A) and SPH (at address FE0B). It is initialized to 0000H on a reset.
The SP is incremented by 1 before data is saved in stack memory and decremented by 1 after the data is restored from stack memory.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0A	0000 0000	R/W	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
FE0B	0000 0000	R/W	SPH	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP8

The value of the SP changes as follows:

1) When the PUSH instruction is executed: SP = SP + 1, RAM (SP) = DATA
2) When the CALL instruction is executed: SP = SP + 1, RAM (SP) = ROMBANK + ADL
   SP = SP + 1, RAM (SP) = ADH
3) When the POP instruction is executed: DATA = RAM (SP), SP = SP - 1
4) When the RET instruction is executed: ADH = RAM (SP), SP = SP - 1
   ROM BANK + ADL = RAM(SP), SP = SP - 1

2.10 Indirect Addressing Registers

LC870000 series microcontrollers are provided with three addressing schemes ([Rn], [Rn + C], [off]), which use the contents of indirect registers (indirect addressing modes). (See Section 2.11 for the addressing modes.) These addressing modes use 64 2-byte indirect registers (R0 to R63) allocated to RAM addresses 0 to 7EH. The indirect registers can also be used as general-purpose registers (e.g., for saving 2-byte data). Naturally, these addresses can be used as ordinary RAM (in a 1-byte (9 bits) units) if they are not used as indirect registers. R0 to R63 are "system reserved words" to the assembler and need not be defined by the user.

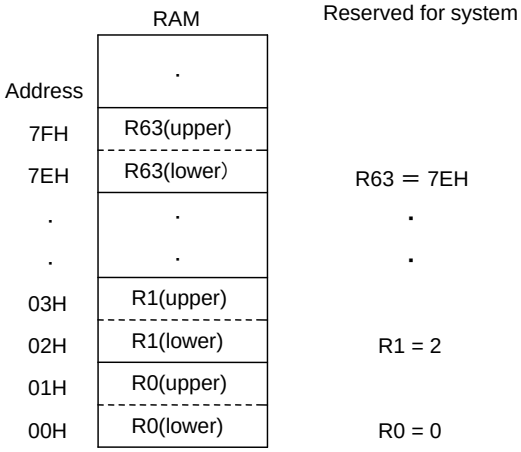


Figure 2.10.1 Allocation of Indirect Registers

2.11 Addressing Modes

LC870000 series microcontrollers support the following seven addressing modes:

1) Immediate (Immediate data refers to data whose value has been established at program preparation (assembly) time.)
2) Indirect register (Rn) indirect ($0 \leqq n \leqq 63$)
3) Indirect register (Rn) + C register indirect ($0 \leqq n \leqq 63$)
4) Indirect register (R0) + Offset value indirect
5) Direct
6) ROM table look-up
7) External data memory access

The rest of this section describes these addressing modes.

2.11.1 Immediate Addressing (#)

The immediate addressing mode allows 8-bit (1-byte) or 16-bit (1-word) immediate data to be handled. Examples are given below.

Examples:

```
      LD      #12H;       Loads the accumulator with byte data (12H).
L1:   LDW     #1234H;     Loads the BA register pair with word data (1234H).
      PUSH    #34H;       Loads the stack with byte data (34H).
      ADD     #56H;       Adds byte data (56H) to the accumulator.
      BE      #78H, L1;   Compares byte data (78H) with the accumulator for a branch.
```

2.11.2 Indirect Register Indirect Addressing ([Rn])

In indirect register indirect addressing mode, it is possible to select one of the indirect registers (R0 to R63) and use its contents to designate an address in RAM or SFR. When the selected register contains, for example, "FE02H," it designates the C register.

Example: When R3 contains "123H" (RAM address 6: 23H, RAM address 7: 01H)

```
      LD    [R3];      Transfers the contents of RAM address 123H to the accumulator.
L1:   STW   [R3];      Transfers the contents of the BA register pair to RAM address 123H.
      PUSH  [R3];      Saves the contents of RAM address123H in the stack.
      SUB   [R3];      Subtracts the contents of RAM address 123H from the accumulator.
      DBZ   [R3], L1;  Decrements the contents of RAM address 123H by 1 and causes a branch if
                       zero.
```

2.11.3 Indirect Register + C Register Indirect Addressing ([Rn, C])

In the indirect register + C register indirect addressing mode, the result of adding the contents of one of the indirect registers (R0 to R63) to the contents of the C register (-128 to +127 with MSB being the sign bit) designates an address in RAM or SFR. For example, if the selected indirect register contains "FE02H" and the C register contains "FFH (-1)," the address "B register (FE02H + (-1) = FE01H" is designated.

Examples: When R3 contains "123H" and the C register contains "02H"

```
      LD    [R3, C];     Transfers the contents of RAM address 125H to the accumulator.
L1:   STW   [R3, C];     Transfers the contents of the BA register pair to RAM address 125H.
      PUSH  [R3, C];     Saves the contents of RAM address 125H in the stack.
      SUB   [R3, C];     Subtracts the contents of RAM address 125H from the accumulator.
      DBZ   [R3, C], L1; Decrements the contents of RAM address 125H by 1 and causes a branch if
                         zero.
```

<Notes on this addressing mode >

The internal data memory space is divided into three closed functional areas as explained in Section 2.1, namely, 1) system reserved area (FF00H to FFFFH), 2) SFR area (FE00H to FEFFH), and 3) RAM/stack area (0000H to FDFFH). Consequently, it is not possible to point to a different area using the value of the C register from the basic area designated by the contents of Rn. For example, if the instruction "LD [R5,C]" is executed when R5 contains "0FDFFH" and the C register contains "1," since the basic area is 3) RAM/stack area (0000H to FDFFH), the intended address "0FDFFH+1 = 0FE00H" lies outside the basic area and "0FFH" is consequently placed in the ACC as the result of LD. If the instruction "LD [R5,C]" is executed when R5 contains "0FEFFH" and the C register contains "2," since the basic area is 2) SFR area (FE00H to FEFFH), the intended address "0FEFFH+2 = 0FF01H" lies outside the basic area. In this case, since SFR is confined in an 8-bit address space, the part of the address data addressing outside the 8-bit address space is ignored and the contents of 0FE01H (B register) are placed in the ACC as the result of the computation "0FF01H&0FFH+0FE00H = 0FE01H."

2.11.4 Indirect Register (R0) + Offset Value Indirect Addressing ([off])

In this addressing mode, the results of adding the 7-bit signed offset data off (-64 to + 63) to the contents of the indirect register R0 designate an address in RAM or SFR. If R0 contains "FE02H" and off has a value of "7EH(-2)," for example, the A register (FE02H + (-2) = FE00H) is designated.

Examples: When R0 contains "123H" (RAM address 0: 23H, RAM address 1: 01H)

```
      LD      [10H];      Transfers the contents of RAM address 133H to the accumulator.
L1:   STW     [10H];      Transfers the contents of the BA register pair to RAM address 133H.
      PUSH    [10H];      Saves the contents of RAM address 133H in the stack.
      SUB     [10H];      Subtracts the contents of RAM address 133H from the accumulator.
      DBZ     [10H], L1;  Decrements the contents of RAM address 133H by 1 and causes a branch if
                          zero.
```

<Notes on this addressing mode>

The internal data memory space is divided into three closed functional areas as explained in Section 2.1, namely, 1) system reserved area (FF00H to FFFFH), 2) SFR area (FE00H to FEFFH), and 3) RAM/stack area (0000H to FDFFH). Consequently, it is not possible to point to a different area using an offset value from the basic area designated by the contents of R0. For example, if the instruction "LD [1]" is executed when R0 contains "0FDFFH," since the basic area is 3) RAM/stack area (0000H to FDFFH), the intended address "0FDFFH+1 = 0FE00H" lies outside the basic area and "0FFH" is placed in the ACC as the results of LD. If the instruction "LD [2]" is executed when R0 contains "0FEFFH," since the basic area is 2) SFR (FE00H to FEFFH), the intended address "0FEFFH+2 = 0FF01H" lies outside the basic area. In this case, since SFR is confined in an 8-bit address space, the part of the address data addressing outside the 8-bit address space is ignored and the contents of 0FE01H (B register) are placed in the ACC as the result of computation "0FF01H&0FFH+0FE00H = 0FE01H."

2.11.5 Direct Addressing (dst)

Direct addressing mode allows a RAM or SFR address to be specified directly in an operand. In this addressing mode, the assembler automatically generates the optimum instruction code from the address specified in the operand (the number of instruction bytes varies according to the address specified in the operand). Long (middle) range instructions (identified by an "L (M)" at the end of the mnemonic) are available to make the byte count of instructions constant (align instructions with the longest one).

Examples:

```
      LD      123H;       Transfers the contents of RAM address 123H to the accumulator
                          (2-byte instruction).
      LDL     123H;       Transfers the contents of RAM address 123H to the accumulator
                          (3-byte instruction).
L1:   STW     123H;       Transfers the contents of the BA register pair to RAM address 123H.
      PUSH    123H;       Saves the contents of RAM address 123H in the stack.
      SUB     123H;       Subtracts the contents of RAM address 123H from the accumulator.
      DBZ     123H, L1;   Decrements the contents of RAM address 123H by 1 and causes a branch if
                          zero.
```

2.11.6 ROM Table Look-up Addressing

The LC870000 series microcontrollers can read 2-byte data into the BA register pair at once using the LDCW instruction. Three addressing modes [Rn], [Rn, C], and [off] are available for this purpose. (In this case only, Rn is configured as 17-bit registers. (128K-byte space))

For models with banked ROM, it is possible to reference the ROM data in the ROM bank (128K bytes) identified by the LDCBNK flag (bit 3) in the PSW. Consequently, when looking into the ROM table on a series model with banked ROM, execute the LDCW instruction after switching the bank using the SET1 or CLR1 instruction so that the LDCBNK flag designates the ROM bank where the ROM table resides.

Examples:

```
TBL: DB      34H
     DB      12H
     DW      5678H
     •       •
     •       •
     LDW     #TBL;              Loads the BA register pair with the TBL address.
     CHGP3   (TBL >> 17) & 1;   Loads LDCBNK in PSW with bit 17 of the TBL address. (Note 1)
     CHGP1   (TBL >> 16) & 1;   Loads P1 in PSW with bit 16 of the TBL address.
     STW     R0;                Loads indirect register R0 with the TBL address (bits 16 to 0).
     LDCW    [1];               Reads the ROM table (B=78H, ACC=12H).
     MOV     #1, C;             Loads the C register with 01H.
     LDCW    [R0, C];           Reads the ROM table (B=78H, ACC=12H).
     INC     C;                 Increments the C register by 1.
     LDCW    [R0, C]:           Reads the ROM table (B=56H, ACC=78H).
```

Note 1: LDCBNK (bit 3) of PSW needs to be set up only for models with banked ROM.

2.11.7 External Data Memory Addressing

LC870000 series microcontrollers can access external data memory spaces of up to 16M bytes (24 bits) using the LDX and STX instructions. To designate a 24-bit space, specify the contents of the B register (8 bits) as the highest-order byte of the address and the contents (16 bits) of (Rn), (Rn) + (C), or (R0) + off (either one) as the low-order bytes of the address.

Examples:

```
LDW     #3456H;    Sets up the low-order 16 bits.
STW     R5;        Loads the indirect register R5 with the low-order 16 bits of the address.
MOV     #12H, B;   Sets up the high-order 8 bits of the address.
LDX     [1];       Transfers the contents of external data memory (address 123456H) to the
                   accumulator.
```

2.12 Wait Sequence

2.12.1 Wait Sequence Occurrence

This series of microcontrollers does not have a wait sequence that automatically suspends execution of instructions.

2.12.2 What is a Wait Sequence?

1) When a wait request occurs out of a factor explained in Subsection 2.12.1, the CPU suspends the execution of the instruction for one cycle, during which the required data is transferred. This is called a wait sequence.
2) The peripheral circuits such as timers and PWM continue processing during the wait sequence.
3) A wait sequence extends over no more than two cycles.
4) The microcontroller performs no wait sequence when it is in HALT or HOLD mode.
5) Note that one cycle of discrepancy is introduced between the progress of the program counter and time once a wait sequence occurs.

Table 2.4.1 Chart of State Transitions of Bit 8 (RAM / SFR) and P1

Instruction	Bit 8 (RAM/SFR)	P1 (PSW Bit 1)	Remarks
LD#/LDW#	—	—	
LD	—	P1←REG8	
LDW	—	P1←REGH8	
ST	REG8←P1	—	
STW	REGL8, REGH8←P1	—	
MOV	REG8←P1	—	
PUSH#	RAM8←P1	—	
PUSH	RAM8←REG8	P1←REG8	
PUSHW	RAMH8←REGH8, RAML8←REGL8	P1←REGH8	
PUSH_P	RAM8←Pl	—	
PUSH_BA	RAMH8←P1, RAML8←P1	—	
POP	REG8←RAM8	P1←RAM8	P1←bit1 when PSW is popped
POPW	REGH8←RAMH8, REGL8←RAML8	Pl←RAMH8	P1←bit1 when high-order address of PSW is popped
POP_P	—	P1←RAMl (bit l)	Bit 8 ignored
POP_BA	—	P1←RAMH8	
XCH	REG8↔P1	Same as left.	
XCHW	REGH8←P1, REGL8←Pl, P1←REGH8	Same as left.	
INC	INC 9 bits	P1←REG8 after computation	INC 9 bits
INCW	INC 17 bits, REGL8←lower byte of CY	P1←REGH8 after computation	INC 17 bits
DEC	DEC 9 bits	P1←REG8 after computation	DEC 9 bits
DECW	DEC 17 bits REGL8← lower byte of CY inverted	P1←REGH8 after computation	DEC 17 bits
DBNZ	DEC 9 bits	P1←REG8	DEC 9 bits, check low-order 8 bits
DBZ	DEC 9 bits	P1←REG8	DEC 9 bits, check low-order 8 bits
SET1	—	—	
NOT1	—	—	
CLR1	—	—	
BPC	—	—	
BP	—	—	
BN	—	—	
MUL24 /DIV24	RAM8←"1"	—	Bit 8 of RAM address for storing results is set to 1.
FUNC	—	—	

Note: A "1" is read if the processing target is an 8-bit register (no bit 8).

Legends:

REG8: Bit 8 of a RAM or SFR location
REGH8/REGL8: Bit 8 of the high-order byte of a RAM or SFR location /bit 8 of the low-order byte
RAM8: Bit 8 of a RAM location
RAMH8/RAML8: Bit 8 of the high-order byte of a RAM location/bit 8 of the low-order byte

3. Peripheral System Configuration

This chapter describes the internal functional blocks (peripheral system) of the LC870K00 series microcontrollers except the CPU core, RAM, and ROM. Port block diagrams are provided in Appendix A-II for reference.

3.1 Port 0

3.1.1 Overview

Port 0 is an 8-bit I/O port equipped with programmable pull-up resistors. It is made up of a data latch, a data direction register, and a control circuit. The I/O direction and the pull-up resistor are set by the data direction register in 1-bit units.

As a user option, either CMOS output with a programmable pull-up resistor or N-channel open drain output with a programmable pull-up resistor can be selected as the output type in 1-bit units.

3.1.2 Functions

1) I/O port (8 bits: P00 to P07)
   - The port output data is controlled by the port 0 data latch (P0:FE40) and the I/O direction is controlled by the port 0 data direction register (P0DDR:FE41).
   - Each port is provided with a programmable pull-up resistor.

2) Interrupt input pin function
   - P07 is assigned to INT3 and used to detect a low or high edge, or both edges and sets the interrupt flag.
   - P04 is assigned to INT4 and used to detect a low or high edge, or both edges and sets the interrupt flag.

3) Timer 0 count input function

   A count signal is sent to timer 0 each time a signal change that sets the interrupt flag is supplied to P07 (INT3).

4) Timer 0L capture input function

   A timer 0L capture signal is generated each time a signal change that sets the interrupt flag is supplied to P04 (INT4).

5) Timer 0H capture input function

   A timer 0H capture signal is generated each time a signal change that sets the interrupt flag is supplied to a port selected from P04 (INT4) and P07 (INT3).

6) HOLD mode release function

- When both of the interrupt flag and interrupt enable flag are set by INT4, a HOLD mode release signal is generated, releasing HOLD mode. The CPU then enters HALT mode. When the interrupt request is accepted, the CPU switches from HALT mode to normal operating mode.
- When a signal change that sets an interrupt flag is input to INT4 in HOLD mode, the interrupt flag is set. In this case, HOLD mode is released if the corresponding interrupt enable flag is set. The interrupt flag, however, cannot be set by a rising edge occurring when INT4 data that is established when HOLD mode is entered is in the high state, or by a falling edge occurring when INT 4 data that is established when HOLD mode is entered is in the low state. Consequently, to release HOLD mode with INT4, it is recommended that INT4 be used in both-edge interrupt mode.

7) Multiplexed pin function

P04 is also used as the INT4 input, P05 and P06 as the SIO1 input/output and UART input/output, respectively, P05 as the system clock output, P06 as the timer 6 toggle output, P07 as the INT3 input, timer 7 toggle output, and PPGO monitor output. P00 to P04 are also used as the analog input channels AN0 to AN4, respectively. The description of the PPGO monitor output is shown in the PPG2 section.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE40	0000 0000	R/W	P0	P07	P06	P05	P04	P03	P02	P01	P00
FE41	0000 0000	R/W	P0DDR	P07DDR	P06DDR	P05DDR	P04DDR	P03DDR	P02DDR	P01DDR	P00DDR
FE42	00HH 0000	R/W	P0FCR	T7OE	T6OE	-	-	CLKOEN	CKODV2	CKODV 1	CKODV0
FE4A	HHHH 0000	R/W	I45CR	-	-	-	-	INT4HEG	INT4LEG	INT4IF	INT4IE
FE4B	HHHH HH00	R/W	I45SL	-	-	-	-	-	-	I4SL1	I4SL0
FE5E	0000 0000	R/W	I23CR	INT3HEG	INT3LEG	INT3IF	INT3IE	INT2HEG	INT2LEG	INT2IF	INT2IE
FE5F	0000 0000	R/W	ISL	ST0HCP	ST0LCP	BTIMC1	BTIMC0	BUZON	NFSEL	NFON	ST0IN
FE77	H00H HHHH	R/W	P0FCNT	-	P06FCNT	P05FCNT	-	-	-	-	-

3.1.3 Related Registers

3.1.3.1 Port 0 data latch (P0)

1) The port 0 data latch is an 8-bit register that controls the port 0 output data.
2) When this register is read with an instruction, data at pins P00 to P07 is read in. If P0 (FE40) is manipulated using a NOT1, CLR1, SET1, DBZ, DBNZ, INC, or DEC instruction, the contents of the register are referenced instead of the data at port pins.
3) Port 0 data can always be read regardless of the I/O state of the port.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE40	0000 0000	R/W	P0	P07	P06	P05	P04	P03	P02	P01	P00

3.1.3.2 Port 0 data direction register (P0DDR)

1) This register is an 8-bit register that controls the I/O direction of port 0 in 1-bit units. Port P0n is placed into output mode when bit P0nDDR is set to 1 and into input mode when bit P0nDDR is set to 0.

2) Port P00 to P07 becomes an input with a pull-up resistor when bit P0nDDR is set to 0 and bit P0n of the port 0 data latch is set to 1.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE41	0000 0000	R/W	P0DDR	P07DDR	P06DDR	P05DDR	P04DDR	P03DDR	P02DDR	P01DDR	P00DDR

Register Data		Port P0n State		Internal Pull-up Resistor
P0n	P0nDDR	Input	Output	
0	0	Enabled	Open	OFF
1	0	Enabled	Internal pull-up resistor	ON
0	1	Disabled	Low	OFF
1	1	Disabled/enabled	High/open (CMOS/N-channel open drain	OFF

3.1.3.3 Port 0 function control register (P0FCR)

1) This register is a 6-bit register that controls the multiplexed pin output of port 0.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE42	00HH 0000	R/W	P0FCR	T7OE	T6OE	-	-	CLKOEN	CKODV2	CKODV1	CKODV0

T7OE (bit 7):

This bit controls the output data of pin P07.

This bit is disabled when P07 is in input mode.

When P07 is in output mode:

0: Outputs the value of the port data latch.

1: Outputs the OR of the waveform that toggles at the period of timer 7 and the value of the port data latch.

T6OE (bit 6):

This bit controls the output data of pin P06.

Register Data			P06 Pin Output in Output Mode (P06DDR=1)
P06FCNT	T6OE	P06	
0	0	x	Value of port data latch (P06)
0	1	0	Timer 6 toggle output
0	1	1	High output
1	0	0	SIO1 clock output
1	0	1	High output
1	1	0	OR of timer 6 toggle output and SIO1 clock output
1	1	1	High output

CLKOEN (bit 3):

This bit controls the output data of pin P05.

Register Data			P05 Pin Output in Output Mode (P05DDR=1)
P05FCNT	CLKOEN	P05	
0	0	x	Value of port data latch (P05)
0	1	0	System clock output
0	1	1	High output
1	0	0	SIO1 data output
1	0	1	High output
1	1	0	OR of system clock output and SIO1 data output
1	1	1	High output

CKODV2 (bit 2)

CKODV1 (bit 1)

CKODV0 (bit 0)

These bits define the frequency of the system clock to be placed at P05.

000: Frequency of source oscillator selected as system clock

001: 1/2 of frequency of source oscillator selected as system clock

010: 1/4 of frequency of source oscillator selected as system clock

011: 1/8 of frequency of source oscillator selected as system clock

100: 1/16 of frequency of source oscillator selected as system clock

101: 1/32 of frequency of source oscillator selected as system clock

110: 1/64 of frequency of source oscillator selected as system clock

111: Inhibited

<Notes on the use of the clock output function>

Follow notes 1) to 3) given below when using the clock output function. Anomalies may be observed in the waveform of the port clock output if these notes are violated.

1) Do not change the frequency of the clock output divider setting when CLKOEN (bit 3) is set to 1.
   → Do not change the settings of CKODV2 to CKODV0 (bits 2 to 0).
2) Do not change the system clock selection when CLKOEN (bit 3) is set to 1.
   → Do not change the setting of CLKCB4 (bit 4) of the OCR register.
3) CLKOEN will not go to 0 immediately even when the user executes an instruction that loads the P0FCR register with data that sets the state of CLKOEN from 1 to 0. CLKOEN is set to 0 at the end of the clock that is being output (on detection of the falling edge of the clock). Accordingly, when changing the clock frequency division setting or changing the system clock selection after setting CLKOEN to 0 with an instruction, be sure to read the CLKOEN value in advance and make sure that it is 0.

3.1.3.4 Port 0 function control register 2 (P0FCNT)

1) This register is a 2-bit register that controls the port 0 multiplexed outputs of port 0.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE77	H00H HHHH	R/W	P0FCNT	-	P06FCNT	P05FCNT	-	-	-	-	-

P06FCNT (bit 6)

This bit controls the output data of pin P06.

P05FCNT (bit 5)

This bit controls the output data of pin P05.

3.1.3.5 External interrupt 4 control register (I45CR)

1) This register is a 4-bit register that controls the external interrupt 4.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE4A	HHHH 0000	R/W	I45CR	-	-	-	-	INT4HEG	INT4LEG	INT4IF	INT4IE

INT4HEG (bit 3): INT4 rising edge detection control

INT4LEG (bit 2): INT4 falling edge detection control

INT4HEG	INT4LEG	INT4 Interrupt Conditions
0	0	No edge detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

INT4IF (bit 1): INT4 interrupt source flag

This bit is set when the conditions specified by INT4HEG, INT4LEG are satisfied. When this bit and the INT4 interrupt request enable bit (INT4IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

The interrupt flag, however, cannot be set by a rising edge occurring when INT4 data that is established when HOLD mode is entered is in the high state, or by a falling edge occurring when INT4 data that is established when HOLD mode is entered is in the low state. Consequently, to release HOLD mode with INT4, it is recommended that INT4 be used in both-edge interrupt mode.

This bit must be cleared with an instruction as it is not cleared automatically.

INT4IE (bit 0): INT4 interrupt request enable

When this bit and INT4IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

3.1.3.6 External interrupt 4 pin select register (I45SL)

1) This register is a 2-bit register used to select the pin for the external interrupt 4.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE4B	HHHH HH00	R/W	I45SL	-	-	-	-	-	-	I4SL1	I4SL0

I4SL1 (bit 1):

I4SL0 (bit 0): INT4 pin function select

When the data change specified in the external interrupt 4 control register (I45CR) is given to the pin that is assigned to INT4, a timer 1 count clock input and timer 0 capture signal are generated.

I4SL1	I4SL0	Function other than INT4 Interrupt
0	0	None
0	1	Timer 1 count clock input
1	0	Timer 0L capture signal input
1	1	Timer 0H capture signal input

3.1.3.7 External interrupt 2/3 control register (I23CR)

1) This register is an 8-bit register that controls the external interrupts 2 and 3.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5E	0000 0000	R/W	I23CR	INT3HEG	INT3LEG	INT3IF	INT3IE	INT2HEG	INT2LEG	INT2IF	INT2IE

INT3HEG (bit 7): INT3 rising edge detection control

INT3LEG (bit 6): INT3 falling edge detection control

INT3HEG	INT3LEG	INT3 Interrupt Conditions
0	0	No edge detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

INT3IF (bit 5): INT3 interrupt source flag

This bit is set when the conditions specified by INT3HEG and INT3LEG are satisfied. When this bit and the INT3 interrupt request enable bit (INT3IE) are set to 1, an interrupt request to vector address 001BH is generated.

This bit must be cleared with an instruction as it is not cleared automatically.

INT3IE (bit 4): INT3 interrupt request enable

When this bit and INT3IF are set to 1, an interrupt request to vector address 001BH is generated.

INT2HEG (bit 3): INT2 rising edge detection control

INT2LEG (bit 2): INT2 falling edge detection control

INT2HEG	INT2LEG	INT2 Interrupt Conditions (Comparator 1 Output Data)
0	0	No edge detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

INT2IF (bit 1): INT2 interrupt source flag

This bit is set when the conditions specified by INT2HEG and INT2LEG are satisfied. When this bit and the INT2 interrupt request enable bit (INT2IE) are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

The interrupt flag, however, cannot be set by a rising edge occurring when INT2 data that is established when HOLD mode is entered is in the high state, or by a falling edge occurring when INT2 data that is established when HOLD mode is entered is in the low state. Consequently, to release HOLD mode with INT2, it is recommended that INT2 be used in both-edge interrupt mode.

This bit must be cleared with an instruction as it is not cleared automatically.

INT2IE (bit 0): INT2 interrupt request enable

When this bit and INT2IF are set to 1, a HOLD mode release signal and an interrupt request to vector address 0013H are generated.

3.1.3.8 Input signal select register (ISL)

1) This register is an 8-bit register that controls the timer 0 input, noise filter time constant, buzzer output, and base timer clock.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5F	0000 0000	R/W	ISL	ST0HCP	ST0LCP	BTIMC1	BTIMC0	BUZON	NFSEL	NFON	ST0IN

ST0HCP (bit 7): Timer 0H capture signal input port select

This bit selects the timer 0H capture signal input port.

When this bit is set to 0, a timer 0H capture signal is generated when the conditions for detecting an INT3 interrupt are established.

When this bit is set to 1, no timer 0H capture signal is generated.

ST0LCP (bit 6): Timer 0L capture signal input port select

This bit selects the timer 0L capture signal input port.

When this bit is set to 0, a timer 0L capture signal is generated when the conditions for detecting an INT2 interrupt are established.

When this bit is set to 1, no timer 0L capture signal is generated.

BTIMC1 (bit 5): Base timer clock select

BTIMC1	Base Timer Input Clock
0	Cycle clock
1	Timer/counter 0 prescaler output

BTIMC0 (bit 4): This bit must always be set to 0.

BUZON (bit 3): Buzzer output select

This bit enables the buzzer output (fBST/16).

When this bit is set to 1, a signal obtained by frequency-dividing the base timer clock by 16 is sent to port P30 as a buzzer output.

When this bit is set to 0, the buzzer output is fixed at the low level.

NFSEL (bit 2): Noise filter time constant select

NFON (bit 1): Noise filter time constant select

NFSEL	NFON	Noise Filter Time Constant
0	0	1 Tcyc
0	1	128 Tcyc
1	0	1 Tcyc
1	1	32 Tcyc

ST0IN (bit 0): Timer 0 count clock input port select

This bit selects the timer 0 count clock signal input port.

When this bit is set to 1, a timer 0 count clock is generated when the conditions for detecting an INT3 interrupt are established.

When this bit is set to 0, a timer 0 count clock is generated when the conditions for detecting an INT2 interrupt are established.

Port 0

Notes:

1) *When the timer 0L capture signal input or timer 0H capture signal input is specified for INT4 together with for INT2 or INT3, the signal from INT2 or INT3 is ignored.*
2) *When the timer 1 count clock input is specified for INT4, the timer 1L serves as an event counter. If the timer 1 count clock input is not specified for INT4, the timer 1L counts at 2 Tcyc intervals.*

3.1.4 Options

Two user options are available for P00 to P07.

1) CMOS output (with a programmable pull-up resistor)
2) N-channel open drain output (with a programmable pull-up resistor)

3.1.5 HALT and HOLD Mode Operation

When in HALT or HOLD mode, port 0 retains the state that is established when HALT or HOLD mode is entered.

3.2 Port 3

3.2.1 Overview

Port 3 is a 1-bit I/O port equipped with programmable pull-up resistors. It is made up of a data latch, a data direction register, and a control circuit. The I/O direction is set by the data direction register in 1-bit units.

As a user option, either CMOS output with a programmable pull-up resistor or N-channel open drain output with a programmable pull-up resistor can be selected as the output type in 1-bit units.

3.2.2 Functions

1) I/O port (1 bit: P30)
   - The port output data is controlled by the port 3 data latch (P3: FE4C) and the I/O direction is controlled by the port 3 data direction register (P3DDR: FE4D).
   - Each port bit is provided with a programmable pull-up resistor.

2) Multiplexed pin function
   - P30 is multiplexed to provide the buzzer output and PPG comparator 1 output functions. Details are explained in the individual sections.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE4C	HHHH HHH0	R/W	P3	-	-	-	-	-	-	-	P30
FE4D	HHHH HHH0	R/W	P3DDR	-	-	-	-	-	-	-	P30DDR

3.2.3 Related Registers

3.2.3.1 Port 3 data latch (P3)

1) This latch is a 1-bit register used to control the port 3 output data and its pull-up register.
2) When this register is read with an instruction, data at pin P30 is read in. If P3 (FE4C) is manipulated using the NOT1, CLR1, SET1, DBZ, DBNZ, INC, or DEC instruction, the contents of the register are referenced instead of the data at the port pin.
3) Port 3 data can always be read regardless of the I/O state of the port.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE4C	HHHH HHH0	R/W	P3	-	-	-	-	-	-	-	P30

3.2.3.2 Port 3 data direction register (P3DDR)

1) This register is a 1-bit register that controls the I/O direction of port 3 data in 1-bit units. Port P3n is placed into output mode when bit P3nDDR is set to 1 and into input mode when bit P3nDDR is set to 0.
2) Port P3 becomes an input with a pull-up resistor if bit P3nDDR is set to 0 and the bit P3n of the port 3 data latch is set to 1

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE4D	HHHH HHH0	R/W	P3DDR	-	-	-	-	-	-	-	P30DDR

Register Data		Port P3n State		Internal Pull-up Resistor
P3n	P3nDDR	Input	Output	
0	0	Enabled	Open	OFF
1	0	Enabled	Internal pull-up resistor	ON
0	1	Enabled	Low	OFF
1	1	Enabled	High/open (CMOS/N-channel open drain)	OFF

3.2.4 Options

Two user options are available.

1) CMOS output (with a programmable pull-up resistor)
2) N-channel open drain output (with a programmable pull-up resistor)

3.2.5 HALT and HOLD Mode Operation

When in HALT or HOLD mode, port 3 retains the state that is established when HALT or HOLD mode is entered.

3.3 Timer/Counter 0 (T0)

3.3.1 Overview

The timer/counter 0 (T0) incorporated in this series of microcontrollers is a 16-bit timer/counter that provides the following four functions:

1) Mode 0: 8-bit programmable timer with a programmable prescaler (with an 8-bit capture register) × 2 channels
2) Mode 1: 8-bit programmable timer with a programmable prescaler (with an 8-bit capture register) + 8-bit programmable counter (with an 8-bit capture register)
3) Mode 2: 16-bit programmable timer with a programmable prescaler (with a 16-bit capture register)
4) Mode 3: 16-bit programmable counter (with a 16-bit capture register)

3.3.2 Functions

1) Mode 0: 8-bit programmable timer with a programmable prescaler (with an 8-bit capture register) × 2 channels
   - Two independent 8-bit programmable timers (T0L and T0H) run on the clock (with a period of 1 to 256 Tcyc) from an 8-bit programmable prescaler.
   - The contents of T0L are captured into the capture register T0CAL on detection signals from the INT2/INT4 pin.
   - The contents of T0H are captured into the capture register T0CAH on detection signals from the INT3/INT4 pin.

     T0L period = (T0LR + 1) × (T0PRR + 1) × Tcyc

     T0H period = (T0HR + 1) × (T0PRR + 1) × Tcyc

     Tcyc = Period of cycle clock

2) Mode 1: 8-bit programmable timer with a programmable prescaler (with an 8-bit capture register) + 8-bit programmable counter (with an 8-bit capture register)
   - T0L serves as an 8-bit programmable counter that counts the number of detection signals from the INT2/INT3 pin.
   - T0H serves as an 8-bit programmable timer that runs on the clock (with a period of 1 to 256 Tcyc) from an 8-bit programmable prescaler.
   - The contents of T0L are captured into the capture register T0CAL on detection signals from the INT2/INT4 pin.
   - The contents of T0H are captured into the capture register T0CAH on detection signals from the INT3/INT4 pin.

     T0L period = (T0LR + 1)

     T0H period = (T0HR + 1) × (T0PRR + 1) × Tcyc

3) Mode 2: 16-bit programmable timer with a programmable prescaler (with a 16-bit capture register)
   - Timer/counter 0 serves as a 16-bit programmable timer that runs on the clock (with a period of 1 to 256 Tcyc) from an 8-bit programmable prescaler.
   - The contents of T0L and T0H are captured into the capture registers T0CAL and T0CAH at the same time on detection signals from the INT3/INT4 pin.

     T0 period = ([T0HR, T0LR] + 1) × (T0PRR +1) × Tcyc

     16 bits

4) Mode 3: 16-bit programmable counter (with a 16-bit capture register)
   - Timer/counter 0 serves as a 16-bit programmable counter that counts the number of detection signals from INT2 and INT3.
   - The contents of T0L and T0H are captured into the capture registers T0CAL and T0CAH at the same time on detection signals from the INT3/INT4 pin.

     T0 period = [T0HR,T0LR] + 1

     16 bits

5) Interrupt generation

   T0L or T0H interrupt requests are generated at the counter interval for T0L or T0H if the interrupt request enable bit is set.

6) It is necessary to manipulate the following special function registers to control timer/counter 0 (T0).
   - T0CNT, T0PRR, T0L, T0H, T0LR, T0HR,
   - ISL, I23CR
   - P0, P0DDR, I45CR, I45SL

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE10	0000 0000	R/W	T0CNT	T0HRUN	T0LRUN	T0LONG	T0LEXT	T0HCMP	T0HIE	T0LCMP	T0LIE
FE11	0000 0000	R/W	T0PRR	T0PRR7	T0PRR6	T0PRR5	T0PRR4	T0PRR3	T0PRR2	T0PRR1	T0PRR0
FE12	0000 0000	R	T0L	T0L7	T0L6	T0L5	T0L4	T0L3	T0L2	T0L1	T0L0
FE13	0000 0000	R	T0H	T0H7	T0H6	T0H5	T0H4	T0H3	T0H2	T0H1	T0H0
FE14	0000 0000	R/W	T0LR	T0LR7	T0LR6	T0LR5	T0LR4	T0LR3	T0LR2	T0LR1	T0LR0
FE15	0000 0000	R/W	T0HR	T0HR7	T0HR6	T0HR5	T0HR4	T0HR3	T0HR2	T0HR1	T0HR0
FE16	XXXX XXXX	R	T0CAL	T0CAL7	T0CAL6	T0CAL5	T0CAL4	T0CAL3	T0CAL2	T0CAL1	T0CAL0
FE17	XXXX XXXX	R	T0CAH	T0CAH7	T0CAH6	T0CAH5	T0CAH4	T0CAH3	T0CAH2	T0CAH1	T0CAH0

3.3.3 Circuit Configuration

3.3.3.1 Timer/counter 0 control register (T0CNT) (8-bit register)

1) This register controls the operation and interrupts of T0L and T0H.

3.3.3.2 Programmable prescaler match register (T0PRR) (8-bit register)

1) This register stores the match data for the programmable prescaler.

3.3.3.3 Programmable prescaler (8-bit counter)

1) Start/stop: This register runs in modes other than HOLD mode.
2) Count clock: Cycle clock (period = 1 Tcyc).
3) Match signal: A match signal is generated when the count value matches the value of the register T0PRR (period: 1 to 256 Tcyc)
4) Reset: The counter starts counting from 0 when a match signal occurs or when data is written into T0PRR.

3.3.3.4 Timer/counter 0 low byte (T0L) (8-bit counter)

1) Start/stop: Stop/start is controlled by the 0/1 value of T0LRUN (timer/counter 0 control register, bit 6).
2) Count clock: Either a prescaler match signal or detection signal of INT2 or INT3 must be selected through the 0/1 value of T0LEXT (timer/counter 0 control register, bit 4).
3) Match signal: A match signal is generated when the count value matches the value of the match buffer register (16 bits of data must match in the 16-bit mode).
4) Reset: When the counter stops operation or a match signal is generated.

3.3.3.5 Timer/counter 0 high byte (T0H) (8-bit counter)

1) Start/stop: Stop/start is controlled by the 0/1 value of T0HRUN (timer/counter 0 control register, bit 7).
2) Count clock: Either prescaler match signal or a T0L match signal must be selected through the 0/1 value of T0LONG (timer/counter 0 control register, bit 5).
3) Match signal: A match signal is generated when the count value matches the value of the match buffer register (16 bits of data must match in the 16-bit mode).
4) Reset: When the counter stops operation or a match signal is generated.

3.3.3.6 Timer/counter 0 match data register low byte (T0LR) (8-bit register with a match buffer register)

1) This register is used to store the match data for T0L. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of the low-order byte of timer/counter 0 (16 bits of data must match in the 16-bit mode).
2) The match buffer register is updated as follows:
   - When it is inactive (T0LRUN=0), the match buffer register matches T0LR.
   - When it is active (T0LRUN=1), the match buffer register is loaded with the contents of T0LR when a match signal is generated.

3.3.3.7 Timer/counter 0 match data register high byte (T0HR) (8-bit register with a match buffer register)

1) This register is used to store the match data for T0H. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of the high-order byte of timer/counter 0 (16 bits of data must match in the 16-bit mode).
2) The match buffer register is updated as follows:
   - When it is inactive (T0HRUN=0), the match buffer register matches T0HR.
   - When it is active (T0HRUN=1), the match buffer register is loaded with the contents of T0HR when a match signal is generated.

3.3.3.8 Timer/counter 0 capture register low byte (T0CAL) (8-bit register)

1) Capture clock: Detection signals from the INT2/INT4 pin when T0LONG (timer/counter 0 control register, bit 5) is set to 0.

   Detection signals from the INT3/INT4 pin when T0LONG (timer/counter 0 control register, bit 5) is set to 1.

2) Capture data: Contents of timer/counter 0 low byte (T0L)

3.3.3.9 Timer/counter 0 capture register high byte (T0CAH) (8-bit register)

1) Capture clock: Detection signals from the INT3/INT4 pin
2) Capture data: Contents of timer/counter 0 high byte (T0H)

Table 3.3.1 Timer 0 (T0H, T0L) Count Clocks

Mode	T0LONG	T0LEXT	T0H Count Clock	T0L Count Clock	[T0H, T0L] Count Clock
0	0	0	T0PRR match signal	T0PRR match signal	–
1	0	1	T0PRR match signal	Detection signal from INT2/INT3	–
2	1	0	–	–	T0PRR match signal
3	1	1	–	–	Detection signal from INT2/INT3

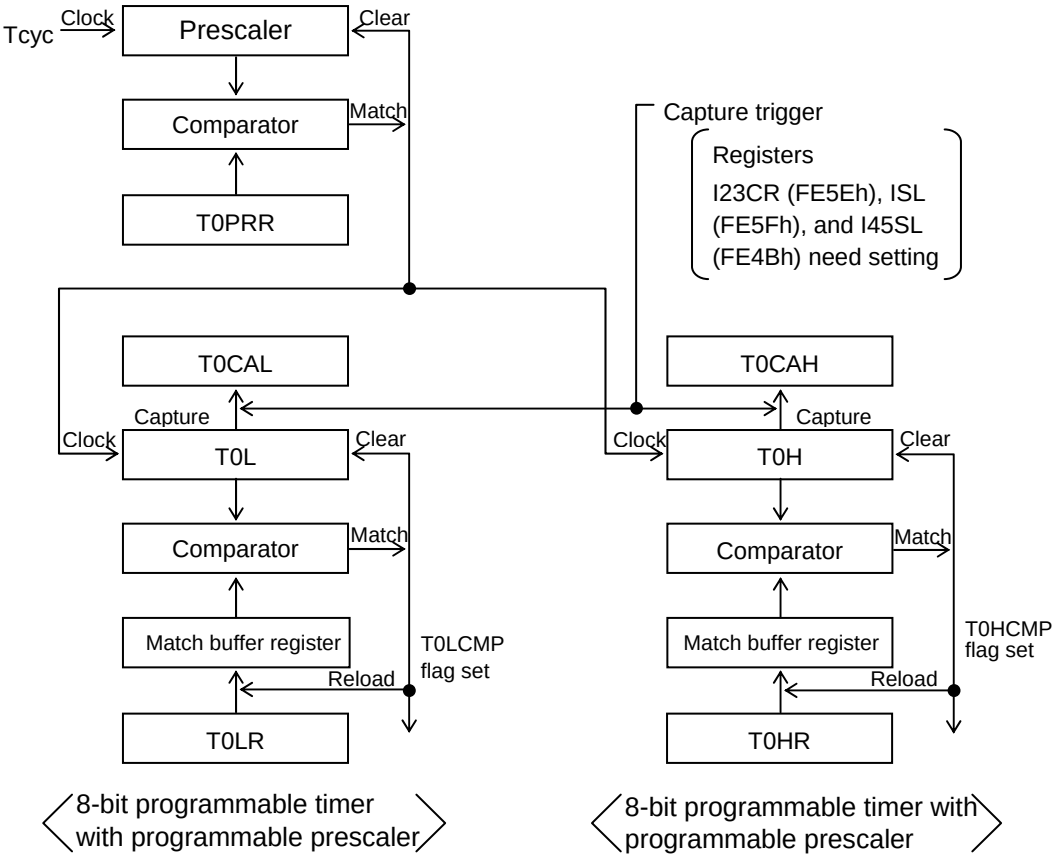


Figure 3.3.1 Mode 0 Block Diagram (T0LONG = 0 , T0LEXT = 0)

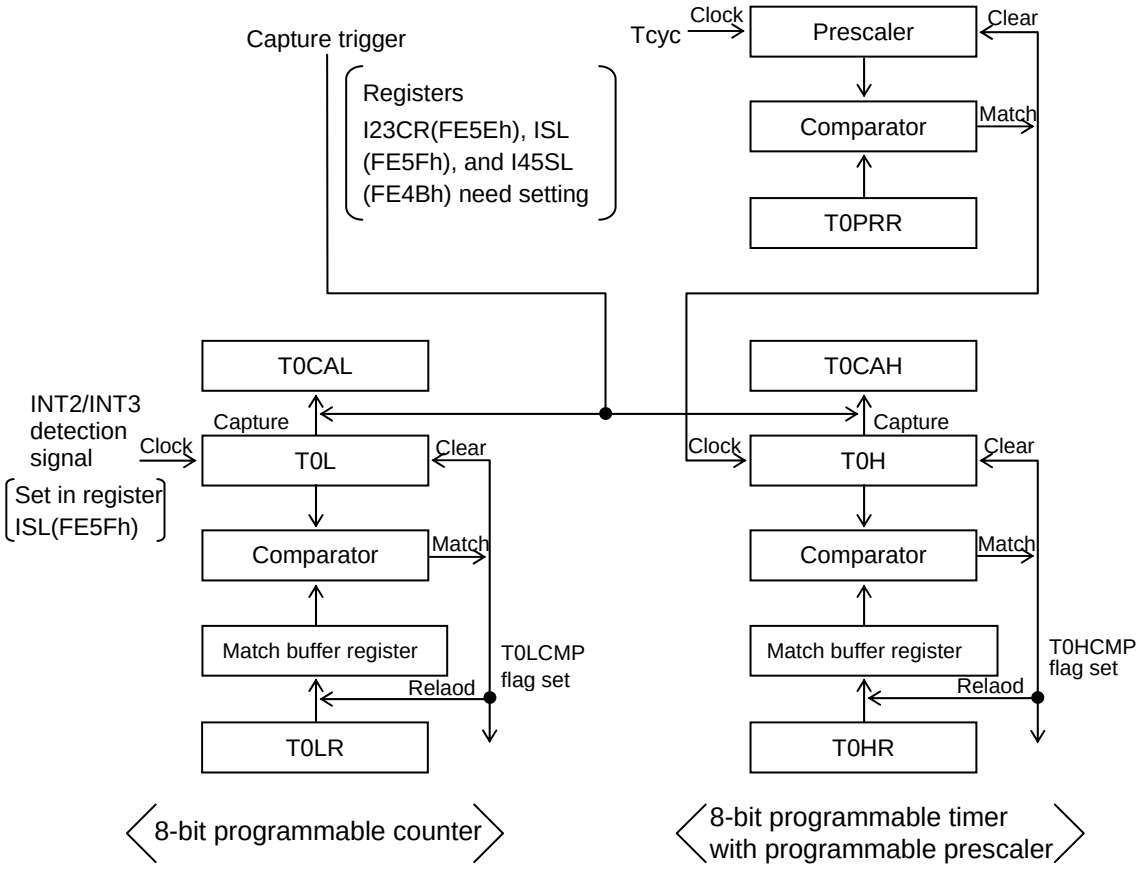


Figure 3.3.2 Mode 1 Block Diagram (T0LONG = 0, T0LEXT = 1)

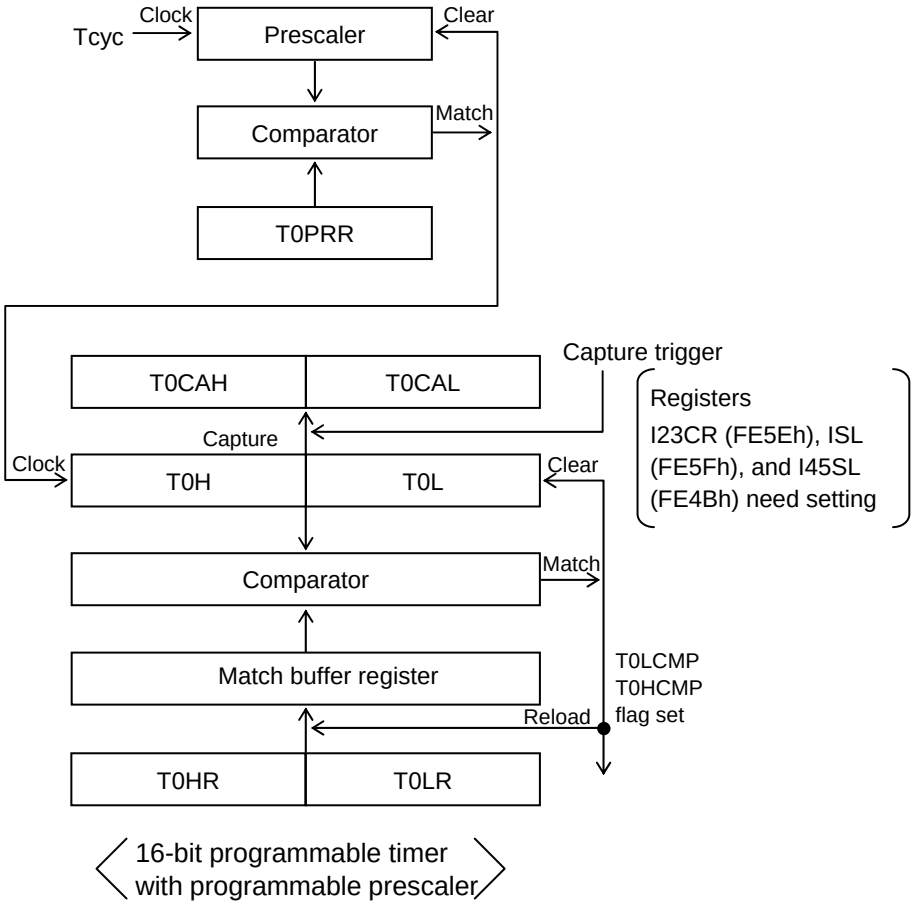


Figure 3.3.3 Mode 2 Block Diagram (T0LONG = 1, T0LEXT = 0)

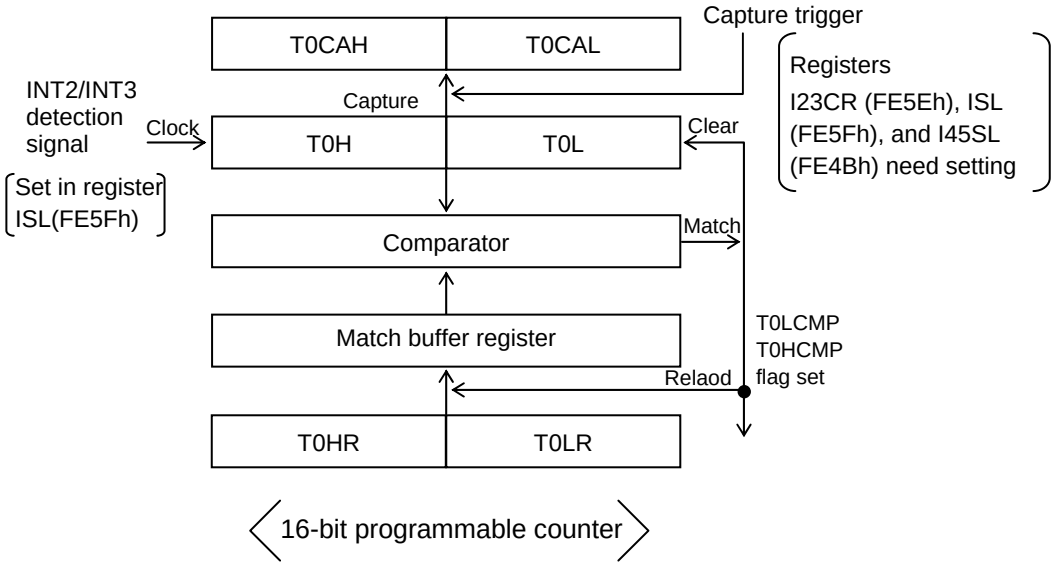


Figure 3.3.4 Mode 3 Block Diagram (T0LONG = 1, T0LEXT = 1)

3.3.4 Related Registers

3.3.4.1 Timer/counter 0 control register (T0CNT)

1) This register is an 8-bit register that controls the operation and interrupts of T0L and T0H.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE10	0000 0000	R/W	T0CNT	T0HRUN	T0LRUN	T0LONG	T0LEXT	T0HCMP	T0HIE	T0LCMP	T0LIE

T0HRUN (bit 7): T0H count control

When this bit is set to 0, timer/counter 0 high byte (T0H) stops on a count value of 0. The match buffer register of T0H has the same value as T0HR.

When this bit is set to 1, timer/counter 0 high byte (T0H) performs the required counting operation. The match buffer register of T0H is loaded with the contents of T0HR when a match signal is generated.

T0LRUN (bit 6): T0L count control

When this bit is set to 0, timer/counter 0 low byte (T0L) stops on a count value of 0. The match buffer register of T0L has the same value as T0LR.

When this bit is set to 1, timer/counter 0 low byte (T0L) performs the required counting operation. The match buffer register of T0L is loaded with the contents of T0LR when a match signal is generated.

T0LONG (bit 5): Timer/counter 0 bit length select

When this bit is set to 0, timer/counter 0 high- and low-order bytes serve as independent 8-bit timers/ counters.

When this bit is set to 1, timer/counter 0 functions as a 16-bit timer/counter. A match signal is generated when the count value of the 16-bit counter comprising T0H and T0L matches the contents of the match buffer registers of T0H and T0L.

T0LEXT (bit 4): T0L input clock select

When this bit is set to 0, the count clock for T0L is the match signal for the prescaler.

When this bit is set to 1, the count clock for T0L is the detection signal of INT2 or INT3.

T0HCMP (bit 3): T0H match flag

This bit is set when the value of T0H matches the value of the match buffer register for T0H while T0H is running (T0HRUN = 1) and a match signal is generated. Its state does not change if no match signal is generated. Consequently, this flag must be cleared with an instruction.

In the 16-bit mode (T0LONG = 1), a match must occur in all 16 bits of data for a match signal to occur.

T0HIE (bit 2): T0H interrupt request enable control

When this bit and T0HCMP are set to 1, an interrupt request to vector address 0023H is generated.

T0LCMP (bit 1): T0L match flag

This bit is set when the value of T0L matches the value of the match buffer register for T0L while T0L is running (T0LRUN = 1) and a match signal is generated. Its state does not change if no match signal is generated. Consequently, this flag must be cleared with an instruction.

In the 16-bit mode (T0LONG = 1), a match must occur in all 16 bits of data for a match signal to occur.

T0LIE (bit 0): T0L interrupt request enable control

When this bit and T0LCMP are set to 1, an interrupt request to vector address 0013H is generated.

Notes:

- *T0HCMP and T0LCMP must be cleared to 0 with an instruction.*
- *When the 16-bit mode is to be used, T0LRUN and T0HRUN must be set to the same value to control operation.*
- *T0LCMP and T0HCMP are set at the same time in the 16-bit mode.*

3.3.4.2 Timer 0 programmable prescaler match register (T0PRR)

1) This register is an 8-bit register that is used to define the clock period (Tpr) of timer/counter 0.
2) The count value of the prescaler starts at 0 when T0PRR is loaded with data.
3) Tpr = (T0PRR + 1) × Tcyc Tcyc = Period of cycle clock

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE11	0000 0000	R/W	T0PRR	T0PRR7	T0PRR6	T0PRR5	T0PRR4	T0PRR3	T0PRR2	T0PRR1	T0PRR0

3.3.4.3 Timer/counter 0 low byte (T0L)

1) This is a read-only 8-bit timer/counter. It counts the number of match signals from the prescaler or detection signal of INT2 or INT3.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE12	0000 0000	R	T0L	T0L7	T0L6	T0L5	T0L4	T0L3	T0L2	T0L1	T0L0

3.3.4.4 Timer/counter 0 high byte (T0H)

1) This is a read-only 8-bit timer/counter. It counts the number of match signals from the prescaler or overflows occurring in T0L.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE13	0000 0000	R	T0H	T0H7	T0H6	T0H5	T0H4	T0H3	T0H2	T0H1	T0H0

3.3.4.5 Timer/counter 0 match data register low byte (T0LR)

1) This register is used to store the match data for T0L. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of the low-order byte of timer/counter 0 (16 bits of data must match in the 16-bit mode).
2) The match buffer register is updated as follows:
   - When it is inactive (T0LRUN=0), the match buffer register matches T0LR.
   - When it is active (T0LRUN=1), the match buffer register is loaded with the contents of T0LR when a match signal is generated.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE14	0000 0000	R/W	T0LR	T0LR7	T0LR6	T0LR5	T0LR4	T0LR3	T0LR2	T0LR1	T0LR0

3.3.4.6 Timer/counter 0 match data register high byte (T0HR)

1) This register is used to store the match data for T0H. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of the high-order byte of timer/counter 0 (16 bits of data must match in the 16-bit mode).

2) The match buffer register is updated as follows:

   • When it is inactive (T0HRUN=0), the match buffer register matches T0HR.

   • When it is active (T0HRUN=1), the match buffer register is loaded with the contents of T0HR when a match signal is generated.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE15	0000 0000	R/W	T0HR	T0HR7	T0HR6	T0HR5	T0HR4	T0HR3	T0HR2	T0HR1	T0HR0

3.3.4.7 Timer/counter 0 capture register low byte (T0CAL)

1) This register is a read-only 8-bit register used to capture the contents of timer/counter 0 low byte (T0L) on an external input detection signal.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE16	XXXX XXXX	R	T0CAL	T0CAL7	T0CAL6	T0CAL5	T0CAL4	T0CAL3	T0CAL2	T0CAL1	T0CAL0

3.3.4.8 Timer/counter 0 capture register high byte (T0CAH)

1) This register is a read-only 8-bit register used to capture the contents of timer/counter 0 high byte (T0H) on an external input detection signal.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE17	XXXX XXXX	R	T0CAH	T0CAH7	T0CAH6	T0CAH5	T0CAH4	T0CAH3	T0CAH2	T0CAH1	T0CAH0

3.4 Timer/Counter 1 (T1)

3.4.1 Overview

The timer/counter 1 (T1) incorporated in this series of microcontrollers is a 16-bit timer/counter with a prescaler that provides the following three functions:

1) Mode 0: 8-bit programmable timer with an 8-bit prescaler + 8-bit programmable timer/counter
2) Mode 2: 16-bit programmable timer/counter with an 8-bit prescaler
3) Mode 3: 16-bit programmable timer with an 8-bit prescaler

3.4.2 Functions

1) Mode 0: 8-bit programmable timer with an 8-bit prescaler + 8-bit programmable timer/counter
   - Two independent 8-bit programmable timers (T1L and T1H) run on a clock that is obtained by dividing the cycle clock by 2.
   - T1L functions as an 8-bit programmable timer/counter that counts the number of signals obtained by dividing the cycle clock by 2 or external events while T1H functions as an 8-bit programmable timer that counts the number of signals obtained by dividing the cycle clock by 2.

     T1L period = (T1LR + 1) × (T1LPRC count) × 2Tcyc or
     (T1LR + 1) × (T1LPRC count) events detected

     T1H period = (T1HR + 1) × (T1HPRC count) × 2Tcyc

2) Mode 2: 16-bit programmable timer/counter with an 8-bit prescaler
   - 16-bit programmable timer/counter functions as a clock that counts the number of signals obtained by dividing the cycle clock by 2 or external events. Since interrupts can occur from the low-order 8-bit timer (T1L) at the interval of T1L period, the low-order 8 bits of this 16-bit programmable timer/counter can be used as the reference timer.

     T1L period = (T1LR + 1) × (T1LPRC count) × 2Tcyc or
     (T1LR + 1) × (T1LPRC count) events detected

     T1 period = (T1HR + 1) × (T1HPRC count) × T1L period or
     (T1HR + 1) × (T1HPRC count) × (T1LR + 1) × (T1LPRC count) events detected

3) Mode 3: 16-bit programmable timer with an 8-bit prescaler
   - A 16-bit programmable timer runs on the cycle clock.

     T1 period = (T1HR + 1) × (T1HPRC count) × 256 × (T1LPRC count) × Tcyc

4) Interrupt generation

   T1L or T1H interrupt request is generated at the counter period of the T1L or T1H if the interrupt request enable bit is set.

5) It is necessary to manipulate the following special function registers to control timer 1 (T1).
   - T1CNT, T1L, T1H, T1LR, T1HR, T1PRR
   - P0, P0DDR, I45CR, I45SL

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE18	0000 0000	R/W	T1CNT	T1HRUN	T1LRUN	T1LONG	T1PWM	T1HCMP	T1HIE	T1LCMP	T1LIE
FE1A	0000 0000	R	T1L	T1L7	T1L6	T1L5	T1L4	T1L3	T1L2	T1L1	T1L0
FE1B	0000 0000	R	T1H	T1H7	T1H6	T1H5	T1H4	T1H3	T1H2	T1H1	T1H0
FE1C	0000 0000	R/W	T1LR	T1LR7	T1LR6	T1LR5	T1LR4	T1LR3	T1LR2	T1LR1	T1LR0
FE1D	0000 0000	R/W	T1HR	T1HR7	T1HR6	T1HR5	T1HR4	T1HR3	T1HR2	T1HR1	T1HR0
FE19	0000 0000	R/W	T1PRR	T1HPRE	T1HPRC2	T1HPRC1	T1HPRC0	T1LPRE	T1PRC2	T1LPRC1	T1LPRC0

3.4.3 Circuit Configuration

3.4.3.1 Timer 1 control register (T1CNT) (8-bit register)

1) This register controls the operation and interrupts of T1L and T1H.

3.4.3.2 Timer 1 prescaler control register (T1PRR) (8-bit counter)

1) This register sets the clocks for T1L and T1H.

3.4.3.3 Timer 1 prescaler low byte (8-bit counter)

1) Start/stop: Stop/start is controlled by the 0/1 value of T1LRUN (timer 1 control register, bit 6).

2) Count clock: Depends on the operating mode.

Mode	T1LONG	T1PWM	T1L Prescaler Count Clock
0	0	0	2 Tcyc/events (Note 1)
2	1	0	2 Tcyc/events (Note 1)
3	1	1	1 Tcyc (Note 2)

Note 1: T1L serves as an event counter when INT4 is specified as the timer 1 count clock input in the external interrupt 4 pin select register (I45SL). It serves as a timer that runs using 2Tcyc as its count clock if INT4 is not specified as the timer 1 count clock input.

Note 2: T1L will not run normally if INT4 is specified as the timer 1 count clock input when T1PWM = 1. When T1PWM = 1, do not specify INT4 as the timer 1 count clock input.

3) Prescaler count: Determined by the T1PRC value.

The count clock for T1L is output at intervals determined by the prescaler count.

T1LPRE	T1LPRC2	T1LPRC1	T1LPRC0	T1L Prescaler Count
0	–	–	–	1
1	0	0	0	2
1	0	0	1	4
1	0	1	0	8
1	0	1	1	16
1	1	0	0	32
1	1	0	1	64
1	1	1	0	128
1	1	1	1	256

4) Reset: When operation stopped or a T1L reset signal is generated.

3.4.3.4 Timer 1 prescaler high byte (8-bit counter)

1) Start/stop: Stop/start is controlled by the 0/1 value of T1HRUN (timer 1 control register, bit 7).

2) Count clock: Depends on the operating mode.

Mode	T1LONG	T1PWM	T1H Prescaler Count Clock
0	0	0	2 Tcyc
2	1	0	T1L match signal
3	1	1	256 × (T1LPRC count) × Tcyc

3) Prescaler count: Determined by the T1PRC value.

The count clock for T1H is output at intervals determined by the prescaler count.

T1HPRE	T1HPRC2	T1HPRC1	T1HPRC0	T1H Prescaler Count
0	–	–	–	1
1	0	0	0	2
1	0	0	1	4
1	0	1	0	8
1	0	1	1	16
1	1	0	0	32
1	1	0	1	64
1	1	1	0	128
1	1	1	1	256

4) Reset: When operation stopped or a T1H reset signal is generated.

3.4.3.5 Timer 1 low byte (T1L) (8-bit counter)

1) Start/stop: Stop/start is controlled by the 0/1 value of T1LRUN (timer 1 control register, bit 6).

2) Count clock: T1L prescaler output clock.

3) Match signal: A match signal is generated when the count value matches the value of the match buffer register.

4) Reset: When operation stopped or a match signal occurs in the mode 0 or 2 condition.

3.4.3.6 Timer 1 high byte (T1H) (8-bit counter)

1) Start/stop: Stop/start is controlled by the 0/1 value of T1HRUN (timer 1 control register, bit 7).

2) Count clock: T1H prescaler output clock

3) Match signal: A match signal is generated when the count value matches the value of the match buffer register.

4) Reset: When operation stopped or a match signal occurs in the mode 0, 2, or 3 condition.

3.4.3.7 Timer 1 match data register low byte (T1LR) (8-bit register with a match buffer register)

1) This register is used to store the match data for T1L. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of timer 1 low byte (T1L).
2) The match buffer register is updated as follows:
   - When it is inactive (T1LRUN=0), the match buffer register matches T1LR.
   - When it is active (T1LRUN=1), the match buffer register is loaded with the contents of T1LR when a match signal is generated.

3.4.3.8 Timer 1 match data register high byte (T1HR) (8-bit register with a match buffer register

1) This register is used to store the match data for T1H. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of timer 1 high byte (T1H).
2) The match buffer register is updated as follows:
   - When it is inactive (T1HRUN=0), the match buffer register matches T1HR.
   - When it is active (T1HRUN=1), the match buffer register is loaded with the contents of T1HR when a match signal is generated.

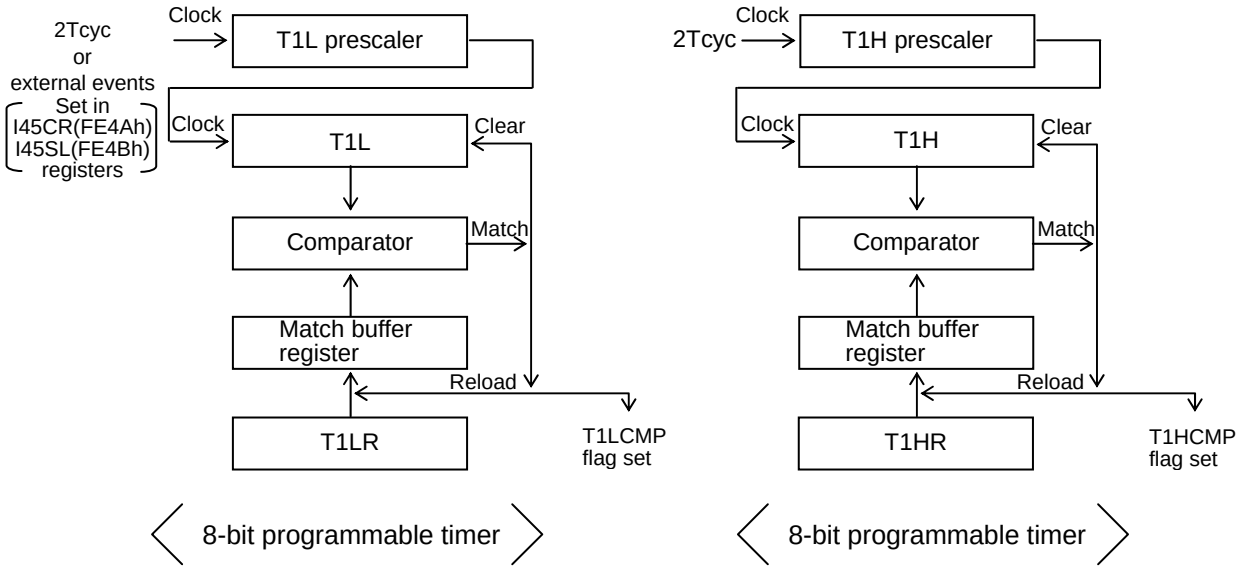


Figure 3.4.1 Mode 0 (T1LONG = 0, T1PWM = 0) Block Diagram

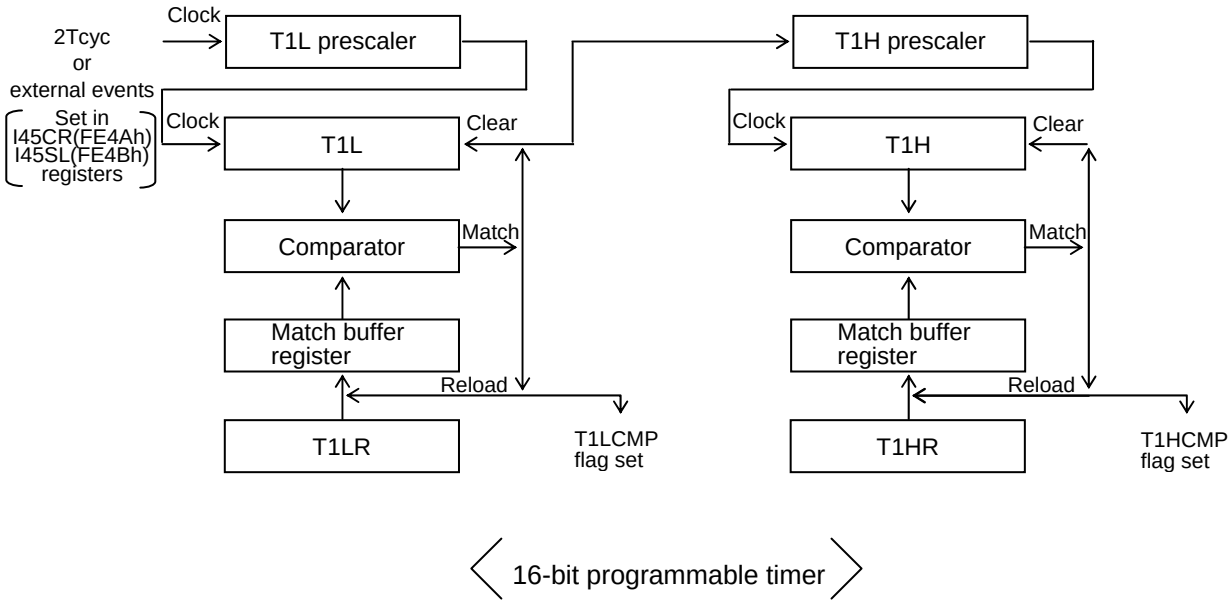


Figure 3.4.2 Mode 2 (T1LONG = 1, T1PWM = 0) Block Diagram

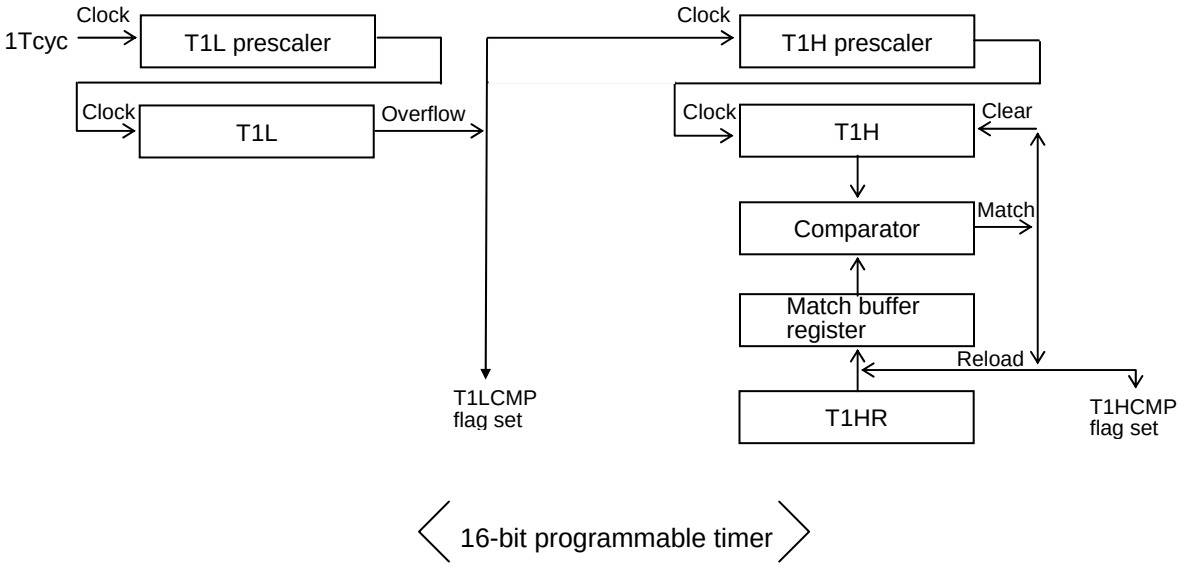


Figure 3.4.3 Mode 3 (T1LONG = 1, T1PWM = 1) Block Diagram

3.4.4 Related Registers

3.4.4.1 Timer 1 control register (T1CNT)

1) This register is an 8-bit register that controls the operation and interrupts of T1L and T1H.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE18	0000 0000	R/W	T1CNT	T1HRUN	T1LRUN	T1LONG	T1PWM	T1HCMP	T1HIE	T1LCMP	T1LIE

T1HRUN (bit 7): T1H count control

When this bit is set to 0, timer 1 high byte (T1H) stops at a count value of 0. The match buffer register of T1H has the same value as T1HR.

When this bit is set to 1, timer 1 high byte (T1H) performs the required counting operation.

T1LRUN (bit 6): T1L count control

When this bit is set to 0, timer 1 low byte (T1L) stops at a count value of 0. The match buffer register of T1L has the same value as T1LR.

When this bit is set to 1, timer 1 low byte (T1L) performs the required counting operation.

T1LONG (bit 5): Timer 1 bit length select

When this bit is set to 0, timer 1 high- and low-order bytes serve as independent 8-bit timers.

When this bit is set to 1, timer 1 serves as a 16-bit timer since the timer 1 high byte (T1H) counts up at the interval of the timer 1 low byte (T1L).

Independent match signals are generated from T1H and T1L when their count value matches the contents of the corresponding match buffer register, regardless of the value of this bit.

T1PWM (bit 4): T1 mode select

This bit and T1LONG (bit 5) determine the mode of T1.

T1HCMP (bit 3): T1H match flag

This flag is set if T1H reaches 0 when T1H is active (T1HRUN = 1).

This flag must be cleared with an instruction.

T1HIE (bit 2): T1H interrupt request enable control

An interrupt request is generated to vector address 002BH when this bit and T1HCMP are set to 1.

T1LCMP (bit 1): T1L match flag

This flag is set if T1L reaches 0 when T1L is active (T1LRUN = 1).

This flag must be cleared with an instruction.

T1LIE (bit 0): T1L interrupt request enable control

An interrupt request is generated to vector address 002BH when this bit and T1LCMP are set to 1.

Note:

- *T1HCMP and T1LCMP must be cleared to 0 with an instruction.*

3.4.4.2 Timer 1 prescaler control register (T1PRR)

1) This register sets up the count values for the timer 1 prescaler.
2) When the register value is changed while the timer is running, the change is reflected in the prescaler operation at the same timing when the match buffer register for the timer (T1L, T1H) is updated.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE19	0000 0000	R/W	T1PRR	T1HPRE	T1HPRC2	T1HPRC1	T1HPRC0	T1LPRE	T1LPRC2	T1LPRC1	T1LPRC0

T1HPRE (bit 7): Timer 1 prescaler high byte control
T1HPRC2 (bit 6): Timer 1 prescaler high byte control
T1HPRC1 (bit 5): Timer 1 prescaler high byte control
T1HPRC0 (bit 4): Timer 1 prescaler high byte control

T1HPRE	T1HPRC2	T1HPRC1	T1HPRC0	T1H Prescaler Count
0	–	–	–	1
1	0	0	0	2
1	0	0	1	4
1	0	1	0	8
1	0	1	1	16
1	1	0	0	32
1	1	0	1	64
1	1	1	0	128
1	1	1	1	256

T1LPRE (bit 3): Timer 1 prescaler low byte control
T1LPRC2 (bit 2): Timer 1 prescaler low byte control
T1LPRC1 (bit 1): Timer 1 prescaler low byte control
T1LPRC0 (bit 0): Timer 1 prescaler low byte control

T1LPRE	T1LPRC2	T1LPRC1	T1LPRC0	T1L Prescaler Count
0	–	–	–	1
1	0	0	0	2
1	0	0	1	4
1	0	1	0	8
1	0	1	1	16
1	1	0	0	32
1	1	0	1	64
1	1	1	0	128
1	1	1	1	256

3.4.4.3 Timer 1 low byte (T1L)

1) This is a read-only 8-bit timer. It counts up on the T1L prescaler output clock.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE1A	0000 0000	R	T1L	T1L7	T1L6	T1L5	T1L4	T1L3	T1L2	T1L1	T1L0

3.4.4.4 Timer 1 high byte (T1H)

1) This is a read-only 8-bit timer. It counts up on the T1H prescaler output clock.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE1B	0000 0000	R	T1H	T1H7	T1H6	T1H5	T1H4	T1H3	T1H2	T1H1	T1H0

3.4.4.5 Timer 1 match data register low byte (T1LR)

1) This register is used to store the match data for T1L. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of timer 1 low byte.
2) The match buffer register is updated as follows:
   - When it is inactive (T1LRUN=0), the match buffer register matches T1LR.
   - When it is active (T1LRUN=1), the match buffer register is loaded with the contents of T1LR when the value of T1L reaches 0.

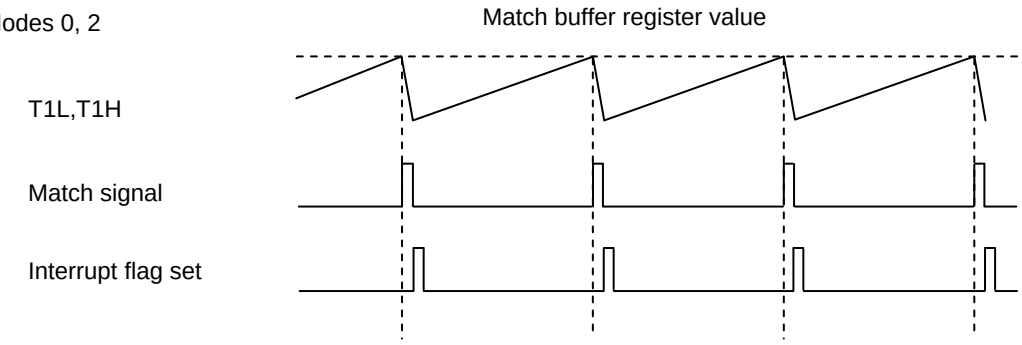
Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE1C	0000 0000	R/W	T1LR	T1LR7	T1LR6	T1LR5	T1LR4	T1LR3	T1LR2	T1LR1	T1LR0

3.4.4.6 Timer 1 match data register high byte (T1HR)

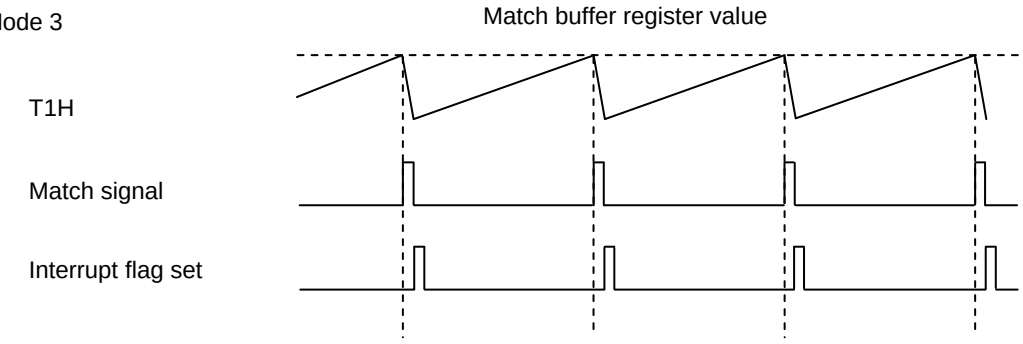
1) This register is used to store the match data for T1H. It has an 8-bit match buffer register. A match signal is generated when the value of this match buffer register matches the value of timer 1 high byte.
2) The match buffer register is updated as follows:
   - When it is inactive (T1HRUN=0), the match buffer register matches T1HR.
   - When it is active (T1HRUN=1), the match buffer register is loaded with the contents of T1HR when the value of T1H reaches 0.

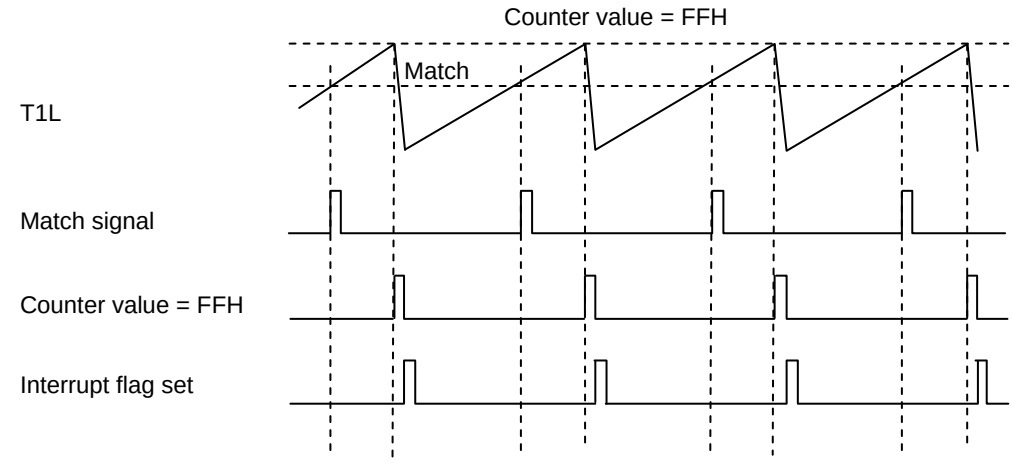
Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE1D	0000 0000	R/W	T1HR	T1HR7	T1HR6	T1HR5	T1HR4	T1HR3	T1HR2	T1HR1	T1HR0

Modes 0, 2



Mode 3





3.5 Timer 6 and Timer 7 (T6, T7)

3.5.1 Overview

Timer 6 (T6) and timer 7 (T7) incorporated in this series of microcontrollers are 8-bit timers with two independently controlled 6-bit prescalers.

3.5.2 Functions

1) Timer 6 (T6)

Timer 6 is an 8-bit timer that runs on either 2Tcyc, 4Tcyc, or 8Tcyc. It can generate toggle waveforms at pin P06 whose frequency is equal to the period of timer 6.

$$\text{T6 period} = (\text{T6R}+1) \times 2^{n}\text{Tcyc} \quad (n = 1, 2, 3)$$

Tcyc = Period of cycle clock

2) Timer 7 (T7)

Timer 7 is an 8-bit timer that runs on either 4Tcyc, 16Tcyc, or 64Tcyc. It can generate toggle waveforms at pin P07 whose frequency is equal to the period of timer 7.

$$\text{T7 period} = (\text{T7R} + 1) \times 4^{n}\text{Tcyc} \quad (n = 1, 2, 3)$$

Tcyc = Period of cycle clock

3) Interrupt generation

An interrupt request to vector address 0043H is generated when the overflow flag is set at the interval of timer 6 or timer 7 period and the corresponding interrupt request enable bit is set.

4) It is necessary to manipulate the following special function registers to control the timer 6 (T6) and timer 7 (T7).

- T67CNT, T6R, T7R, P0FCR

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE78	0000 0000	R/W	T67CNT	T7C1	T7C0	T6C1	T6C0	T7OV	T7IE	T6OV	T6IE
FE7A	0000 0000	R/W	T6R	T6R7	T6R6	T6R5	T6R4	T6R3	T6R2	T6R1	T6R0
FE7B	0000 0000	R/W	T7R	T7R7	T7R6	T7R5	T7R4	T7R3	T7R2	T7R1	T7R0
FE42	00HH 0000	R/W	P0FCR	T7OE	T6OE	-	-	CLKOEN	CKODV2	CKODV1	CKODV0

3.5.3 Circuit Configuration

3.5.3.1 Timer 6/7 control register (T67CNT) (8-bit register)

1) This register controls the operation and interrupts of T6 and T7.

3.5.3.2 Timer 6 counter (T6CTR) (8-bit counter)

1) The timer 6 counter counts the number of clocks from the timer 6 prescaler (T6PR). The value of the timer 6 counter (T6CTR) reaches 0 on the clock following the clock that brought about the value specified in the timer 6 period setting register (T6R), when an interrupt flag (T6OV) is set.
2) When T6C0 and T6C1 (T67CNT: FE78, bits 4 and 5) are set to 0, the timer 6 counter stops at a count value of 0. In the other cases, the timer 6 counter continues operation.
3) When data is written into T6R while timer 6 is running, both the timer 6 prescaler and counter are cleared and start counting again.

3.5.3.3 Timer 6 prescaler (T6PR) (6-bit counter)

1) This prescaler is used to define the clock period for timer 6 determined by T6C0 and T6C1 (T67CNT: FE78, bits 4 and 5).

Table 3.5.1 Timer 6 Count Clocks

T6C1	T6C0	T6 Count Clock
0	0	Timer 6 prescaler and timer/counter are in the reset state.
0	1	2 Tcyc
1	0	4 Tcyc
1	1	8 Tcyc

3.5.3.4 Timer 6 period setting register (T6R) (8-bit register)

1) This register defines the period of timer 6.
2) When data is written into T6R while timer 6 is running, both the timer 6 prescaler and counter are cleared and start counting again.

3.5.3.5 Timer 7 counter (T7CTR) (8-bit counter)

1) The timer 7 counter counts the number of clocks from the timer 7 prescaler (T7PR). The value of timer 7 counter (T7CTR) reaches 0 on the clock following the clock that brought about the value specified in the timer 7 period setting register (T7R), when the interrupt flag (T7OV) is set.
2) When T7C0 and T7C1 (T67CNT: FE78, bits 6 and 7) are set to 0, the timer 7 counter stops at a count value of 0. In the other cases, the timer 7 counter continues operation.
3) When data is written into T7R while timer 7 is running, both the timer 7 prescaler and counter are cleared and start counting again.

3.5.3.6 Timer 7 prescaler (T7PR) (6-bit counter)

1) This prescaler is used to define the clock period for the timer 7 determined by T7C0 and T7C1 (T67CNT: FE78, bits 6 and 7).

Table 3.5.2 Timer 7 Count Clocks

T7C1	T7C0	T7 Count Clock
0	0	Timer 7 prescaler and timer/counter are in the reset state.
0	1	4 Tcyc
1	0	16 Tcyc
1	1	64 Tcyc

3.5.3.7 Timer 7 period setting register (T7R) (8-bit register)

1) This register defines the period of timer 7.
2) When data is written into T7R while timer 7 is running, both the timer 7 prescaler and counter are cleared and start counting again.

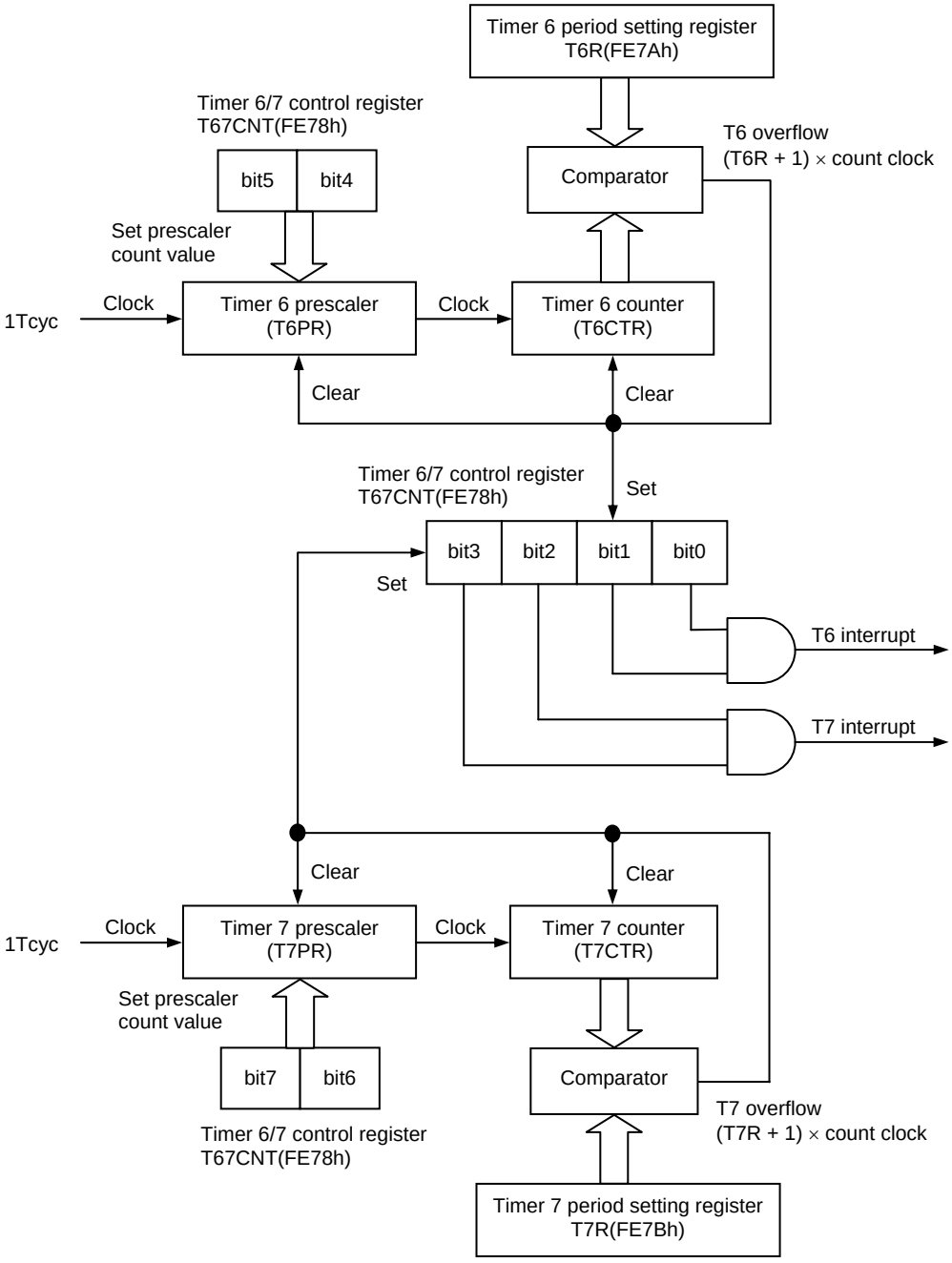


Figure 3.5.1 Timers 6/7 Block Diagram

3.5.4 Related Registers

3.5.4.1 Timer 6/7 control register (T67CNT)

1) This register is an 8-bit register that controls the operation and interrupts of T6 and T7.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE78	0000 0000	R/W	T67CNT	T7C1	T7C0	T6C1	T6C0	T7OV	T7IE	T6OV	T6IE

T7C1 (bit 7): T7 count clock control

T7C0 (bit 6): T7 count clock control

T7C1	T7C0	T7 Count Clock
0	0	Timer 7 prescaler and timer/counter are in the reset state.
0	1	4 Tcyc
1	0	16 Tcyc
1	1	64 Tcyc

T6C1 (bit 5): T6 count clock control

T6C0 (bit 4): T6 count clock control

T6C1	T6C0	T6 Count Clock
0	0	Timer 6 prescaler and timer/counter are in the reset state.
0	1	2 Tcyc
1	0	4 Tcyc
1	1	8 Tcyc

T7OV (bit 3): T7 overflow flag

This flag is set at the interval of timer 7 period when timer 7 is running.

This flag must be cleared with an instruction.

T7IE (bit 2): T7 interrupt request enable control

An interrupt request to vector address 0043H is generated when this bit and T7OV are set to 1.

T6OV (bit 1): T6 overflow flag

This flag is set at the interval of timer 6 period when timer 6 is running.

This flag must be cleared with an instruction.

T6IE (bit 0): T6 interrupt request enable control

An interrupt request to vector address 0043H is generated when this bit and T6OV are set to 1.

3.5.4.2 Timer 6 period setting register (T6R)

1) This register is an 8-bit register for defining the period of timer 6.

   Timer 6 period = (T6R value + 1) × Timer 6 prescaler value (2, 4 or 8 Tcyc)

2) When data is written into T6R while timer 6 is running, both the timer 6 prescaler and counter are cleared and start counting again.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7A	0000 0000	R/W	T6R	T6R7	T6R6	T6R5	T6R4	T6R3	T6R2	T6R1	T6R0

3.5.4.3 Timer 7 period setting register (T7R)

1) This register is an 8-bit register for defining the period of timer 7.

   Timer 7 period = (T7R value + 1) × Timer 7 prescaler value (4, 16 or 64 Tcyc)

2) When data is written into T7R while timer 7 is running, both the timer 7 prescaler and counter are cleared and start counting again.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7B	0000 0000	R/W	T7R	T7R7	T7R6	T7R5	T7R4	T7R3	T7R2	T7R1	T7R0

3.5.4.4 Port 0 function control register (P0FCR)

1) This register is a 6-bit register that controls the multiplexed output of port 0 pins. It controls the toggle outputs of timer 6 and timer 7.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE42	00HH 0000	R/W	P0FCR	T7OE	T6OE	-	-	CLKOEN	CKODV2	CKODV1	CKODV0

T7OE (bit 7):

This flag is used to control the timer 7 toggle output at pin P07.

This flag is disabled when pin P07 is set in the input mode.

When pin P07 is set in the output mode:

A 0 in this bit outputs the value of port data latch.

A 1 in this bit outputs OR of the value of the port data latch and the waveform that toggles at the interval equal to the timer 7 period.

T6OE (bit 6):

This flag is used to control the timer 6 toggle output at pin P06.

Register data			P06 Pin Output in Output Mode (when P06DDR=1)
P06FCNT	T6OE	P06	
0	0	X	Port data latch (P06) values
0	1	0	Timer 6 toggle output
0	1	1	High output
1	0	0	SIO1 clock output
1	0	1	High output
1	1	0	Outputs OR between timer 6 toggle output and SIO1 clock output
1	1	1	High output

(Bits 5, 4): These bits do not exist.

They are always read as 1.

CLKOEN (bit 3):

CKODV2 (bit 2):

CKODV1 (bit 1):

CKODV0 (bit 0):

These 4 bits have nothing to do with the control functions on timers 6 and 7. See the description of port 0 for details on these bits.

3.6 Base Timer (BT)

3.6.1 Overview

The base timer (BT) incorporated in this series of microcontrollers is a 14-bit binary up-counter that provides the following three functions:

1) 14-bit binary up-counter
2) Buzzer output
3) Hold mode release

3.6.2 Functions

1) 14-bit binary up-counter

   A 14-bit binary up-counter can be constructed using an 8-bit binary up-counter and a 6-bit binary up-counter. These counters can be cleared under program control.

2) Buzzer output function

   The buzzer output can be controlled using the input signal select register (ISL). The buzzer output can be transmitted via pin P30.

3) Interrupt generation

   An interrupt request to vector address 001BH is generated if an interrupt request is generated by the base timer when the interrupt request enable bit is set. The base timer can generate two types of interrupt requests: "base timer interrupt 0" and "base timer interrupt 1."

4) HOLD mode operation and HOLD mode release function

   The base timer is enabled for operation in HOLD mode when bit 2 of the power control register (PCON) is set. HOLD mode can be released by an interrupt from the base timer. This function allows the microcontroller to perform low-current intermittent operations.

5) It is necessary to manipulate the following special function registers to control the base timer.
   - BTCR, ISL, P3, P3DDR

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7F	0000 0000	R/W	BTCR	BTFST	BTON	BTC11	BTC10	BTIF1	BTIE1	BTIF0	BTIE0
FE5F	0000 0000	R/W	ISL	ST0HCP	ST0LCP	BTIMC1	BTIMC0	BUZON	NFSEL	NFON	ST0IN

3.6.3 Circuit Configuration

3.6.3.1 8-bit binary up-counter

1) This counter is an up-counter that receives, as its input, the signal selected by the input signal select register (ISL). It generates a buzzer output and base timer interrupt 1 flag set signals.

   The overflow from this counter functions as the clock for the 6-bit binary counter.

3.6.3.2 6-bit binary up-counter

1) This counter is a 6-bit up-counter that receives, as its input, the signal selected by the input signal select register (ISL) or the overflow signal from the 8-bit counter and generates set signals for base timer interrupts 0 and 1. The switching of the input clock is accomplished by the base timer control register (BTCR).

3.6.3.3 Base timer input clock source

1) The clock input to the base timer (fBST) can be selected from the cycle clock and timer 0 prescaler via the input signal select register (ISL).

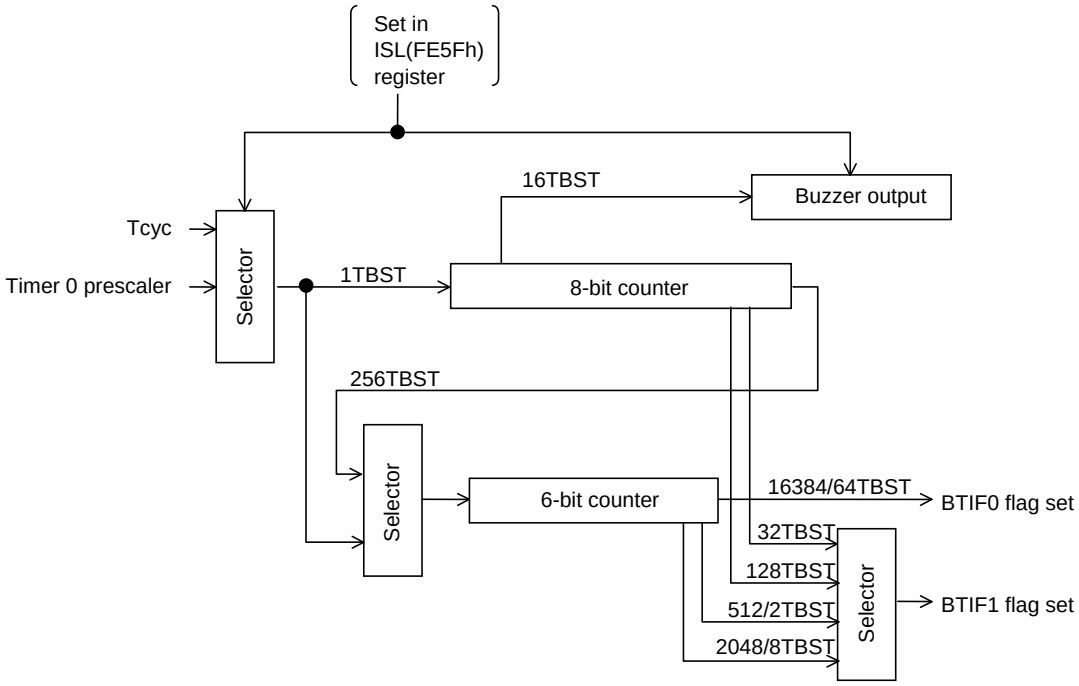


Figure 3.6.1 Base Timer Block Diagram

3.6.4 Related Registers

3.6.4.1 Base timer control register (BTCR)

1) This register is an 8-bit register that controls the operation of the base timer.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7F	0000 0000	R/W	BTCR	BTFST	BTON	BTC11	BTC10	BTIF1	BTIE1	BTIF0	BTIE0

BTFST (bit 7): Base timer interrupt 0 period control

This bit is used to select the interval at which base timer interrupt 0 is to occur.

When this bit is set to 1, the base timer interrupt 0 flag is set when an overflow occurs in the 6-bit counter. The interval at which overflows occur is 64fBST.

When this bit is set to 0, the base timer interrupt 0 flag is set when an overflow occurs in the 14-bit counter. The interval at which overflows occur is 16384fBST.

BTON (bit 6): Base timer operation control

When this bit is set to 0, the base timer stops when the count value reaches 0.

When this bit is set to 1, the base timer continues operation.

BTC11 (bit 5): Base timer interrupt 1 period control

BTC10 (bit 4): Base timer interrupt 1 period control

BTFST	BTC11	BTC10	Base Timer Interrupt 0 Period	Base Timer Interrupt 1 Period
0	0	0	16384fBST	32fBST
1	0	0	64fBST	32fBST
0	0	1	16384fBST	128fBST
1	0	1	64fBST	128fBST
0	1	0	16384fBST	512fBST
0	1	1	16384fBST	2048fBST
1	1	0	64fBST	2fBST
1	1	1	64fBST	8fBST

fBST: The frequency of the input clock that is selected by the input signal select register (ISL).

BTIF1 (bit 3): Base timer interrupt 1 flag

This flag is set at the interval equal to the base timer interrupt 1 period that is defined by BTFST, BTC11, and BTC10.

This flag must be cleared with an instruction.

BTIE1 (bit 2): Base timer interrupt 1 request enable control

When this bit and BTIF1 are to 1, an interrupt request to vector address 001BH is generated.

BTIF0 (bit 1): Base timer interrupt 0 flag

This flag is set at the interval equal to the base timer interrupt 0 period that is defined by BTFST, BTC11, and BTC10.

This flag must be cleared with an instruction.

BTIE0 (bit 0): Base timer interrupt 0 request enable control

When this bit and BTIF0 are to 1, an interrupt request to vector address 001BH is generated.

Notes:

- *Note that BTIF1 is likely to be set to 1 when BTC11 and BTC10 are rewritten.*
- *If HOLD mode is entered while running the base timer when the cycle clock is selected as the base timer clock source, the base timer is subject to the influence of unstable oscillations caused by the main clock when it is started following the release of HOLD mode, resulting in an erroneous count from the base timer. When entering HOLD, therefore, it is recommended that the base timer be stopped.*

3.6.4.2 Input signal select register (ISL)

1) This register is an 8-bit register that controls the timer 0 input, noise filter time constant, buzzer output, and base timer clock.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5F	0000 0000	R/W	ISL	ST0HCP	ST0LCP	BTIMC1	BTIMC0	BUZON	NFSEL	NFON	ST0IN

ST0HCP (bit 7): Timer 0H capture signal input port select

ST0LCP (bit 6): Timer 0L capture signal input port select

These two bits have nothing to do with the control function of the base timer.

BTIMC1 (bit 5): Base timer clock select

BTIMC0 (bit 4): Base timer clock select

BTIMC1	BTIMC0	Base Timer Input Clock
0	0	Prohibited
0	1	Cycle clock
1	0	Prohibited
1	1	Timer/counter 0 prescaler output

BUZON (bit 3): Buzzer output enable

This bit enables the buzzer output ($\frac{fBST}{16}$).

When this bit is set to 1, a signal that is obtained by dividing the base timer clock by 16 is sent to port P30 as the buzzer output.

When this bit is set to 0, the buzzer output is fixed at a low level.

NFSEL (bit 2): Noise filter time constant select

NFON (bit 1): Noise filter time constant select

ST0IN (bit 0): Timer 0 count clock input port select

These three bits have nothing to do with the control function of the base timer.

3.7 Serial Interface 1 (SIO1)

3.7.1 Overview

The serial interface 1 (SIO1) incorporated in this series of microcontrollers provides the following three functions:

1) Mode 0: Synchronous 8-bit serial I/O (2-wire system, transfer clock of 2 to 512 Tcyc)
2) Mode 2: Bus-master (start bit, 8 data bits, transfer clock of 2 to 512 Tcyc)
3) Mode 3: Bus-slave (start detection, 8 data bits, stop detection)

3.7.2 Functions

1) Mode 0: Synchronous 8-bit serial I/O
   - Performs 2-wire synchronous serial communication. The clock may be an internal or external clock.
   - The clock rate of the internal clock is programmable within the range of 2 to 512 Tcyc.

2) Mode 2: Bus-master
   - SIO1 is used as a bus master controller.
   - The start conditions are automatically generated but the stop conditions must be generated by manipulating ports.
   - Clock synchronization is used. Since it is possible to verify the transfer-time bus data at the end of transfer, this mode can be combined with mode 3 to provide support for multi-master configurations.
   - The period of the output clock is programmable within the range of 2 to 512 Tcyc.

3) Mode 3: Bus-slave
   - SIO1 is used as a slave device of the bus.
   - Start/stop condition detection processing is performed but the detection of an address match condition and the generation of an acknowledge require program intervention.
   - SIO1 can generate an interrupt after automatically placing the clock line at the low level on the falling edge of the eighth clock for recognition by a program.

4) Interrupt generation

   An interrupt request is generated at the end of communication if the interrupt request enable bit is set.

5) It is necessary to manipulate the following special function registers to control serial interface 1 (SIO1).
   - SCON1, SBUF1, SBR1
   - P0, P0DDR, P1FCNT

Address	Initial Value	R/W	Name	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE34	0000 0000	R/W	SCON1	-	SI1M1	SI1M0	SI1RUN	SI1REC	SI1DIR	SI1OVR	SI1END	SI1IE
FE35	00000 0000	R/W	SBUF1	SBUF18	SBUF17	SBUF16	SBUF15	SBUF14	SBUF13	SBUF12	SBUF11	SBUF10
FE36	0000 0000	R/W	SBR1	-	SBRG17	SBRG16	SBRG15	SBRG14	SBRG13	SBRG12	SBRG11	SBRG10

3.7.3 Circuit Configuration

3.7.3.1 SIO1 control register (SCON1) (8-bit register)

1) This register controls the operation and interrupts of SIO1.

3.7.3.2 SIO1 shift register (SIOSF1) (8-bit shift register)

1) This register is a shift register used to transfer and receive SIO1 data.
2) This register cannot be accessed with an instruction. It is accessed via SBUF1.

3.7.3.3 SIO1 data register (SBUF1) (9-bit register)

1) The low-order 8 bits of SBUF1 are transferred to SIOSF1 at the beginning of data transfer.
2) At the end of data transfer, the contents of SIOSF1 are placed in the low-order 8 bits of SBUF1. In modes 1, 2, and 3, since the 9th input data is placed in bit 8 of SBUF1, it is possible to check for a stop bit.

3.7.3.4 SIO1 baudrate generator register (SBR1) (8-bit reload counter)

1) This is a reload counter for generating internal clocks.
2) The generator can generate clocks of 2 to 512 Tcyc in modes 0 and 2, and clocks of 8 to 2048 Tcyc in mode 1.

Table 3.7.1 SIO1 Operations and Operating Modes

		Synchronous (Mode 0)		Bus Master (Mode 2)		Bus Slave (Mode 3)	
		Transfer SI1REC=0	Receive SI1REC=1	Transfer SI1REC=0	Receive SI1REC=1	Transfer SI1REC=0	Receive SI1REC=1
Start bit		None	None	See 1) and 2) below	Not required	Not required	See 2) below
Data output		8 (Shift data)	8 (All 1's)	8 (Shift data)	8 (All 1's)	8 (Shift data)	8 (All 1's)
Data input		8 (Input pin)	←	8 (Input pin)	←	8 (Input pin)	←
Stop bit		None	←	Input (H/L)	Output (SBUF1 bit8)	Input (H/L)	Output (L)
Clock		8	←	9	←	Low output on falling edge of 8th clock	←
Operation start		SI1RUN ↑	←	1) No start bit on falling edge of SI1END when SI1RUN=1 2) With start bit on rising edge of SI1RUN when SI1END=0	1) on left side	1) on right side	1) Clock released on falling edge of SI1END when SI1RUN=1 2) Start bit detected when SI1RUN=0 and SI1END=0
Period		2 to 512 Tcyc	←	2 to 512Tcyc	←	2 to 512Tcyc	←
SI1RUN (bit 5)	Set	Instruction	←	Instruction	Already set	Already set	Start bit detected
	Clear	End of processing	←	1) Stop condition detected 2) When arbitration lost (Note 1)	←	1) Stop condition detected 2) Ack=1 detected	←
SI1END (bit 1)	Set	End of processing	←	1) Rising edge of 9th clock 2) Stop condition detected	←	1) Falling edge of 8th clock 2) Stop condition detected	←
	Clear	Instruction	←	Instruction	←	Instruction	←

Note 1: If internal data output state = "H" and data port state = "L" conditions are detected at the rising edges of the first to 8th clocks, the microcontroller recognizes a bus contention loss and clears SI1RUN (and also stops the generation of the clock immediately).

(Continued on next page)

Table 3.7.1 SIO1 Operations and Operating Modes (cont.)

		Synchronous (Mode 0)		Bus Master (Mode 2)		Bus Slave (Mode 3)	
		Transfer SI1REC=0	Receive SI1REC=1	Transfer SI1REC=0	Receive SI1REC=1	Transfer SI1REC=0	Receive SI1REC=1
SI1OVR (bit 2)	Set	1) Falling edge of clock detected when SI1RUN=0 2) SI1END set conditions met when SI1END=1	←	1) SI1END set conditions met when SI1END=1	←	1) Falling edge of clock detected when SI1RUN=0 2) SI1END set conditions met when SI1END=1 3) Start bit detected	←
	Clear	Instruction	←	Instruction	←	Instruction	←
Shifter data update		SBUF1→ shifter at beginning of operation	←	SBUF1→ shifter at beginning of operation	←	SBUF1→ shifter at beginning of operation	←
Shifter→ SBUF1 (bits 0 to 7)		Rising edge of 8th clock	←	Rising edge of 8th clock	←	Rising edge of 8th clock	←
Automatic update of SBUF1 bit 8		None	←	Input data read in on rising edge of 9th clock	←	Input data read in on rising edge of 9th clock	←

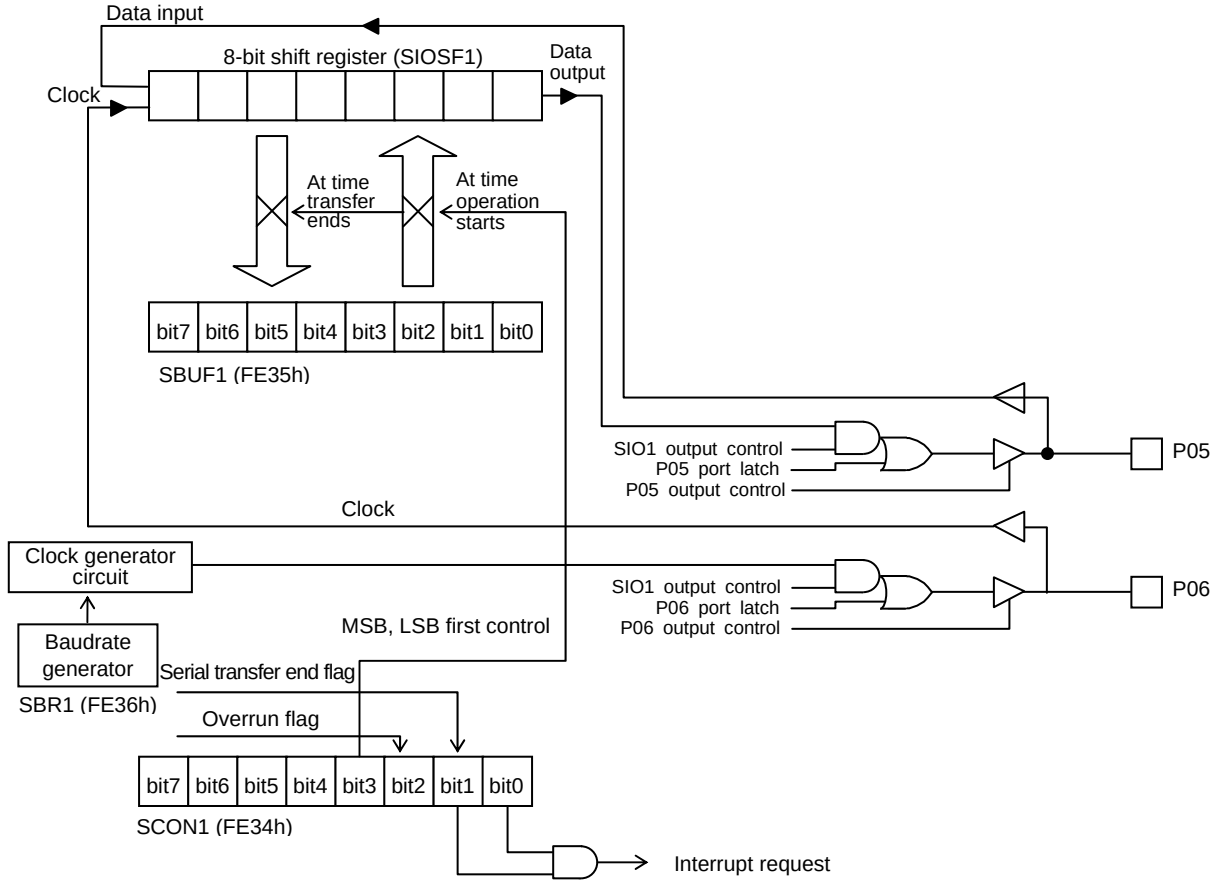


Figure 3.7.1 SIO1 Mode 0: Synchronous 8-bit Serial I/O Block Diagram (SI1M1 = 0, SI1M0 = 0)

3.7.4 SIO1 Communication Examples

3.7.4.1 Synchronous serial communication (mode 0)

1) Setting the clock
   - Set up SBR1 when using an internal clock.
2) Setting the mode
   - Set as follows:
     SI1M0 = 0, SI1M1 = 0, SI1DIR, SI1IE = 1
3) Setting up the ports and SI1REC (bit 4)

	P06
Internal clock	Output
External clock	Input

	P05	SI1REC
Data transmission only	–	0
Data reception only	Input	1
Data transmission/reception (2-wire)	N-channel open drain output	0

4) Setting up output data
   - Write output data into SBUF1 in the data transmission mode (SI1REC = 0).
5) Starting operation
   - Set SI1RUN.
6) Reading data (after an interrupt)
   - Read SBUF1 (SBUF1 has been loaded with serial data from the data I/O port even in transmission mode).
   - Clear SI1END and exit interrupt processing.
   - Return to step 4) when repeating processing.

3.7.4.2 Bus-master mode (mode 2)

1) Setting the clock
   - Set up SBR1.
2) Setting the mode.
   - Set as follows:
     SI1M0 = 0, SI1M1 = 1, SI1DIR, SI1IE = 1, SI1REC = 0
3) Setting up the ports
   - Configure the clock port (P06) and data port (P05) as N-channel open drain output ports by setting the option.
   - Set P05 (P0, bit 5) and P06 (P0, bit 6) to 0.
   - Set P05FCNT (P0FCNT, bit 5) and P06FCNT (P0FCNT, bit 6) to 1.
   - Set P05DDR (P0DDR, bit 5) and P06DDR (P0DDR, bit 6) to 1.

4) Starting communication (sending an address)
   - Load SBUF1 with address data.
   - Set SI1RUN (transfer a start bit + SBUF1 (8 bits) + stop bit (H)).

5) Checking address data (after an interrupt)
   - Read SBUF1. (SBUF1 has been loaded with serial data from the data I/O port even in transmission mode. When SBUF1 is read in, the data on the position of the stop bit is read into bit 1 of the PSW.)
   - Check for an acknowledge by reading bit 1 of the PSW.
   - If a condition for losing the bus contention occurs (see Note 1 in Table 3.7.1), no interrupt will be generated because SI1RUN is cleared. If there is a possibility of a condition for losing the bus contention, for example, when another device is in master mode in the system, perform timeout processing, etc. using a timer module to detect the condition .

6) Sending data
   - Load SBUF1 with output data.
   - Clear SI1END and exit interrupt processing (transfer SBUF1 (8 bits) + stop bit (H)).

7) Checking sent data (after an interrupt)
   - Read SBUF1. (SBUF1 has been loaded with serial data from the data I/O port even in the transmission mode. When SBUF1 is read in, the data about the position of the stop bit is read into bit 1 of the PSW.)
   - Check for an acknowledge by reading bit 1 of the PSW.
   - If a condition for losing the bus contention occurs (see Note 1 in Table 3.7.1), no interrupt will be generated because SI1RUN is cleared. If there is a possibility of a condition for losing the bus contention, for example, when another device is in master mode in the system, perform timeout processing, etc. using a timer module to detect the condition .
   - Return to step 6) when continuing data transmission.
   - Go to step 10) to terminate communication.

8) Receiving data
   - Set SI1REC to 1.
   - Clear SI1END and exit interrupt processing (receive (8 bits) + SBUF1 bit 8 (acknowledge) output).

9) Reading received data (after an interrupt)
   - Read SBUF1.
   - Return to step 8) to continue reception of data.
   - Go to * in step 10) to terminate processing. At this moment, SBUF1 bit 8 data has already been output as acknowledge data and the clock for the master side has been released.

10) Terminating communication
   - Manipulate the clock output port (P06FCNT = 0, P06DDR = 1, P06 = 0) and set the clock output to 0.
   - Manipulate the data output port (P05FCNT = 0, P05DDR = 1, P05 = 0) and set the data output to 0.
   - Restore the clock output port to the original state (P06FCNT = 1, P06DDR = 1, P06 = 0) and release the clock output.
   * • Wait for all slaves to release the clock and the clock to be set to 1.
   - Allow for a data setup time, then manipulate the data output port (P05FCNT = 0, P05DDR = 1, P05 = 1) and set the data output to 1. In this case, the SIO1 overrun flag (SCON1:FE34, bit 2) is set but this will exert no influence on the operation of SIO1.
   - Restore the data output port to the original state (set P05FCNT to 1, then P05DDR to 1 and P05 to 0).
   - Clear SI1END and SI1OVR, then exit interrupt processing.
   - Return to step 4) to repeat processing.

3.7.4.3 Bus-slave mode (mode 3)

1) Setting the clock
   - Set up SBR1 (to set the acknowledge data setup time).
2) Setting the mode
   - Set as follows:

     SI1M0 = 1, SI1M1 = 1, SI1DIR, SI1IE = 1, SI1REC = 0
3) Setting up ports
   - Configure the clock port (P06) and data port (P05) as N-channel open drain output ports by setting the option.
   - Set P05 (P0, bit 5) and P06 (P0, bit 6) to 0.
   - Set P05FCNT (P0FCNT, bit 5) and P06FCNT (P0FCNT, bit 6) to 1.
   - Set P05DDR (P0DDR bit, 5) and P06DDR (P0DDR, bit 6) to 1.
4) Starting communication (waiting for an address)

   *1 • Set SI1REC.

   *2 • SI1RUN is automatically set on detection of a start bit.
   - Perform receive processing (8 bits) and set the clock output to 0 on the falling edge of the 8th clock, which generates an interrupt.
5) Checking address data (after an interrupt)
   - When a start condition is detected, SI1OVR is set. Check SI1RUN = 1 and SI1OVR=1 to determine if the address has been received.

     (SI1OVR is not automatically cleared. Clear it with an instruction.)
   - Read SBUF1 and check the address.
   - If no address match occurs, clear SI1RUN and SI1END and exit interrupt processing, then wait for a stop condition detection at * of step 8).
6) Receiving data

   * • Clear SI1END and exit interrupt processing. (If a receive sequence has been performed, send an acknowledge and release the clock port after the lapse of (SBR1 value + 1/3) × Tcyc.)
   - When a stop condition is detected, SI1RUN is automatically cleared and an interrupt is generated. Then, clear SI1END to exit interrupt processing and return to *2 in step 4).
   - Perform receive processing (8 bits) and set the clock output to 0 on the falling edge of the 8th clock, which generates an interrupt. The clock counter will be cleared if a start condition is detected in the middle of receive processing. In such a case, another 8 clocks are required to generate an interrupt.
   - Read SBUF1 and store the read data.

   Note: Bit 8 of SBUF1 is not yet updated because the rising edge of the 9th clock has not yet occurred.
   - Return to * in step 6) to continue receive processing.
7) Sending data
   - Clear SI1REC.
   - Load SBUF1 with output data.
   - Clear SI1END and exit interrupt processing. (Send an acknowledge for the preceding receive operation and release the clock port after the lapse of (SBR1 value + 1/3) × Tcyc.)
   - Clear SI1END and exit interrupt processing. (Send an acknowledge for the preceding receive operation and release the clock port after the lapse of (SBR1 value + 1/3) × Tcyc.)
   - Clear SI1END and exit interrupt processing. (Send an acknowledge for the preceding receive operation and release the clock port after the lapse of (SBR1 value + 1/3) × Tcyc.)

*1 • Perform a send operation (8 bits) and set the clock output to 0 on the falling edge of the 8th clock, after which an interrupt occurs.

*2 • Go to *3 in step 7) when SI1RUN is set to 1.

• When SI1RUN is set to 0, implying an interrupt from *4 in step 7), clear SI1END and SI1OVR and return to *1 in step 4).

*3 • Read SBUF1 and check send data as required.

Note: Bit 8 of SBUF1 is not yet updated because the rising edge of the 9th clock has not yet occurred.

• Load SBUF1 with the next output data.

• Clear SI1END and exit interrupt processing. (Release the clock port after the lapse of (SBR1 value + 1/3) × Tcyc).

• Return to *1 in step7) if an acknowledge from the master is present (L).

• If there is no acknowledge from the master (H), SIO1, recognizing the end of data transmission, automatically clears SI1RUN and releases the data port.

* However, if the restart condition occurs just after the event, SI1REC must be set to 1 before exiting the interrupt. (SI1REC is for detecting a start condition and is not set automatically).

It may disturb the transmission of address from the master if there is an unexpected restart just after the slave's transmission (when SI1REC is not set to 1 with an instruction).

*4 • When a stop condition is detected, an interrupt is generated and processing returns to *2 in step 7).

8) Terminating communication

• Set SI1REC.

• Return to * in step 6) to automatically terminate communication.

• To force communication to terminate, clear SI1RUN and SI1END (release the clock port).

* • An interrupt occurs when a stop condition is detected. Then, clear SI1END and SI1OVR and return to *2 in step 4).

3.7.5 Related Registers

3.7.5.1 SIO1 control register (SCON1)

1) This register is an 8-bit register that controls the operation and interrupts of SIO1.

Address	Initial Value	R/W	Name	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE34	0000 0000	R/W	SCON1	-	SI1M1	SI1M0	SI1RUN	SI1REC	SI1DIR	SI1OVR	SI1END	SI1IE

SI1M1 (bit 7): SIO1 mode control

SI1M0 (bit 6): SIO1 mode control

Table 3.7.2 SIO1 Operating Modes

Mode	SI1M1	SI1M0	Operating Mode
0	0	0	Synchronous 8-bit SIO
1	0	1	Inhibited
2	1	0	Bus master mode
3	1	1	Bus slave mode

SI1RUN (bit 5): SIO1 operation flag

<1> A 1 in this bit indicates that SIO1 is running.

<2> See Table 3.7.1 for the conditions for setting and clearing this bit.

SI1REC (bit 4): SIO1 receive/send control

<1> Setting this bit to 1 places SIO1 into reception mode.

<2> Setting this bit to 0 places SIO1 into transmission mode.

SI1DIR (bit 3): MSB/LSB first select

<1> Setting this bit to 1 places SIO1 into MSB first mode.

<2> Setting this bit to 0 places SIO1 into LSB first mode.

SI1OVR (bit 2): SIO1 overrun flag

<1> In modes 0, 1, and 3, this bit is set when the falling edge of the input clock is detected with SI1RUN = 0

<2> This bit is set if the conditions for setting SI1END are established when SI1END=1.

<3> In mode 3 this bit is set when the start condition is detected.

<4> This bit must be cleared with an instruction.

SI1END (bit 1): Serial transfer end flag

<1> This bit is set when serial transfer terminates (see Table 3.7.1).

<2> This bit must be cleared with an instruction.

SI1IE (bit 0): SIO1 interrupt request enable control

When this bit and SI1END are set to 1, an interrupt request to vector address 003BH is generated.

3.7.5.2 Serial buffer 1 (SBUF1)

1) Serial buffer 1 is a 9-bit register used to store data to be handled during SIO1 serial transmission.
2) The low-order 8 bits of SBUF1 are transferred to the data shift register for data transmission/ reception at the beginning of transmit processing and the contents of the shift register are placed in the low-order 8 bits of SBUF1 when 8-bit data is transferred.
3) In modes 2, and 3, bit 8 of SBUF1 is loaded with the 9th data bit that is received (data on the position of the stop bit).

Address	Initial Value	R/W	Name	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE35	00000 0000	R/W	SBUF1	SBUF18	SBUF17	SBUF16	SBUF15	SBUF14	SBUF13	SBUF12	SBUF11	SBUF10

3.7.5.3 Baudrate generator register (SBR1)

1) The baudrate generator register is an 8-bit register that defines the baudrate of SIO1. (Modes 0, 2)
2) Loading this register with data causes the baudrate generating counter to be initialized immediately.
3) The baudrate varies from mode to mode

   Modes 0 and 2: TSBR1 = (SBR1 value + 1) × 2 Tcyc
   (Value range = 2 to 512 Tcyc)
4) When in mode 3, it sets up the acknowledge-data-set-up-time (See 3.7.4.3 6), 7)). When setting to mode 3, time that clock port is released after SI1END is cleared is

   (SBR1 value + 1/3) × Tcyc (SBR1=0 is inhibited)

   Set this value to meet the opponent device's data-set-up-time.

Address	Initial Value	R/W	Name	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE36	0000 0000	R/W	SBR1	-	SBRG17	SBRG16	SBRG15	SBRG14	SBRG13	SBRG12	SBRG11	SBRG10

3.8 Asynchronous Serial Interface (UART1)

3.8.1 Overview

This series of microcontrollers incorporates an asynchronous serial interface (UART1) that has the following characteristics and functions:

1) Data length: 7/8/9 bits (LSB first)
2) Stop bits: 1 bit (2 bits in continuous transmit mode)
3) Parity bits: None
4) Clock rate: Programmable within the range of $(\frac{16}{3}$ to $\frac{2048}{3})$ Tcyc or $(\frac{64}{3}$ to $\frac{8192}{3})$ Tcyc
5) Full duplex communication

   The independent transmitter and receiver blocks allow both transmit and receive operations to be performed at the same time. Both transmitter and receiver blocks adopt a double buffer configuration, so that data can be transmitted and received continuously.

3.8.2 Functions

1) Asynchronous serial (UART1)
   - Performs full duplex asynchronous serial communication using a data length of 7, 8, or 9 bits with 1 stop bit.
   - The transfer rate of the UART1 is programmable within the range of $(\frac{16}{3}$ to $\frac{2048}{3})$ Tcyc or $(\frac{64}{3}$ to $\frac{8192}{3})$ Tcyc.

2) Continuous data transmission/reception
   - Performs continuous transmit and receive operation whose data length and clock rate are fixed (The data length and clock rate that are identified at the beginning of transmit operation are used).
   - The number of stop bits used in the continuous transmit mode is 2 (see Figure 3.8.4).
   - Performs continuous data receive operation whose data length and clock rate vary on each receive operation.
   - The clock rate of the UART1 is programmable within the range of $(\frac{16}{3}$ to $\frac{2048}{3})$ Tcyc or $(\frac{64}{3}$ to $\frac{8192}{3})$ Tcyc.
   - The transmit data is read from the transmit data register (TBUF) and the received data is stored in the receive data register (RBUF).

3) Interrupt generation

   An interrupt request is generated at the beginning of transmit operation and at the end of receive operation if the interrupt request enable bit is set.

4) It is necessary to manipulate the following special function registers to control the asynchronous serial interface 1 (UART1).
   - UCON0, UCON1, UBR, TBUF, RBUF, P0, P0DDR

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FED0	0000 0000	R/W	UCON0	UBRSEL	STRDET	RECRUN	STPERR	U0B3	RBIT8	RECEND	RECIE
FED1	0000 0000	R/W	UCON1	TRUN	8/9BIT	TDDR	TCMOS	8/7BIT	TBIT8	TEPTY	TRNSIE
FED2	0000 0000	R/W	UBR	UBRG7	UBRG6	UBRG5	UBRG4	UBRG3	UBRG2	UBRG1	UBRG0
FED3	0000 0000	R/W	TBUF	T1BUF7	T1BUF6	T1BUF5	T1BUR4	T1BUF3	T1BUF2	T1BUF1	T1BUF0
FED4	0000 0000	R/W	RBUF	R1BUF7	R1BUF6	R1BUF5	R1BUR4	R1BUF3	R1BUF2	R1BUF1	R1BUF0

3.8.3 Circuit Configuration

3.8.3.1 UART1 control register 0 (UCON0) (8-bit register)

1) This register controls the receive operation and interrupts for the UART1.

3.8.3.2 UART1 control register 1 (UCON1) (8-bit register)

1) This register controls the transmit operation, data length, and interrupts for the UART1.

3.8.3.3 UART1 baudrate generator (UBR) (8-bit reload counter)

1) This generator is a reload counter for generating internal clocks.
2) It can generate clocks at intervals of $(n + 1) \times \frac{8}{3}$ Tcyc or $(n + 1) \times \frac{32}{3}$ Tcyc (n = 1 to 255; Note: n = 0 is inhibited).

3.8.3.4 UART1 transmit data register (TBUF) (8-bit register)

1) This register is an 8-bit register for storing the data to be transmitted.

3.8.3.5 UART1 transmit shift register (TSFT) (11-bit shift register)

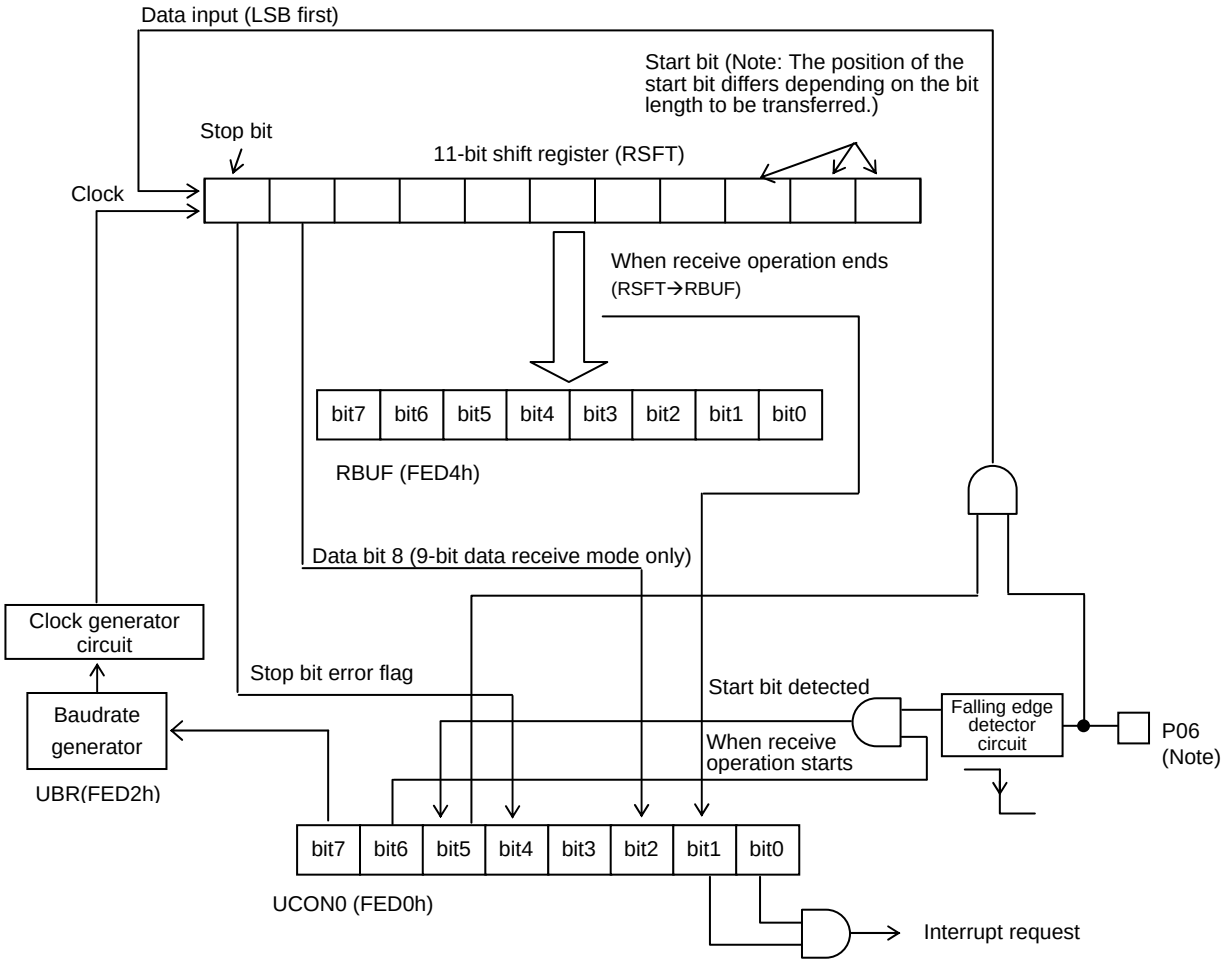
1) This register is used to send transmit data via the UART1.
2) This register cannot be accessed directly with an instruction. It must be accessed through the transmit data register (TBUF).

3.8.3.6 UART1 receive data register (RBUF) (8-bit register)

1) This register is an 8-bit register for storing receive data.

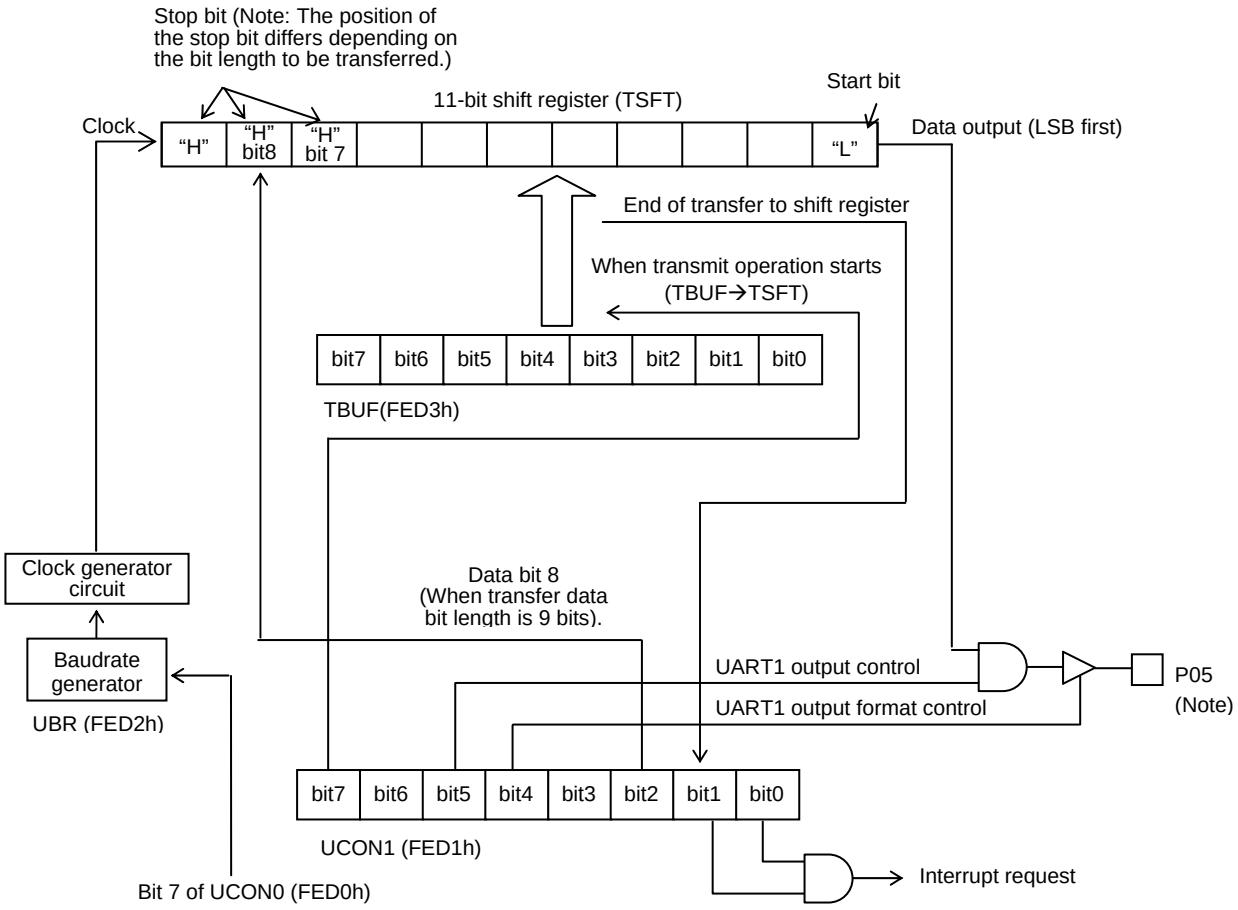
3.8.3.7 UART1 receive shift register (RSFT) (11-bit shift register)

1) This register is used to receive serial data via the UART1.
2) This register cannot be accessed directly with an instruction. It must be accessed through the receive data register (RBUF).



Note: Bit 6 of P0DDR (at FE41) must be set to 0 when the UART1 is to be used in receive mode (The UART1 will not function normally if this bit is set to 1).

Figure 3.8.1 UART1 Block Diagram (Receive Mode)



Note: Bit 5 of P0DDR (at FE41) must be set to 0 when the UART1 transmit data is to be output (Transmit data is not output if this bit is set to 1).

Figure 3.8.2 UART1 Block Diagram (Transmit Mode)

3.8.4 Related Registers

3.8.4.1 UART1 control register 0 (UCON0)

1) This register is an 8-bit register that controls the receive operation and interrupts for the UART1.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FED0	0000 0000	R/W	UCON0	UBRSEL	STRDET	RECRUN	STPERR	U0B3	RBIT8	RECEND	RECIE

UBRSEL (bit 7): UART1 baudrate generator period control

<1> When this bit is set to 1, the UART1 baudrate generator generates clocks at a frequency of (n + 1) × ($\frac{32}{3}$)Tcyc

<2> When this bit is set to 0, the UART1 baudrate generator generates clocks at a frequency of (n + 1) × ($\frac{8}{3}$)Tcyc.

*n: Represents the value that is defined in the UART baudrate generator (UBR:FED2).

STRDET (bit 6): UART1 start bit detection control

<1> When this bit is set to 1, the start bit detection (falling edge detection) function is enabled.

<2> When this bit is set to 0, the start bit detection (falling edge detection) function is disabled.

* This bit must be set to 1 to enable the start bit detection function when the UART1 is to be used in continuous receive mode.

* If this bit is set to 1 when the receive port (P06) is held at a low level, RECRUN is automatically set and the UART1 starts the receive operation.

RECRUN (bit 5): UART1 receive operation start flag

<1> This bit is set and a receive operation starts when a falling edge of the signal at the receive port (P06) is detected when the start bit detection function is enabled (STRDET = 1).

<2> This bit is automatically cleared at the end of the receive operation. (If this bit is cleared during the receive operation, the operation is aborted in the middle of the processing.)

* When a receive operation is forced to terminate prematurely, RECEND is set to 1 and the contents of the receive shift register are transferred to RBUF. STPERR is set to 1 if the state of the last data bit that is received on the forced termination is low.

STPERR (bit 4): UART1 stop bit error flag

<1> This bit is set at the end of a receive operation if the state of the received stop bit (the last data bit received) is low.

<2> This bit must be cleared with an instruction.

U0B3 (bit 3): General-purpose flag

<1> This bit can be used as a general-purpose flag bit.

Any attempt to manipulate this bit exerts no influence on the operation of this functional block.

RBIT8 (bit 2): UART1 receive data bit 8 storage bit

<1> This bit position is loaded with bit 8 of the received data at the end of a receive operation when the data length is set to 9 bits (UCON1: 8/9BIT = 1, 8/7BIT = 0). (If the receive operation is terminated prematurely, this bit position is loaded with the last received bit but one.)

<2> This bit must be cleared with an instruction.

RECEND (bit 1): UART1 receive end flag

<1> This bit is set at the end of a receive operation (When this bit is set, the received data is transferred from the receive shift register (RSFT) to the receive data register (RBUF)).

<2> This bit must be cleared with an instruction.

* In the continuous receive mode, the next receive operation is not carried out even when the UART1 detects such data as sets the receive operation start flag (RECRUN) before this bit is set.

RECIE (bit 0): UART1 receive interrupt request enable control

<1> When this bit and RECEND are set to 1, an interrupt request to vector address 0033H is generated.

3.8.4.2 UART1 control register 1 (UCON1)

1) This register is an 8-bit register that controls the transmit operation, data length, and interrupts for the UART1.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FED1	0000 0000	R/W	UCON1	TRUN	8/9BIT	TDDR	TCMOS	8/7BIT	TBIT8	TEPTY	TRNSIE

TRUN (bit 7): UART1 transmit control

<1> When this bit is set to 1, the UART1 starts a transmit operation.

<2> This bit is automatically cleared at the end of the transmit operation. (f this bit is cleared during the transmit operation, the operation is aborted in the middle of the processing.)

* In continuous transmit mode, this bit is cleared at the end of a transmit operation but is automatically set within the same cycle (Tcyc). Consequently, transmit operations occur with intervening 1-Tcyc delays.

* In continuous transmit mode, TRUN will not be set automatically if a bit-manipulation-instruction (NOT1, CLR1, or SET1) is executed to the UCON1 register in the same cycle in which TRUN is to be automatically cleared.

8/9BIT (bit 6): UART1 transfer data length control

<1> This bit and 8/7BIT (bit 3) are used to control the transfer data length for the UART1.

8/9 BIT	8/7 BIT	Data Length (in bits)
1	0	9
0	0	8
0	1	7
1	1	Inhibited

* The UART1 will not run normally if the data length is changed in the middle of a transfer operation. Be sure to manipulate this bit after confirming completion of the transfer operation.

* The same data length is used when both transmit and receive operations are to be performed at the same time.

TDDR (bit 5): UART1 transmit port output control

<1> When this bit is set to 1, the transmit data is placed at the transmit port (P05). No transmit data is generated if bit 5 of P0DDR (FE41) is set to 1.

<2> When this bit is set to 0, no transmit data is placed at the transmit port (P05).

* The transmit port generates a high/open (CMOS/N-channel open drain) signal if this bit is set to 1 when the UART1 has stopped a transmit operation (TRUN = 0).

* This bit must always be set to 0 when the UART1 transmit function is not to be used.

TCMOS (bit 4): UART1 transmit port output type control

<1> When this bit is set to 1, the output type of the transmit port (P05) is set to CMOS.

<2> When this bit is set to 0, the output type of the transmit port (P05) is set to N-channel open drain.

8/7BIT (bit 3): UART1 transmit data length control

<1> This bit and 8/9BIT (bit 6) are used to control the transfer data length of UART1.

TBIT8 (bit 2): UART1 transmit data bit 8 storage bit

<1> This bit stores bit 8 of the transmit data when the data length is set to 9 bits (8/9BIT = 1, 8/7BIT = 0).

TEPTY (bit 1): UART1 transmit shift register transfer flag

<1> This bit is set when the data transfer from the transmit data register (TBUF) to the transmit shift register (TSFT) ends after the start of the transmit operation. (This bit is set in the cycle (Tcyc) following the one in which the transmit control bit (TRUN) is set to 1.)

<2> This bit must be cleared with an instruction.

* When performing a continuous transmit operation, make sure that this bit is set before each loading of the next transmit data into the transmit data register (TBUF). When this bit is subsequently cleared, the transmit control bit (TRUN) is automatically set at the end of the transmit operation.

TRNSIE (bit 0): UART1 transmit interrupt request enable control

<1> An interrupt request to vector address 003BH is generated when this bit and TEPTY are set to 1.

3.8.4.3 UART1 baudrate generator (UBR)

1) This generator is an 8-bit register that defines the transfer rate of the UART1 transfer.

2) The counter for the baudrate generator is initialized when a UART1 transfer operation is suspended or terminated (UCON0: RECRUN = 0, UCON1: TRUN = 0).

* Do not change the transfer rate in the middle of a UART1 serial transfer operation. The UART1 will not function normally if the transfer rate is changed. Always make sure that the transfer operation has ended before changing the baudrate.

* The same baudrate is used when both transmit and receive operations are to be performed at the same time (This also holds true when the continuous transmit and receive operations are to be performed at the same time).

* When (UCON0:UBRSEL = 0)

TUBR = (UBR value + 1) × $\frac{8}{3}$ Tcyc (value range: $\frac{16}{3}$ to $\frac{2048}{3}$ Tcyc)

* When (UCON0:UBRSEL=1)

TUBR = (UBR value + 1) × $\frac{32}{3}$ Tcyc (value range: $\frac{64}{3}$ to $\frac{8192}{3}$ Tcyc)

* Setting the UBR to 00[H] is inhibited.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FED2	0000 0000	R/W	UBR	UBRG7	UBRG6	UBRG5	UBRG4	UBRG3	UBRG2	UBRG1	UBRG0

3.8.4.4 UART1 transmit data register (TBUF)

1) This register is an 8-bit register that stores the data to be transmitted through the UART1.
2) Data from the TBUF is transferred to the transmit shift register (TSFT) at the beginning of a transmit operation. (Load the next data after checking the transmit shift register transfer flag (UCON1: TEPTY).)

* Bit 8 of the transmit data must be loaded into the transmit data bit 8 storage bit (UCON1:TBIT8).

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FED3	0000 0000	R/W	TBUF	T1BUF7	T1BUF6	T1BUF5	T1BUF4	T1BUF3	T1BUF2	T1BUF1	T1BUF0

3.8.4.5 UART1 receive data register (RBUF)

1) This register is an 8-bit register that stores the data that is received through the UART1.
2) The data from the receive shift register (RSFT) is transferred to this RBUF at the end of a receive operation.

* Bit 8 of the received data is placed in the receive data bit 8 storage bit (UCON0:RBIT8).

* Bit 7 of RBUF is set to 0 when the receive data length is 7 bits.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FED4	0000 0000	R/W	RBUF	R1BUF7	R1BUF6	R1BUF5	R1BUF4	R1BUF3	R1BUF2	R1BUF1	R1BUF0

3.8.5 UART1 Continuous Communication Processing Examples

3.8.5.1 Continuous 8-bit data receive mode (first received data = 55H)

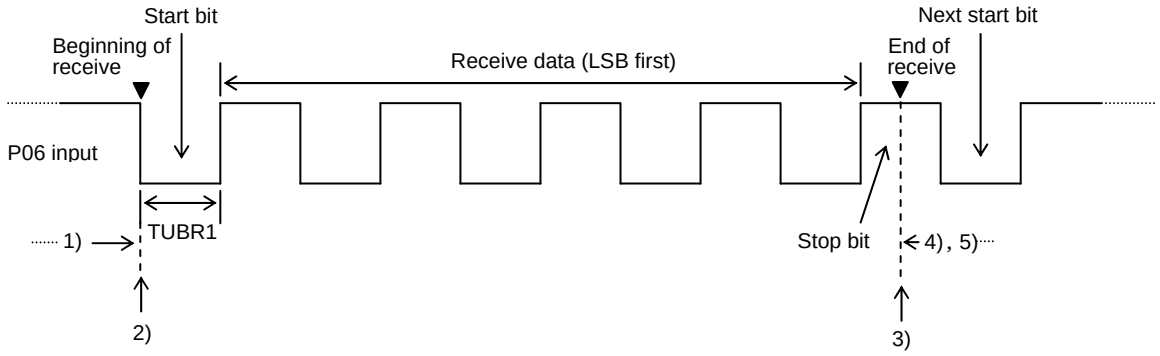


Figure 3.8.3 Example of Continuous 8-bit Data Receive Mode Processing

1) Setting the clock
   - Set the transfer rate (UBR).

   Setting the data length
   - Clear UCON1:8/9BIT and 8/7BIT.

   Configuring the UART1 for receive processing and setting up the receive port and interrupts
   - Set up the receive control register (UCON0 = 41H).
   - * Set P06DDR (P0DDR:bit 6) to 0 and P06 (P0:bit 6) to 0.

2) Starting a receive operation
   - UCON0:RECRUN is set when a falling edge of the signal at the receive port (P06) is detected.

3) End of a receive operation
   - When the receive operation ends, UCON0:RECRUN is automatically cleared and UCON0: RECEND is set. The UART1 then waits for the start bit of the next receive data.

4) Receive interrupt processing
   - Read the received data (RBUF).
   - Clear UCON0:RECEND and STPERR and exit the interrupt routine.
   - * When changing the data length and transfer rate for the next receive operation, do so before the start bit (falling edge of the signal) is detected at the receive port (P06).

5) Receiving the next data
   - Subsequently, repeat steps 2), 3), and 4) above.
   - To end a continuous receive operation, clear UCON0:STRDET during a receive operation, and this receive operation will be the last receive operation that the UART1 executes.

3.8.5.2 Continuous 8-bit data transmit mode (first transmit data = 55H)

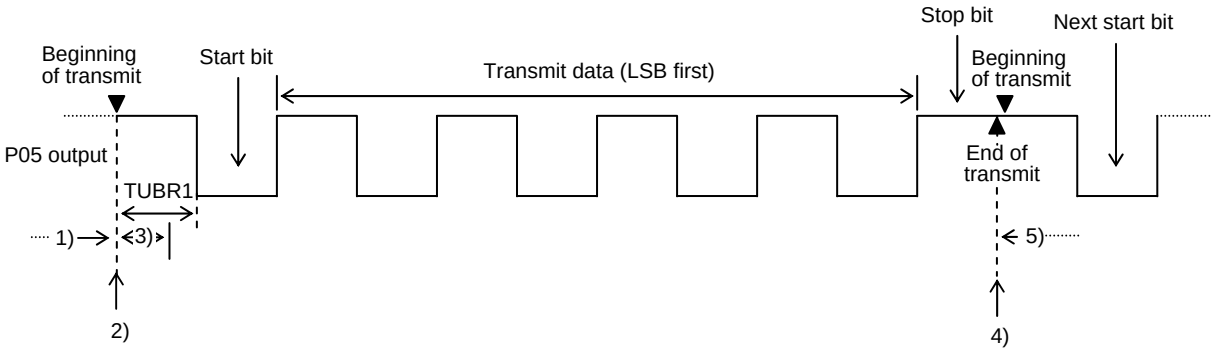


Figure 3.8.4 Example of Continuous 8-bit Data Transmit Mode Processing

1) Setting the clock
   - Set the transfer rate (UBR).

   Setting up transmit data
   - Load the transmit data (TBUF = 55H).

   Setting the data length, transmit port, and interrupts
   - Set up the transmit control register (UCON1 = 31H).
   - * Set P05DDR (P0DDR:bit 5) to 0 and P05 (P0:bit 5) to 0.

2) Starting a transmit operation
   - Set UCON1:TRUN.

3) Transmit interrupt processing
   - Load the next transmit data (TBUF = xxH).
   - Clear UCON1:TEPTY and exit the interrupt routine.

4) End of a transmit operation
   - When the transmit operation ends, UCON1:TRUN is automatically cleared and automatically set in the same cycle (Tcyc) (continuous data transmit mode only; this processing takes 1 Tcyc of time). The UART1 then starts to transmit the next data.

5) Transmitting the next data
   - Subsequently, repeat steps 3) and 4) above.
   - To end a continuous transmit operation, clear UCON1:TRNSIE while not clearing UCON1: TEPTY and exit the interrupt in the step 3) processing, and the transmit operation that is being performed at that time will be the last transmit operation that the UART1 executes.

3.8.5.3 Setting up the UART1 communications ports

When using port 0 as the UART1 port

1) Setting up the receive port (P06)

Register Data		Receive Port (P06) State	Internal Pull-up Resistor
P06	P06DDR		
0	0	Input	Off
1	0	Input	On

* The UART1 can receive no data normally if P06DDR is set to 1.

2) Setting up the transmit port (P05)

Register Data				Transmit Port (P05) State	Internal Pull-up Resistor
P05	P05DDR	TDDR	TCMOS		
0	0	1	1	CMOS output	Off
0	0	1	0	N-channel open drain output	Off
1	0	1	0	N-channel open drain output	On

* The UART1 transmits no data if P05DDR is set to 1.

3.8.6 UART1 HALT Mode Operation

3.8.6.1 Receive mode

1) A UART1 receive mode operation is enabled in HALT mode. (If UCON0:STRDET is set to 1 when the microcontroller enters HALT mode, the receive operation will be restarted if data that sets UCON0:RECRUN is input at the end of a receive operation.)
2) HALT mode can be released using the UART1 receive interrupt.

3.8.6.2 Transmit mode

1) A UART1 transmit mode operation is enabled in HALT mode. (If the continuous transmit mode is specified when the microcontroller enters HALT mode, the UART1 will restart transmit processing after terminating a transmit operation. Since UCON1:TEPTY cannot be cleared in this case, the UART1 stops processing after completing that transmit operation.)
2) HALT mode can be released using the UART1 transmit interrupt.

3.9 AD Converter (ADC12)

3.9.1 Overview

This series of microcontrollers incorporates a 12-bit resolution AD converter that has the features listed below. It allows the microcontroller to capture analog signals easily.

1) 12-bit resolution
2) Successive approximation
3) AD conversion mode select (resolution switching)
4) 5-channel analog input
5) Conversion time select
6) Automatic reference voltage generation control

3.9.2 Functions

1) Successive approximation
   - The AD converter has a resolution of 12 bits.
   - Some conversion time is required after starting conversion processing.
   - The conversion results are placed in the AD conversion result registers (ADRLC, ADRHC).

2) AD conversion select (resolution switching)

   The AD converter supports two AD conversion modes (12- and 8-bit conversion modes), so that the appropriate conversion resolution can be selected according to the operating conditions of the application. The AD mode register (ADMRC) is used to select the AD conversion mode.

3) 5-channel analog input

   The signal to be converted is selected using the AD control register (ADCRC) from 5 types of analog signals that are supplied from the P0 pin.

4) Conversion time select

   The AD conversion time can be set from 1/1 to 1/128 (frequency division ratio). The AD mode register (ADMRC) and AD conversion result register low byte (ADRLC) are used to select the conversion time for appropriate AD conversion.

5) Automatic reference voltage generation control

   The AD converter incorporates a reference voltage generator that automatically generates the reference voltage when an AD conversion starts and stops generation when the conversion ends. For this reason, set/reset control of reference voltage generation is not necessary. Also, there is no need to supply reference voltage externally.

6) It is necessary to manipulate the following special control registers to control the AD converter.
   • ADCRC, ADMRC, ADRLC, ADRHC

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE58	0000 0000	R/W	ADCRC	AD CHSEL3	AD CHSEL2	AD CHSEL1	AD CHSEL0	ADCR3	AD START	AD ENDF	ADIE
FE59	0000 0000	R/W	ADMRC	ADMD4	ADMD3	ADMD2	ADMD1	ADMD0	ADMR2	ADTM1	ADTM0
FE5A	0000 0000	R/W	ADRLC	DATAL3	DATAL2	DATAL1	DATAL0	ADRL3	ADRL2	ADRL1	ADTM2
FE5B	0000 0000	R/W	ADRHC	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

3.9.3 Circuit Configuration

3.9.3.1 AD conversion control circuit

1) The AD conversion control circuit runs in two modes: 12- and 8-bit AD conversion modes.

3.9.3.2 Comparator circuit

1) The comparator circuit consists of a comparator that compares the analog input with the reference voltage and a circuit that controls the reference voltage generator circuit and the conversion results. The conversion end flag (ADENDF) of the AD control register (ADCRC) is set when an analog input channel is selected and the AD conversion terminates in the conversion time designated by the conversion time control register. The conversion results are placed in the AD conversion result registers (ADRHC, ADRLC).

3.9.3.3 Multiplexer 1 (MPX1)

1) Multiplexer 1 is used to select the analog signal to be subject to AD conversion from 5 channels of analog signals.

3.9.3.4 Automatic reference voltage generator circuit

1) The automatic reference voltage generator circuit consists of a network of ladder resistors and a multiplexer (MPX2) and generates the reference voltage that is supplied to the comparator circuit. Generation of the reference voltage is automatically started when an AD conversion starts and automatically stopped when the conversion ends. The reference voltage output ranges from VDD to VSS.

3.9.4 Related Registers

3.9.4.1 AD control register (ADCRC)

1) This register is an 8-bit register that controls the operation of the AD converter.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE58	0000 0000	R/W	ADCRC	AD CHSEL3	AD CHSEL2	AD CHSEL1	AD CHSEL0	ADCR3	AD START	AD ENDF	ADIE

ADCHSEL3 (bit 7):
ADCHSEL2 (bit 6):
ADCHSEL1 (bit 5):
ADCHSEL0 (bit 4):
} **AD conversion input signal select**

These 4 bits are used to select the signal to be subject to AD conversion.

AD CHSEL3	AD CHSEL2	AD CHSEL1	AD CHSEL0	Signal Input Pin
0	0	0	0	P00/AN0
0	0	0	1	P01/AN1
0	0	1	0	P02/AN2
0	0	1	1	P03/AN3
0	1	0	0	P04/AN4

ADCR3 (bit 3): Fixed bit

This bit must always be set to 0.

ADSTART (bit 2): AD converter operation control

This bit starts (1) or stops (0) AD conversion processing. Setting this bit to 1 starts AD conversion. The bit is reset automatically when the AD conversion ends. The amount of time specified by the conversion time control register is required to complete the conversion. The conversion time is defined using three bits, i.e., ADTM2 (bit 0) of the AD conversion result register low byte (ADRLC) and ADTM1 (bit 1) and ADTM0 (bit 0) of the AD mode register (ADMRC).

Setting this bit to 0 stops the AD conversion. No correct conversion results can be obtained if this bit is cleared when AD conversion is in progress.

Never clear this bit or place the microcontroller in HALT or HOLD mode when AD conversion is in progress.

ADENDF (bit 1): AD conversion end flag

This bit identifies the end of AD conversion. It is set to 1 when AD conversion is finished. Then, an interrupt request to vector address 0043H is generated if ADIE is set to 1. If ADENDF is set to 0, it indicates that no AD conversion operation is in progress.

This flag must be cleared with an instruction.

ADIE (bit 0): AD conversion interrupt request enable control

An interrupt request to vector address 0043H is generated when this bit and ADENDF are set to 1.

Notes:

- *It is prohibited to set ADCHSEL3 to ADCHSEL0 to any value between '0101' and '1111.'*
- *Do not place the microcontroller in HALT or HOLD mode with ADSTART set to 1. Make sure that ADSTART is set to 0 before putting the microcontroller in HALT or HOLD mode.*

3.9.4.2 AD mode register (ADMRC)

1) This register is an 8-bit register that controls the operation mode of the AD converter.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE59	0000 0000	R/W	ADMRC	ADMD4	ADMD3	ADMD2	ADMD1	ADMD0	ADMR2	ADTM1	ADTM0

ADMD4 (bit 7): Fixed bit

This bit must always be set to 0.

ADMD3 (bit 6): AD conversion mode control (resolution select)

This bit selects the AD converter resolution between 12-bit AD conversion mode (0) and 8-bit AD conversion mode (1).

When this bit is set to 1, the AD converter operates as an 8-bit AD converter. The conversion results are placed only in the AD conversion result register high byte (ADRHC); the contents of the AD conversion result register low byte (ADRLC) remain unchanged.

When this bit is set to 0, the AD converter operates as a 12-bit AD converter. The conversion results are placed in the AD conversion result register high byte (ADRHC) and the high-order 4 bits of the AD conversion result register low byte (ADRLC).

ADMD2 (bit 5): Fixed bit

This bit must always be set to 0.

ADMD1 (bit 4): Fixed bit

This bit must always be set to 0.

ADMD0 (bit 3): Fixed bit

This bit must always be set to 0.

ADMR2 (bit 2): Fixed bit

This bit must always be set to 0.

ADTM1 (bit 1):
ADTM0 (bit 0): } **AD conversion time control**

These bits and ADTM2 (bit 0) of the AD conversion result register low byte (ADRLC) define the conversion time.

ADRLC Register	ADMRC Register		AD Frequency Division Ratio
ADTM2	ADTM1	ADTM0	
0	0	0	1/1
0	0	1	1/2
0	1	0	1/4
0	1	1	1/8
1	0	0	1/16
1	0	1	1/32
1	1	0	1/64
1	1	1	1/128

Conversion time calculation formulas

- 12-bit AD conversion mode: Conversion time = ((52/(AD division ratio)) + 2) × 1/3 × Tcyc
- 8-bit AD conversion mode: Conversion time = ((32/(AD division ratio)) + 2) × 1/3 × Tcyc

Notes:

- *The conversion time is doubled in the following cases:*
  <1>The AD conversion is carried out in the 12-bit AD conversion mode for the first time after a system reset.
  <2>The AD conversion is carried out for the first time after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.
- *The conversion time determined by the above formula is required in the second and subsequent conversions or in AD conversions that are carried out in the 8-bit AD conversion mode.*

3.9.4.3 AD conversion result register low byte (ADRLC)

1) This register is used to hold the low-order 4 bits of the results of an AD conversion carried out in the 12-bit AD conversion mode and to control the conversion time.
2) Since the data in this register is not established during an AD conversion, the conversion results must be read out only after the AD conversion is completed.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5A	0000 0000	R/W	ADRLC	DATAL3	DATAL2	DATAL1	DATAL0	ADRL3	ADRL2	ADRL1	ADTM2

DATAL3 (bit 7):
DATAL2 (bit 6):
DATAL1 (bit 5):
DATAL0 (bit 4):
} **Low-order 4 bits of AD conversion results**

ADRL3 (bit 3): Fixed bit

This bit must always be set to 0.

ADRL2 (bit 2): Fixed bit

This bit must always be set to 0.

ADRL1 (bit 1): Fixed bit

This bit must always be set to 0.

ADTM2 (bit 0): AD conversion time control

This bit and ADTM1 (bit 1) and ADTM0 (bit 0) of the AD mode register (ADMRC) are used to control the conversion time. See the subsection on the AD mode register for the procedure to set up the conversion time.

Note:

The conversion result data contains errors (quantization error + combination error). Be sure to use only valid conversion results based on specifications provided in the latest "SANYO Semiconductors Data Sheet."

3.9.4.4 AD conversion result register high byte (ADRHC)

1) In 12-bit AD conversion mode, this register stores the high-order 8 bits of the results of an AD conversion.
   In 8-bit AD conversion mode, the register stores the entire 8 bits of the results of an AD conversion.
2) Since the data in this register is not established during an AD conversion, the conversion results must be read out only after the AD conversion is completed.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5B	0000 0000	R/W	ADRHC	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0

3.9.5 AD Conversion Example

3.9.5.1 12-bit AD conversion mode

1) Setting up the 12-bit AD conversion mode
   - Set ADMD3 (bit 6) of the AD mode register (ADMRC) to 0.
2) Setting up the conversion time
   - To set the conversion time to 1/32 frequency division, set ADTM2 (bit 0) of the AD conversion result register low byte (ADRLC) to 1, ADTM1 (bit 1) of the AD mode register (ADMRC) to 0, and ADTM0 (bit 0) of the AD mode register (ADMRC) to 1.
3) Setting up the input channel
   - When using AD channel input AN4, set the AD control register (ADCRC): ADCHSEL3 (bit 7) to 0, ADCHSEL2 (bit 6) to 1, ADCHSEL1 (bit 5) to 0, and ADCHSEL0 (bit 4) to 0.
4) Starting AD conversion
   - Set ADSTART (bit 2) of the AD control register (ADCRC) to 1.
   - The conversion time is doubled when the AD conversion is carried out for the first time after a system reset or after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode. The conversion time determined by the formula is required in the second and subsequent conversions.
5) Detecting the AD conversion end flag
   - Monitor ADENDF (bit 1) of the AD control register (ADCRC) until it is set to 1.
   - Clear the conversion end flag (ADENDF) to 0 after confirming that the ADENDF flag (bit 1) is set to 1.
6) Reading the AD conversion results
   - Read the AD conversion result register high byte (ADRHC) and AD conversion result register low byte (ADRLC). Since the conversion result data contains errors (quantization error + combination error), use only the valid part of the conversion data selected according to the specifications provided in the latest “SANYO Semiconductors Data Sheet.”
   - Send the above read data to application software processing.
   - Return to step 4) to repeat conversion processing.

3.9.6 Hints on the Use of the ADC

1) The conversion time that the user can select varies depending on the frequency of the cycle clock. When preparing a program, refer to the latest “SANYO Semiconductors Data Sheet” to select an appropriate conversion time.

2) Setting ADSTART to 0 while conversion is in progress will stop the conversion function.

3) Do not place the microcontroller in HALT or HOLD mode while AD conversion processing is in progress. Make sure that ADSTART is set to 0 before putting the microcontroller in HALT or HOLD mode.

4) ADSTART is automatically reset and the AD converter stops operation if a reset is triggered while AD conversion processing is in progress.

5) When conversion is finished, the AD conversion end flag (ADENDF) is set and, at the same time, the AD conversion operation control bit (ADSTART) is reset. The end of conversion condition can be identified by monitoring ADENDF. Setting ADIE causes an interrupt request to vector address 0043H to be generated at the end of conversion.

6) The conversion time is doubled in the following cases:
   - The AD conversion is carried out in the 12-bit AD conversion mode for the first time after a system reset.
   - The AD conversion is carried out for the first time after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode.
   - The conversion time determined by the formula given in the paragraph entitled "Conversion time calculation formulas" is required in the second and subsequent conversions or in AD conversions that are carried out in the 8-bit AD conversion mode.

7) The conversion result data contains errors (quantization error + combination error). Be sure to use only valid conversion results based on specifications provided in the latest "SANYO Semiconductors Data Sheet."

8) Make sure that only input voltages that fall within the specified range are supplied to P00/AN0 to P04/AN4 pins. Application of high voltage of VDD or more or low voltage of VSS or less to an input pin may exert an adverse influence on the converted value of the channel in question or of other channels.

9) Take the following measures to prevent a reduction in conversion accuracy due to noise interference:
   - Add external bypass capacitors of several μF plus thousands of pF near the VDD1 and VSS1 pins (as close as possible, desirably 5 mm or less).
   - Add external low-pass filters (RC) or capacitors, most suitable for noise reduction, very close to the analog input pins. To avoid any adverse coupling influences, use a ground that is free of noise interference as the ground for the capacitors (rough standard values are: R = less than 5 kΩ, C=1000 pF to 0.1μF).
   - Do not lay analog signal lines close to, in parallel with, or in a crossed arrangement with digital pulse signal lines or signal lines in which large current changes can occur. Shield both ends of analog signal lines with noise-free ground shields.
   - Make sure that no digital pulses are applied to or generated out of pins adjacent to the analog input pin that is being subject to conversion.

- Correct conversion results may not be obtained because of noise interference if the state of port outputs is changing. To minimize the adverse influences of noise interference, it is necessary to keep line resistance across the power supply and the VDD pins of the microcontroller at a minimum. This should be kept in mind when designing an application circuit.
- Adjust the amplitudes of the voltage at the oscillator pin and the I/O voltages at the other pins so that they fall within the voltage range between VDD and VSS.

10) To obtain valid conversion data, perform conversion operations several times, discard the maximum and minimum values of the conversion results, and use an average of the remaining data.

3.10 Programmable Pulse Generator (PPG2)

3.10.1 Overview

The programmable pulse generator (PPG2) incorporated in this series of microcontrollers has a 12-bit counter that generates pulses whose width is determined arbitrarily through register configuration. Output from the internal comparator, which receives input from an external analog pin, can be used to synchronize the pulse output and to control forced reset processing.

3.10.2 Functions

1) PPG output

- Can generate pulses from the PPGO pin on each detection of the falling edge of the output of comparator 1 which receives inputs from external analog pins (CMP1IA and CMP1IB).
- Generates pulses with a duration of the pulse on-time after the lapse of the pulse start delay time as controlled by the low-order 11 bits of the 12-bit counter which runs on the internal high-speed RC oscillator clock (24 MHz typ), the pulse start delay setting register, and the pulse on-time setting register.

  The pulse on-time setting register can be loaded with one of the two values which can be selected with the pulse on-time setting select register.

  The pulse on-time setting select register is set on detection of the rising edge of the output of comparator 2 which receives input from an external analog pin (CMP2I) and the internal reference voltage input.
- Once pulses are generated, if the falling edge of comparator 1 output is not detected within the period determined by the comparator 1 detection timeout setting register, PPG2 can force pulses to be output.
- The PPG output is forced to be reset on detection of a high level at the output of comparator 3 whose inputs are from the output of amplifier 1, which receives input from an external analog pin (AMP1I), and from the internal reference voltage source.

  After the detection of the next falling edge of the comparator 1 output, however, PPG outputs are generated normally.
- The PPG output is forcibly stopped on detection of the rising edge of the output signal of comparator 7 whose inputs are from an external analog pin (CMP2I) and the internal reference voltage source (the PPG output control register is forced to be reset).
  The PPG output is regenerated by reconfiguring the PPG output control register using software.
- The PPG output is forcibly stopped by the output of the surge detector circuit (comparators 4, 5, and 6) whose inputs are from external analog pins (CMP4I, CMP45I, CMP5I, and CMP6I) (the PPG output control register is forced to be reset).

  The PPG output is regenerated by reconfiguring the PPG output control register using software.

  This function can be disabled using the surge detector circuit enable register.
- The PPG output can be generated from the P07 pin for signal monitoring.

2) PPG output pulse on-time capture operation

- The PPG output pulse on-time can be captured into the pulse on-time capture register on detection of a high level at the output of comparator 3 or comparator 8.

3) Comparator output

- The outputs of comparators 1 to 8 can be selected by the comparator output select register and the selected output can be transmitted from the P30 pin.

4) Amplifier 2 output
   - The level generated as a result of amplifying the input level from an external analog pin (AMP1I) through amplifiers 1 and 2 is output from AMP2O.

5) Interrupt generation
   - The output from comparator 1, whose input is from external analog pins (CMP1IA and CMP1IB), can be used as the INT2 interrupt input.
   - If the comparator 2 interrupt request enable bit is set, a comparator 2 interrupt request is generated on detection of the rising edge of the output of comparator 2 whose input is from an external analog pin (CMP2I) and the internal reference voltage source.
   - If the comparator 3 interrupt request enable bit is set, a comparator 3 interrupt request is generated on detection of a high level at the output of comparator 3 whose input is from the output of the amplifier 1 and the internal reference voltage source.
   - If the comparator 6 interrupt request enable bit is set, a comparator 6 interrupt request is generated on detection of the rising/falling edge of the output of comparator 6 whose input is from an external analog pin (CMP6I) and the internal reference voltage.
   - If the comparator 7 interrupt request enable bit is set, a comparator 7 interrupt request is generated on detection of the rising edge of the output of comparator 7 whose input is from an external analog pin (CMP2I) and the internal reference voltage source.
   - If the comparator 8 interrupt request enable bit is set, a comparator 8 interrupt request is generated on detection of a high level at the output of comparator 8 whose input is from the output of the amplifier 1 and the internal reference voltage source.
   - If the surge interrupt request enable bit is set, a surge interrupt request is generated on detection of a surge voltage.
   - If the comparator 1 detection timeout interrupt request enable bit is set, a comparator 1 detection timeout interrupt request is generated on the occurrence of a comparator 1 detection timeout condition.

6) It is necessary to manipulate the following special function registers to control the programmable pulse generator (PPG2).
   - P2CR1, P2CR2, P2DLY, P2EAL, P2EAH, P2EBL, P2EBH, P2CPL, P2CPH, P2CR3, P2CR4, P2CR5, P2C1DS, P2TOT, P2C3DS, P2C8DS

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE90	0000 0000	R/W	P2CR1	P2EN	P2ON	P2MD	P2SEN	P2SLPE	P2C2FG	P2SIRQ	P2SIEN
FE91	0000 0000	R/W	P2CR2	-	P2COSL2	P2COSL1	P2COSL0	P2POEN	P2COEN	P2A2C1	P2A2C0
FE92	0000 0000	R/W	P2DLY	P2DL7	P2DL6	P2DL5	P2DL4	P2DL3	P2DL2	P2DL1	P2DL0
FE94	0000 0000	R/W	P2EAL	P2EA7	P2EA6	P2EA5	P2EA4	P2EA3	P2EA2	P2EA1	P2EA0
FE95	HHHH H000	R/W	P2EAH	-	-	-	-	-	P2EAA	P2EA9	P2EA8
FE96	0000 0000	R/W	P2EBL	P2EB7	P2EB6	P2EB5	P2EB4	P2EB3	P2EB2	P2EB1	P2EB0
FE97	HHHH H000	R/W	P2EBH	-	-	-	-	-	P2EBA	P2EB9	P2EB8
FE98	0000 0000	R	P2CPL	P2CP7	P2CP6	P2CP5	P2CP4	P2CP3	P2CP2	P2CP1	P2CP0
FE99	0HHH H000	R	P2CPH	-	-	-	-	-	P2CPA	P2CP9	P2CP8
		R/W		P2CPSL	-	-	-	-	-	-	-
FE9A	HH00 0000	R/W	P2CR3	-	-	P2C3IRQ	P2C3IREN	P2C2IRQ	P2C2IREN	P2TOIRQ	P2TOIEN
FE9B	HH00 0000	R/W	P2CR4	-	-	P2C6VR1	P2C6VR0	P2C6HEG	P2C6LEG	P2C6IRQ	P2C6IEN
FE9C	HH00 0000	R/W	P2CR5	-	-	P2C8VR1	P2C8VR0	P2C8IRQ	P2C8IEN	P2C7IRQ	P2C7IEN
FE9D	0000 0000	R/W	P2C1DS	P2C1DS7	P2C1DS6	P2C1DS5	P2C1DS4	P2C1DS3	P2C1DS2	P2C1DS1	P2C1DS0
FE9E	0000 0000	R/W	P2TOT	P2 TOT7	P2 TOT6	P2 TOT5	P2 TOT4	P2 TOT3	P2 TOT2	P2 TOT1	P2 TOT0
FE9F	HH00 0000	R/W	P2C3DS	-	-	P2C3DS5	P2C3DS4	P2C3DS3	P2C3DS2	P2C3DS1	P2C3DS0
FEA0	HH00 0000	R/W	P2C8DS	-	-	P2C8DS5	P2C8DS4	P2C8DS3	P2C8DS2	P2C8DS1	P2C8DS0

3.10.3 Circuit Configuration

3.10.3.1 PPG2 control register 1 (P2CR1) (8-bit register)

1) This register controls the operation and interrupts of the PPG2.

3.10.3.2 PPG2 control register 2 (P2CR2) (7-bit register)

1) This register controls the port output from comparators 1 to 8.
2) The register controls the port output for PPG output monitoring.
3) The register is used to select the gain (1×, 2×, or 4×) of amplifier 2.

3.10.3.3 Amplifiers and comparators (AMP1/2,CMP1/2/3/4/5/6/7/8)

1) Amplifier 1: Amplifies the input from the external analog pin (AMP1I) (6×, 8×, or 10×) and submits the output as the input to amplifier 2, comparator 3, and comparator 8.
   * The gain (6×, 8×, or 10×) can be selected as a user option.
2) Amplifier 2: Amplifies the output from amplifier 1 (1×, 2×, or 4×) and transmits its output to an external analog pin (AMP2O).
   * The gain (1×, 2×, or 4×) can be switched based on the register settings.
3) Comparator 1: Compares the input from external analog pins (CMP1IA and CMP1IB).
4) Comparator 2: Compares the input from an external analog pin (CMP2I) with the internal reference voltage (5/12VDD to 7/12VDD).
   * The internal reference voltage can be selected as a user option.
5) Comparator 3: Compares the output from amplifier 1 with the internal reference voltage (1/6VDD to 4/6VDD).
   * The internal reference voltage can be selected as a user option.
6) Comparator 4: Compares the inputs from external analog pins (CMP4I, CMP45I).
7) Comparator 5: Compares the inputs from external analog pins (CMP5I, CMP45I).
8) Comparator 6: Compares the input from an external analog pin (CMP6I) with the internal reference voltage (1/6VDD to 4/6VDD).
   * The internal reference voltage can be switched based on the register settings.
9) Comparator 7: Compares the input from an external analog pin (CMP2I) with the internal reference voltage (6/12VDD to 8/12VDD).
   * The internal reference voltage can be selected as a user option.
10) Comparator 8: Compares the output from amplifier 1 with the internal reference voltage (1/6VDD to 4/6VDD).
   * The internal reference voltage can be switched based on the register settings.

* See Figure 3.10.1, "Amplifier/Comparator Block Diagram" and Figure 3.10.2, "Surge Detector Circuit Block Diagram."

3.10.3.4 Synchronization flag generator circuit

This circuit generates the PPG output synchronization flag at the following timings:

1) If P2MD (PPG2 control register 1, bit 5) =0: When generation of the PPG output is started.
2) If P2MD (PPG2 control register 1, bit 5) =1:
   - When generation of the PPG output is started.
   - When the falling edge of the comparator 1 output is detected.
   - When a comparator 1 detection timeout occurs.

* See Figure 3.10.3, "PPG Block Diagram 1."

3.10.3.5 12-bit counter

1) Operation start/stop: Stop/start is controlled by the 0/1 value of P2ON (PPG2 control register 1, bit 6).
2) Count clock: Internal high-speed RC oscillator clock (24 MHz typ)
3) Reset: • Synchronization flag from the synchronization flag generator circuit
   • Pulse start delay setting match flag
   • Pulse on-time setting match flag

* See Figure 3.10.3, "PPG Block Diagram 1."

3.10.3.6 Pulse start delay setting register (P2DLY) (8-bit register with match buffer register)

1) This register is used to store the match data used for setting the PPG output pulse start delay. It has an 8-bit match buffer register. The pulse start delay setting match flag is generated when the value of this match buffer register matches the value of the 12-bit counter.
2) The match buffer register is updated as follows:

   The match buffer register is loaded with the contents of P2DLY on the occurrence of the synchronization flag from the synchronization flag generator circuit.

* See Figure 3.10.3, "PPG Block Diagram 1."

3.10.3.7 Pulse on-time setting registers (P2EAL, P2EAH, P2EBL, P2EBH) (11-bit match buffer register, 11-bit register x 2)

1) These registers are used to store the match data for setting the PPG output pulse on-time. They are provided with an 11-bit match buffer register. The pulse on-time setting match flag is generated when the value of this match buffer register matches the value of the 12-bit counter.
2) The match buffer register is updated as follows:

   The match buffer register is loaded with the contents of either one of P2EAL, P2EAH, P2EBL, and P2EBH, selected by P2SLPE (PPG2 control register 1, bit 3), on the occurrence of the synchronization flag from the synchronization flag generator circuit.

* See Figure 3.10.3, "PPG Block Diagram 1."

3.10.3.8 PPG output

1) If P2ON (PPG2 control register 1, bit 6)=1, the PPG output is set by the pulse start delay setting match flag and reset by the pulse on-time setting match flag. It is also reset by the high level detection flag output from comparator 3.
2) If P2ON (PPG2 control register 1, bit 6)=0, the PPG output is in the reset state.
3) The PPG output can be transmitted from the PPGO pin.

   * The polarity of the PPG output can be inverted as a user option.

* The PPG output can also be transmitted from the P07 pin for signal monitoring.
* See Figure 3.10.3, "PPG Block Diagram 1," Figure 3.10.6, "PPG Output Timing 1" and Figure 3.10.8, "PPG Output Timing 3."

3.10.3.9 Pulse on-time capture registers (P2CPL, P2CPH) (1-bit register with buffer register, 11-bit register)

1) This is an 11-bit register for storing the PPG output pulse on-time that is captured on a capture trigger. It is provided with a 1-bit register with buffer register which is used to select the type of the capture trigger.
2) Capture trigger:

   Used to detect the high level of the comparator 3 output or comparator 8 output.
3) The buffer register is updated as follows:

The buffer register is loaded with the contents of P2CPH, bit 7 on the occurrence of a synchronization flag from the synchronization flag generator circuit.

3.10.3.10 PPG2 control register 3 (P2CR3) (6-bit register)

1) This register controls the comparator 2 interrupt processing.
2) This register controls the comparator 3 interrupt processing.
3) The register controls the comparator 1 detection timeout interrupt processing.

3.10.3.11 PPG2 control register 4 (P2CR4) (6-bit register)

1) This register controls the internal reference voltage and interrupt processing for comparator 6.

3.10.3.12 PPG2 control register 5 (P2CR5) (6-bit register)

1) This register controls the comparator 7 interrupt processing.
2) The register controls the internal reference voltage and interrupt processing for comparator 8.

3.10.3.13 Comparator 1 detection disabled period setting register (P2C1DS) (8-bit register with match buffer register)

1) This is a register for storing the match data that is used to set up the comparator 1 disabled period. It has an 8-bit match buffer register. The comparator 1 disabled period setting match flag is generated when the value of this match buffer register matches the value of the 12-bit counter.
2) The match buffer register is updated as follows:

   The match buffer register is loaded with the contents of P2C1DS on the occurrence of a synchronization flag from the synchronization flag generator circuit.
3) The interval from the occurrence of the synchronization flag to the occurrence of the comparator 1 detection disabled period setting match flag is the detection disabled period for comparator 1.

* See Figure 3.10.4, "PPG Block Diagram 2" and Figure 3.10.6, "PPG Output Timing 1."

3.10.3.14 Comparator 1 detection timeout setting register (P2TOT) (8-bit register with match buffer register)

1) This is a register for storing the match data that is used to set up the comparator 1 detection timeout value. It has an 8-bit match buffer register. The comparator 1 detection timeout setting match flag (synchronization flag) is generated when the value of this match buffer register matches the value of the 12-bit counter.
2) The match buffer register is updated as follows:

   The match buffer register is loaded with the contents of P2TOT on the occurrence of a synchronization flag from the synchronization flag generator circuit.
3) When a comparator 1 detection timeout occurs, a PPG output is generated in synchronization with the comparator 1 detection timeout setting match flag (synchronization flag).

* See Figure 3.10.4, "PPG Block Diagram 2" and Figure 3.10.7, "PPG Output Timing 2."

3.10.3.15 Comparator 3 detection disabled period setting register (P2C3DS) (6-bit register with match buffer register)

1) This is a register for storing the match data that is used to set up the comparator 3 disabled period. It has a 6-bit match buffer register. The comparator 3 disabled period setting match flag is generated when the value of this match buffer register matches the value of the 12-bit counter.
2) The match buffer register is updated as follows:

The match buffer register is loaded with the contents of P2C3DS on the occurrence of a synchronization flag from the synchronization flag generator circuit.

3) The interval from the occurrence of the synchronization flag to the occurrence of the comparator 3 detection disabled period setting match flag is the detection disabled period for comparator 3.

* See Figure 3.10.5, "PPG Block Diagram 3" and Figure 3.10.8, "PPG Output Timing 3."

3.10.3.16 Comparator 8 detection disabled period setting register (P2C8DS) (6-bit register with match buffer register)

1) This is a register for storing the match data that is used to set up the comparator 8 disabled period. It has a 6-bit match buffer register. The comparator 8 disabled period setting match flag is generated when the value of this match buffer register matches the value of the 12-bit counter.

2) The match buffer register is updated as follows:
The match buffer register is loaded with the contents of P2C8DS on the occurrence of a synchronization flag from the synchronization flag generator circuit.

3) The interval from the occurrence of the synchronization flag to the occurrence of the comparator 8 detection disabled period setting match flag is the detection disabled period for comparator 8.

* See Figure 3.10.5, "PPG Block Diagram 3" and Figure 3.10.10, "PPG Output Timing 5."

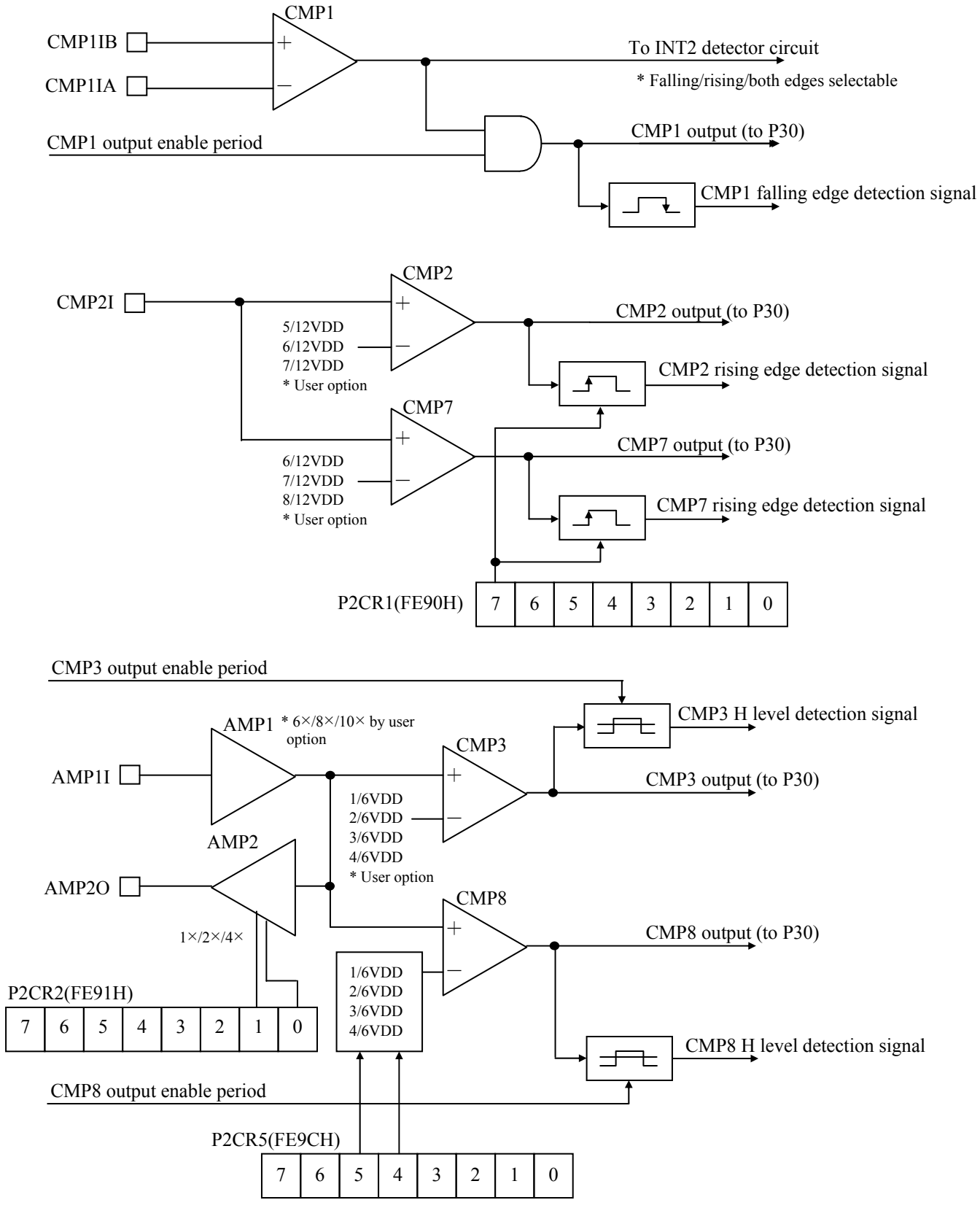


Figure 3.10.1 Amplifier/Comparator Block Diagram

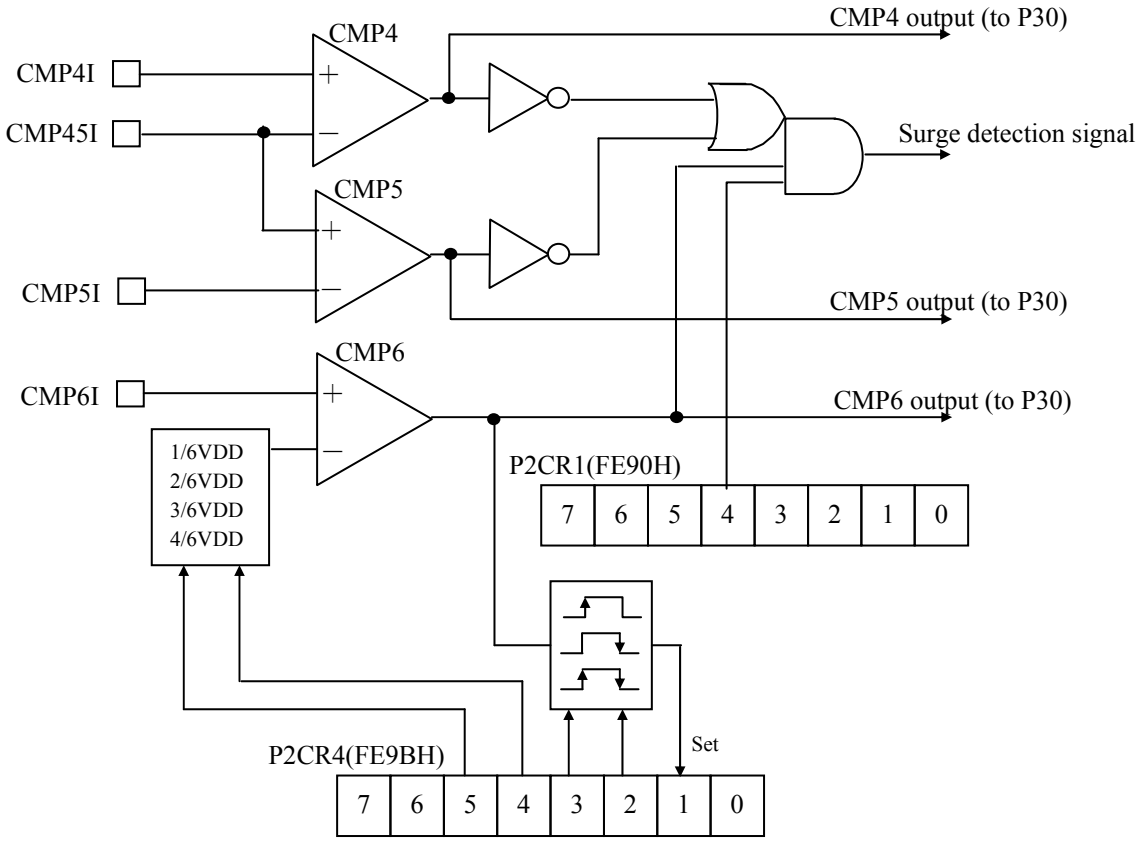


Figure 3.10.2 Surge Detector Circuit Block Diagram

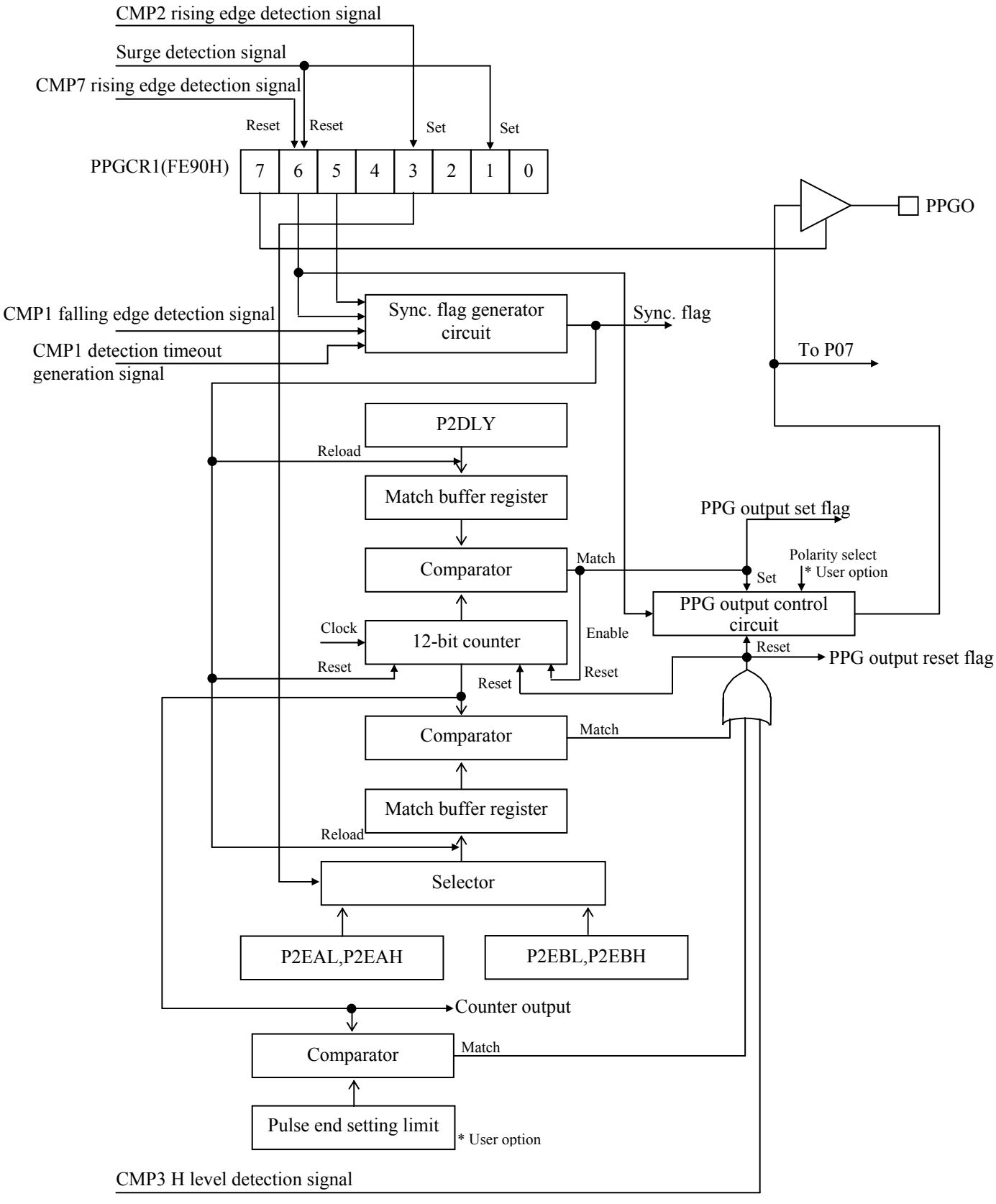


Figure 3.10.3 PPG Block Diagram 1

PPG2

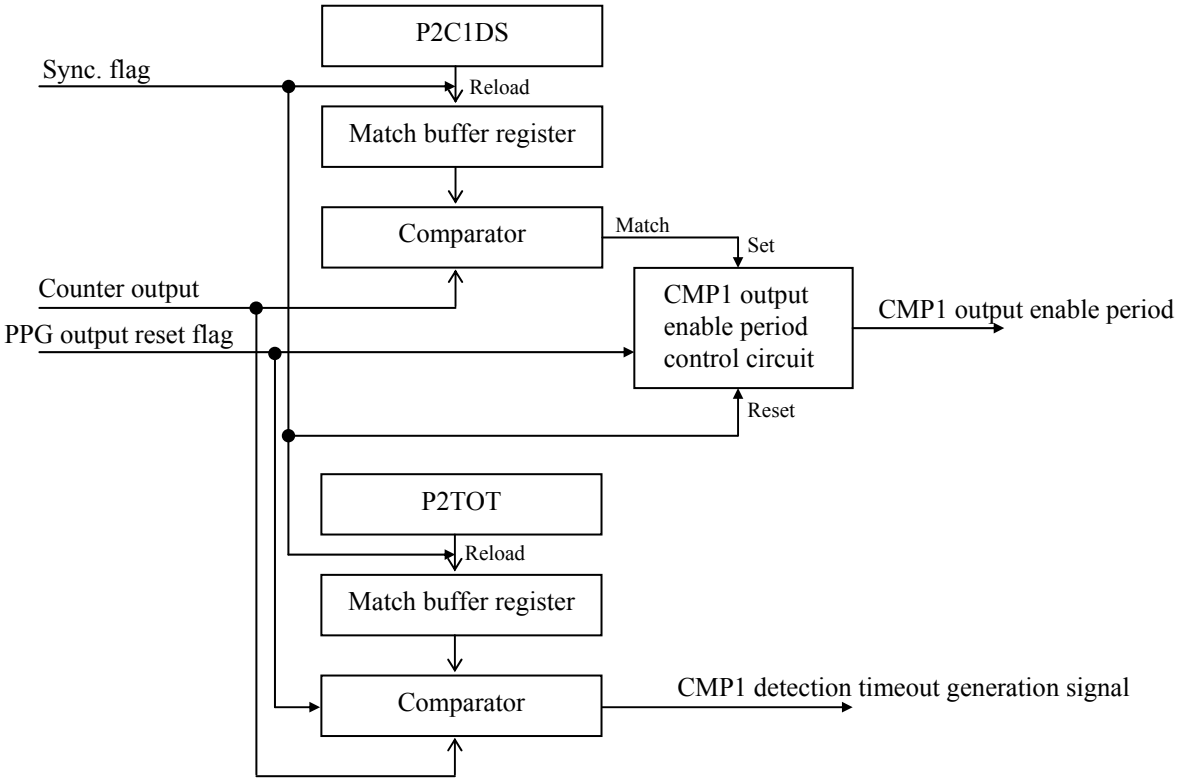


Figure 3.10.4 PPG Block Diagram 2

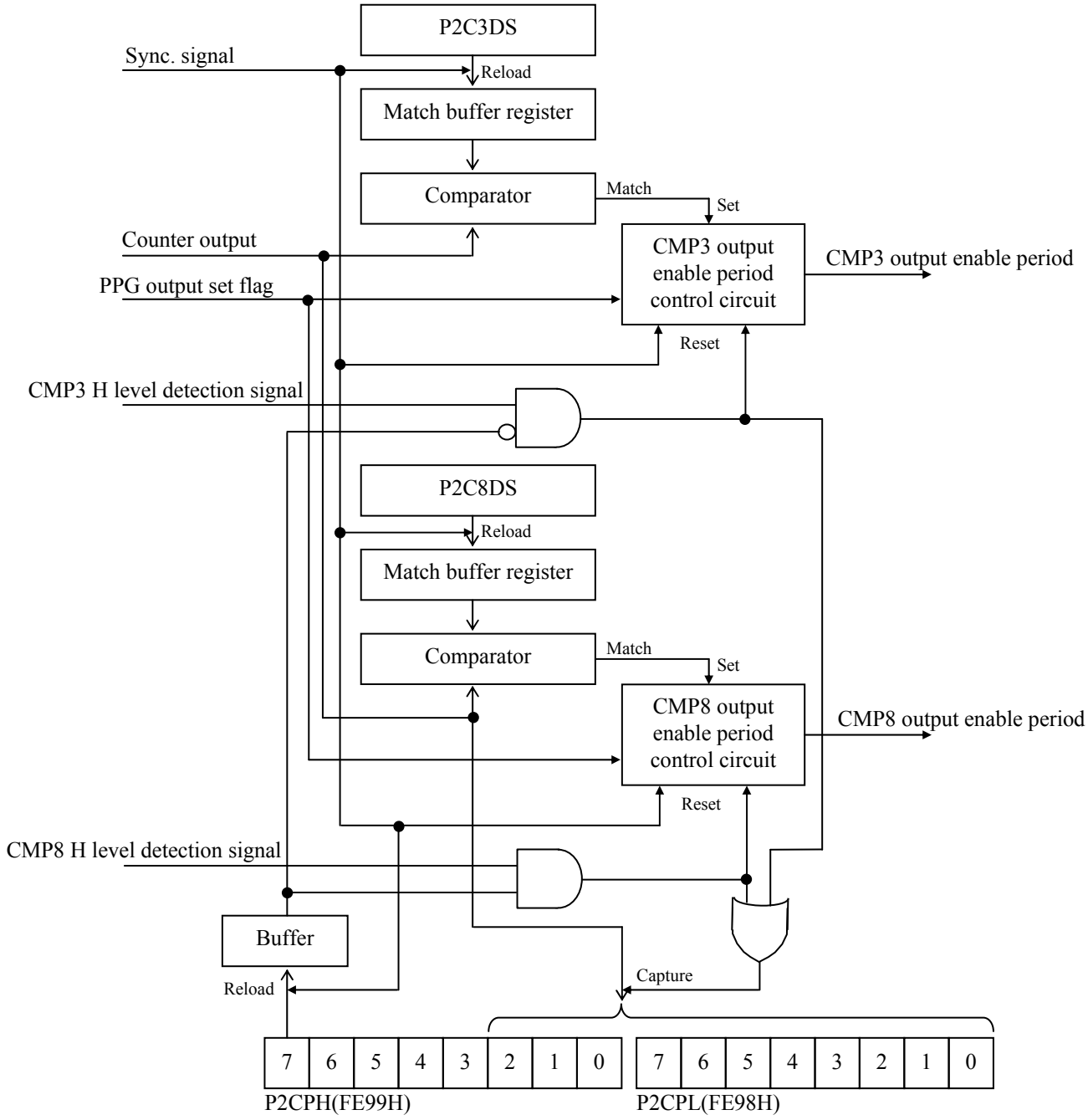


Figure 3.10.5 PPG Block Diagram 3

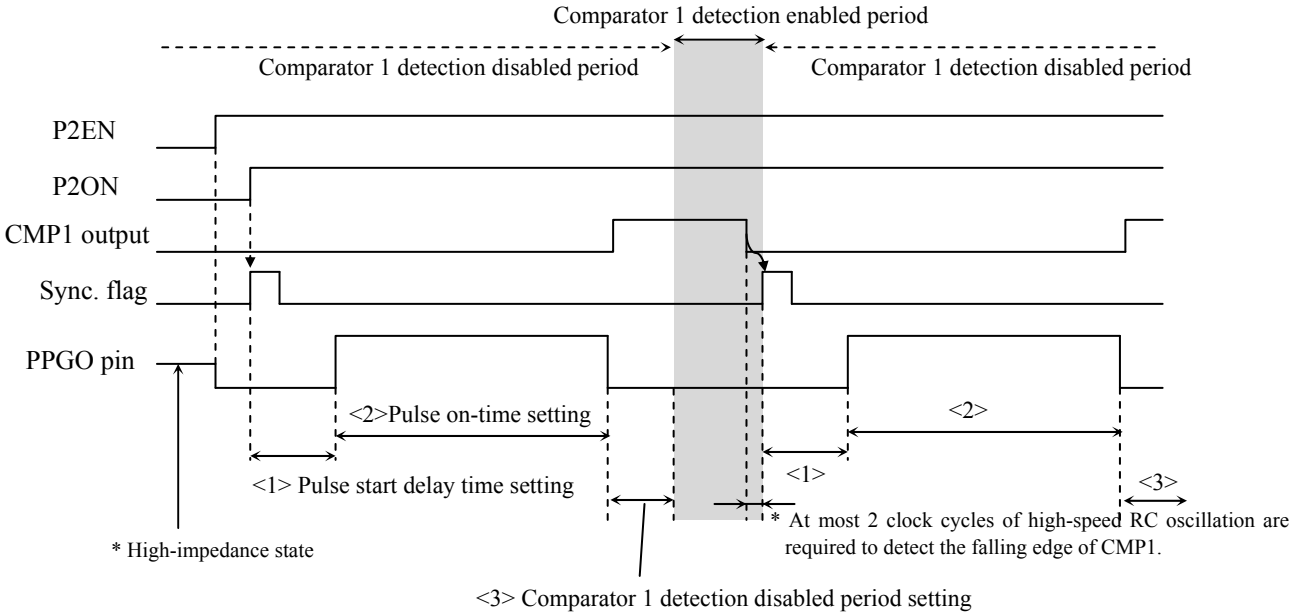


Figure 3.10.6 PPG Output Timing 1
(Normal Mode, PPG Output Polarity Option=No Polarity Inversion, P2MD=1)

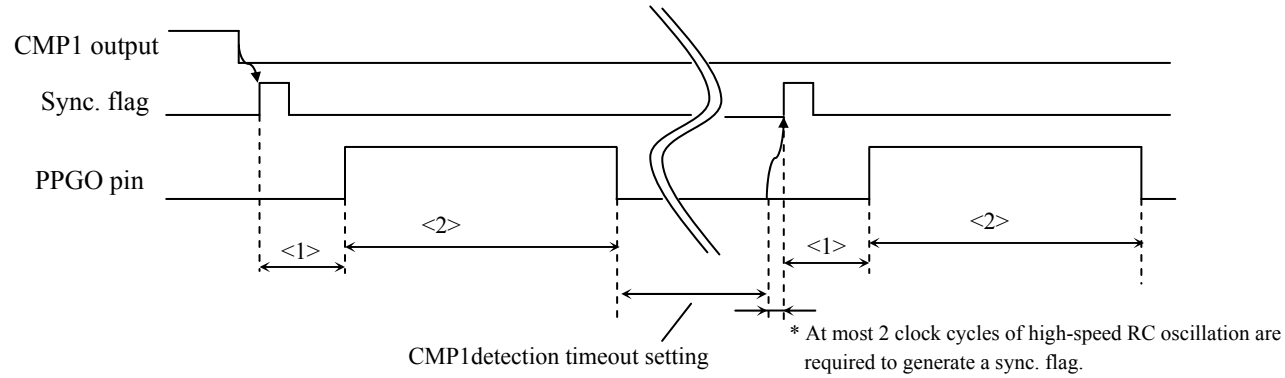


Figure 3.10.7 PPG Output Timing 2
(Comparator 1 Detection Timeout Occurred,
PPG Output Polarity Option=No Polarity Inversion, P2MD=1)

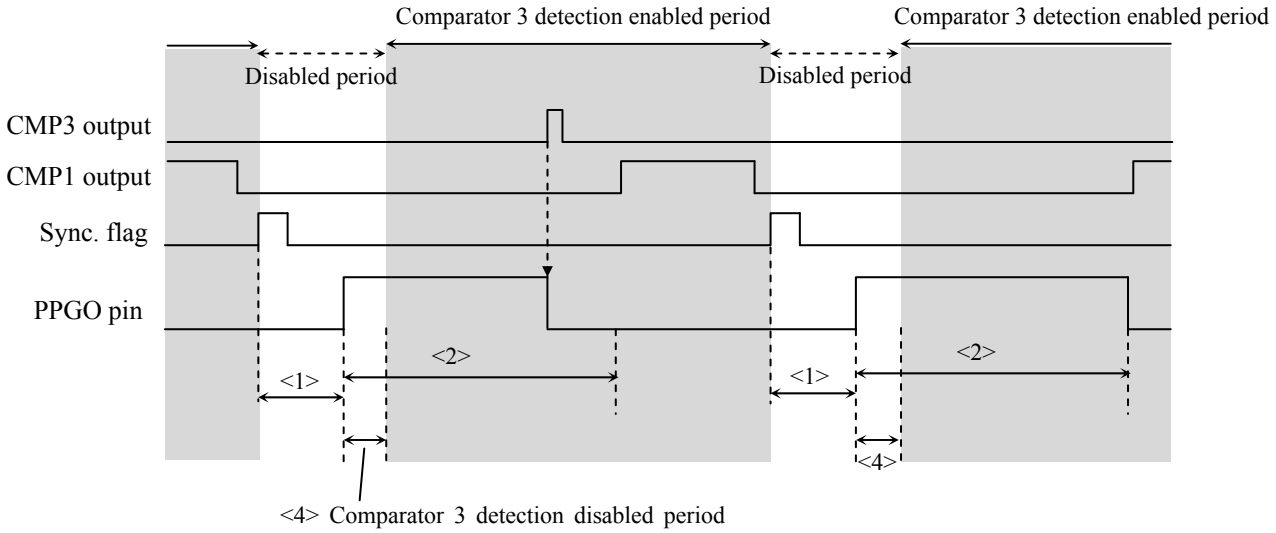


Figure 3.10.8 PPG Output Timing 3
(High Level Comparator 3 Output Detected,
PPG Output Polarity Option=No Polarity Inversion, P2MD=1, P2CPSL=1)

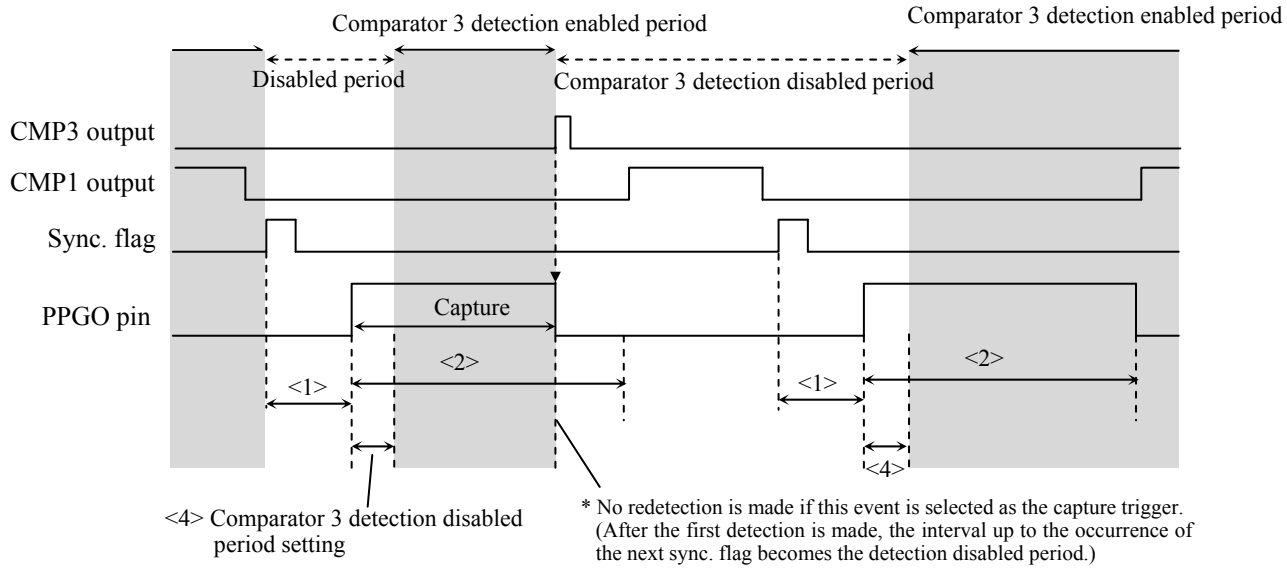


Figure 3.10.9 PPG Output Timing 4
(High Level Comparator 3 Output Detected,
PPG Output Polarity Option=No Polarity Inversion, P2MD=1, P2CPSL=0)

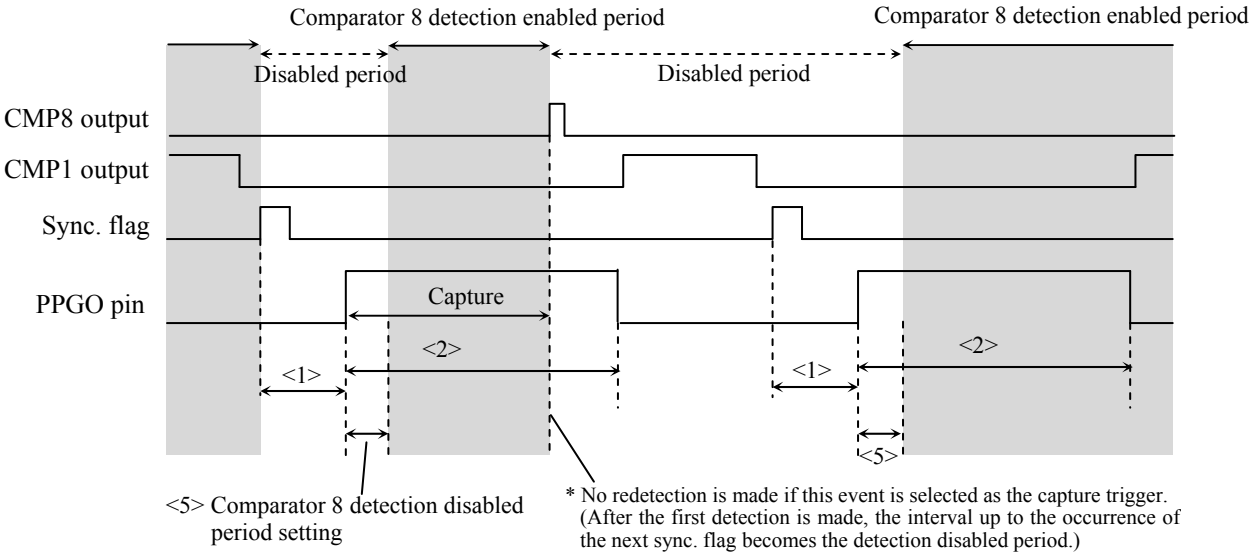


Figure 3.10.10 PPG Output Timing 5
(High Level Comparator 8 Output Detected,
PPG Output Polarity Option=No Polarity Inversion, P2MD=1, P2CPSL=1)

3.10.4 Related Registers

3.10.4.1 PPG2 control register 1 (P2CR1)

1) This register is an 8-bit register that controls the operation and interrupts of the PPG2.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE90	0000 0000	R/W	P2CR1	P2EN	P2ON	P2MD	P2SEN	P2SLPE	P2C2FG	P2SIRQ	P2SIEN

P2EN (bit 7): PPG2 operation control

When this bit is set to 0, the PPGO pin is placed in a high-impedance state, with no PPG output present at that pin.

When this bit is set to 1, the PPG output is transmitted from the PPGO pin.

P2ON (bit 6): PPG output control

When this bit is set to 0, the PPG output is in the reset state.

When this bit is set to 1, the PPG generates pulses that are determined by the pulse start delay setting register and pulse on-time setting register.

This bit is reset when a surge is detected by the surge detector circuit (comparators 4/5/6) or when the rising edge of the comparator 7 output is detected while the PPG2 is running (P2EN=1).

P2MD (bit 5): PPG output mode control

When this bit is set to 0, the synchronization flag generator circuit generates the synchronization flag only when the PPG output is started (P2ON=0→1 is configured). Only the start pulse (1 pulse) is generated as the PPG output.

When this bit is set to 1, the synchronization flag generator circuit generates the synchronization flag when the PPG output is started (P2ON=0→1 is configured), when a falling edge of the comparator 1 output is detected, or when a comparator 1 timeout occurs. The PPG outputs that are generated are the start pulse (1 pulse) and the pulses that are generated each time a falling edge of the comparator 1 output is detected or a comparator 1 timeout occurs.

P2SEN (bit 4): Surge detector circuit enable

When this bit is set to 0, the surge detector circuit (comparators 4/5/6) is disabled.

When this bit is set to 1, the surge detector circuit (comparators 4/5/6) is enabled.

P2SLPE (bit 3): Pulse on-time setting select

When this bit is set to 0, the match buffer register is reloaded with the data from the pulse on-time setting A register.

When this bit is set to 1, the match buffer register is reloaded with the data from the pulse on-time setting B register.

This bit is set on detection of the rising edge of the comparator 2 output while the PPG2 is running (P2EN=1).

P2C2FG (bit 2): Comparator 2 output rising edge detection history flag

This bit maintains a history of whether a rising edge of the comparator 2 output is detected during the period from the detection of the falling edge of the preceding comparator 1 output to the detection of the falling edge of the current comparator 1 output, while the PPG2 is generating PPG outputs (P2EN=1, P2ON=1) and after the detection of the falling edge of the comparator 1 output. The bit is set to 1 if there is a detection of the rising edge of the comparator 2 output and set to 0 otherwise.

P2SIRQ (bit 1): Surge detection flag

This bit is set when a surge is detected while the PPG2 is running (P2EN=1).

This flag must be cleared with an instruction.

P2SIEN (bit 0): Surge interrupt request enable control

When this bit and P2SIRQ are set to 1, an interrupt request to vector address 004BH is generated.

Notes:

- *When the PPG2 is running (P2EN=1), activate the internal high-speed RC oscillator and select it as the system clock source.*
- *P2MD is enabled when output of PPG pulses is started (when P2ON is switched from 0 to 1). Consequently, any changes made while the PPG output is active (P2ON=1) are invalid.*

3.10.4.2 PPG2 control register 2 (P2CR2)

1) This is a 7-bit register that controls the comparator output, the PPG output for signal monitoring, and the operation of amplifier 2.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE91	0000 0000	R/W	P2CR2	-	P2COSL2	P2COSL1	P2COSL0	P2POEN	P2COEN	P2A2C1	P2A2C0

P2COSL2 (bit 6):
P2COSL1 (bit 5):
P2COSL0 (bit 4):
} **Comparator output select**

Setting these bits allows selection of the comparator whose output is to be transmitted from P30.

P2COSL2	P2COSL1	P2COSL0	Comparator Selected
0	0	0	Comparator 1
0	0	1	Comparator 2
0	1	0	Comparator 3
0	1	1	Comparator 4
1	0	0	Comparator 5
1	0	1	Comparator 6
1	1	0	Comparator 7
1	1	1	Comparator 8

P2POEN (bit 3): Signal monitoring PPG output control

A 1 in this bit enables the PPG output for signal monitoring to be generated through P72

P2COEN (bit 2): Comparator output control

A 1 in this bit enables the comparator that is selected by the comparator output select register to generate output through P30.

A 0 in this bit enables buzzer output to be generated through P30.

P2A2C1 (bit 1):
P2A2C0 (bit 0): } **Amplifier 2 gain control**

These bits select the gain of amplifier 2.

P2A2C1	P2A2C0	Amplifier 2 Gain
0	0	1×
0	1	2×
1	0	4×
1	1	Inhibited

Notes:

- *To generate comparator output/buzzer output from P30, it is also necessary to set up registers for port 3 (P30=0, P30DDR=1).*
- *To generate PPG output for signal monitoring from P07, it is also necessary to set up registers for port 0 (P07=0, P07DDR=1.)*

3.10.4.3 Pulse start delay setting register (P2DLY)

1) This register is an 8-bit register used to define the pulse start delay for the PPG outputs.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE92	0000 0000	R/W	P2DLY	P2DL7	P2DL6	P2DL5	P2DL4	P2DL3	P2DL2	P2DL1	P2DL0

P2DL7 to P2DL0: Pulse start delay settings

These bits define the pulse start delay time from the time the synchronization flag is set until the time the PPG output is set. See Figure 3.10.6, "PPG Output Timing 1," for details.

Pulse start delay time = Set value × 1/FmMRC

(FmMRC: Internal high-speed RC oscillator frequency)

Note:

- *The pulse start delay time established by setting P2DL7 to P2DL0 to 00h is identical to the one that is established by setting P2DL7 to P2DL0 to 01h.*

3.10.4.4 Pulse on-time setting A register low byte (P2EAL)

1) This is an 8-bit register used to define the pulse on-time of the PPG output.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE94	0000 0000	R/W	P2EAL	P2EA7	P2EA6	P2EA5	P2EA4	P2EA3	P2EA2	P2EA1	P2EA0

3.10.4.5 Pulse on-time setting A register high byte (P2EAH)

1) This is a 3-bit register used to define the pulse on-time of the PPG output.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE95	HHHH H000	R/W	P2EAH	-	-	-	-	-	P2EAA	P2EA9	P2EA8

3.10.4.6 Pulse on-time setting B register low byte (P2EBL)

1) This is an 8-bit register used to define the pulse on-time of the PPG output.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE96	0000 0000	R/W	P2EBL	P2EB7	P2EB6	P2EB5	P2EB4	P2EB3	P2EB2	P2EB1	P2EB0

3.10.4.7 Pulse on-time setting B register high byte (P2EBH)

1) This is a 3-bit register used to define the pulse on-time of the PPG output.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE97	HHHH H000	R/W	P2EBH	-	-	-	-	-	P2EBA	P2EB9	P2EB8

P2EAA to P2EA0: Pulse on-time setting A

P2EBA to P2EB0: Pulse on-time setting B

These bits define the pulse on-time until the time the PPG output is reset after the expiration of the pulse start delay time. See Figure 3.10.6, "PPG Output Timing 1," for details.

Pulse on-time = Set value × 1/FmMRC

(FmMRC: Internal high-speed RC oscillator frequency)

Notes:

- *The pulse on-time established by setting P2EAA to P2EA0 to 000h is identical to the one that is established by setting P2EAA to P2EA0 to 001h.*
- *The pulse on-time established by setting P2EBA to P2EB0 to 000h is identical to the one that is established by setting P2EBA to P2EB0 to 001h.*

3.10.4.8 Pulse on-time capture register low byte (P2CPL)

1) This register is an 8-bit register used to store the pulse on-time of the PPG output.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE98	0000 0000	R	P2CPL	P2CP7	P2CP6	P2CP5	P2CP4	P2CP3	P2CP2	P2CP1	P2CP0

3.10.4.9 Pulse on-time capture register high byte (P2CPH)

1) This register is a 4-bit register used to store the pulse on-time of the PPG output and to select the capture trigger.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE99	0HHH H000	R	P2CPH	-	-	-	-	-	P2CPA	P2CP9	P2CP8
		R/W		P2CPSL	-	-	-	-	-	-	-

P2CPSL (bit 7): Pulse on-time capture trigger select

When this bit is set to 0, the detection of a high level at the output of comparator 3 is designated as the pulse on-time capture trigger.

When this bit is set to 1, the detection of a high level at the output of comparator 8 is designated as the pulse on-time capture trigger.

P2CPA to P2CP0: Pulse on-time

These bits are loaded with the PPG output pulse on-time (low-order 11 bits of the 12-bit counter) as triggered by the high-level detected at the output of comparator 3 or comparator 8. See Figure 3.10.9, "PPG Output Timing 4" and Figure 3.10.10, "PPG Output Timing 5," for details.

Pulse on-time = Stored value × 1/FmMRC

(FmMRC: Internal high-speed RC oscillator frequency)

Note:

- *P2CPA to P2CP0 are loaded with 000h if a capture trigger occurs when the PPG output is in the reset state.*

3.10.4.10 PPG2 control register 3 (P2CR3)

1) This is a 6-bit register that controls the comparator 2/3 interrupt and comparator 1 detection timeout interrupt.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE9A	HH00 0000	R/W	P2CR3	-	-	P2C3IRQ	P2C3IEN	P2C2IRQ	P2C2IEN	P2TOIRQ	P2TOIEN

P2C3IRQ (bit 5): Comparator 3 interrupt request flag

This bit is set when a high level is detected at the comparator 3 output while the PPG2 is running (P2EN=1).

This flag must be cleared with an instruction.

P2C3IEN (bit 4): Comparator 3 interrupt request enable control

When this bit and P2C3IRQ are set to 1, an interrupt request to vector address 000BH is generated.

P2C2IRQ (bit 3): Comparator 2 interrupt request flag

This bit is set when a rising edge of the comparator 2 output is detected while the PPG2 is running (P2EN=1).

This flag must be cleared with an instruction.

P2C2IEN (bit 2): Comparator 2 interrupt request enable control

When this bit and P2C2IRQ are set to 1, an interrupt request to vector address 0003H is generated.

P2TOIRQ (bit 1): Comparator 1 detection timeout interrupt request flag

This bit is set when a comparator 1 detection timeout occurs while the PPG2 is running (P2EN=1).

This flag must be cleared with an instruction.

P2TOIEN (bit 0): Comparator 1 detection timeout interrupt request enable control

When this bit and P2TOIRQ are set to 1, an interrupt request to vector address 0043H is generated.

3.10.4.11 PPG2 control register 4 (P2CR4)

1) This is a 6-bit register that controls the internal reference voltage and interrupts for comparator 6.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE9B	HH00 0000	R/W	P2CR4	-	-	P2C6VR1	P2C6VR0	P2C6HEG	P2C6LEG	P2C6IRQ	P2C6IEN

P2C6VR1 (bit 5):
P2C6VR0 (bit 4): } **Comparator 6 internal reference voltage setting**

These bits select the level of the internal reference voltage for comparator 6.

P2C6VR1	P2C6VR0	Comparator 6 Internal Reference Voltage
0	0	1/6VDD
0	1	2/6VDD
1	0	3/6VDD
1	1	4/6VDD

P2C6HEG (bit 3): Comparator 6 rising edge detection control

P2C6LEG (bit 2): Comparator 6 falling edge detection control

P2C6HEG	P2C6LEG	Comparator 6 Interrupt Conditions
0	0	Not detected
0	1	Falling edge detected
1	0	Rising edge detected
1	1	Both edges detected

P2C6IRQ (bit 1): Comparator 6 interrupt request flag

This bit is set when the conditions specified by P2C6HEG and P2C6LEG are satisfied while the PPG2 is running (P2EN=1).

This flag must be cleared with an instruction.

P2C6IEN (bit 0): Comparator 6 interrupt request enable control

When this bit and P2C6IRQ are set to 1, an interrupt request to vector address 004BH is generated.

3.10.4.12 PPG2 control register 5 (P2CR5)

1) This is a 6-bit register that controls the internal reference voltage and interrupts for comparators 7/8.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE9C	HH00 0000	R/W	P2CR5	-	-	P2C8VR1	P2C8VR0	P2C8IRQ	P2C8IEN	P2C7IRQ	P2C7IEN

P2C8VR1 (bit 5):
P2C8VR0 (bit 4): } **Comparator 8 internal reference voltage setting**

These bits select the level of the internal reference voltage for comparator 8.

P2C8VR1	P2C8VR0	Comparator 8 Internal Reference Voltage
0	0	1/6VDD
0	1	2/6VDD
1	0	3/6VDD
1	1	4/6VDD

P2C8IRQ (bit 3): Comparator 8 interrupt request flag

This bit is set when a high level is detected at the comparator 8 output while the PPG2 is running (P2EN=1).

This flag must be cleared with an instruction.

P2C8IEN (bit 2): Comparator 8 interrupt request enable control

When this bit and P2C8IRQ are set to 1, an interrupt request to vector address 000BH is generated.

P2C7IRQ (bit 1): Comparator 7 interrupt request flag

This bit is set when a rising edge of the comparator 7 output is detected while the PPG2 is running (P2EN=1).

This flag must be cleared with an instruction.

P2C7IEN (bit 0): Comparator 7 interrupt request enable control

When this bit and P2C7IRQ are set to 1, an interrupt request to vector address 0003H is generated.

3.10.4.13 Comparator 1 detection disabled period setting register (P2C1DS)

1) This is an 8-bit register that controls the detection disabled period for comparator 1.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE9D	0000 0000	R/W	P2C1DS	P2C1DS7	P2C1DS6	P2C1DS5	P2C1DS4	P2C1DS3	P2C1DS2	P2C1DS1	P2C1DS0

P2C1DS7 to P2C1DS0: Comparator 1 detection disabled period setting

- These bits define the detection disabled period for comparator 1 with respect to the PPG output reset timing.

  Comparator 1 detection disabled period = (Set value × 4 + 1) × 1/FmMRC

  (FmMRC: Internal high-speed RC oscillator frequency)

- In addition to the above period, the interval from the generation of the synchronization flag (when generation of the PPG output is started, when a comparator 1 falling edge is detected or when a comparator 1 detection timeout occurs) until the resetting of the PPG output is included in the detection disabled period. See Figure 3.10.6, "PPG Output Timing 1," for details.

3.10.4.14 Comparator 1 detection timeout setting register (P2TOT)

1) This is an 8-bit register that controls the detection timeout value for comparator 1.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE9E	0000 0000	R/W	P2TOT	P2 TOT7	P2 TOT6	P2 TOT5	P2 TOT4	P2 TOT3	P2 TOT2	P2 TOT1	P2 TOT0

P2TOT7 to P2TOT0: Comparator 1 detection timeout setting

- These bits define the detection timeout value for comparator 1 with respect to the PPG output reset timing.

  Timeout value = (Set value × 16 + 1) × 1/FmMRC

  (FmMRC: Internal high-speed RC oscillator frequency)

- When the detection timeout time expires, a synchronization flag is generated and the PPG output is generated. See Figure 3.10.7, "PPG Output Timing 2," for details.
- Control of the timeout value is disabled and the synchronization flag is not generated in the following cases:

  <1> P2MD (PPG2 control register 1, bit 5) is set to 0.

  <2> P2TOT7 to P2TOT0 are set to 00h.

  <3> Comparator 1 detection disabled period > Timeout value

3.10.4.15 Comparator 3 detection disabled period setting register (P2C3DS)

1) This is a 6-bit register that controls the detection disabled period for comparator 3.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE9F	HH00 0000	R/W	P2C3DS	-	-	P2C3DS5	P2C3DS4	P2C3DS3	P2C3DS2	P2C3DS1	P2C3DS0

P2C3DS5 to P2C3DS0: Comparator 3 detection disabled period setting

- These bits define the detection disabled period for comparator 3 with respect to the PPG output set timing.

  Comparator 3 detection disabled period= (Set value × 4 + 1) × 1/FmMRC

  (FmMRC: Internal high-speed RC oscillator frequency)

- In addition to the above period, the interval from the generation of the synchronization flag (when a comparator 1 falling edge is detected or when a comparator 1 detection timeout occurs) until the setting of the PPG output is included in the detection disabled period.
- When comparator 3 detection disabled period > pulse on-time, the detection disabled period expires at the timing of the PPG output resetting.
- If "high level comparator 3 output detection" is selected as the capture trigger (P2CPSL=0), once a high level is detected at the comparator 3 output after the expiration of the comparator 3 detection disabled period, the high level of the comparator 3 output is not subsequently detected until the next synchronization flag occurs (the timing of the beginning of the detection disabled period).

  When P2CPSL is set to 1, the high level of the comparator 3 output can be detected any number of times until the next synchronization flag occurs (the timing of the beginning of the detection disabled period). For details, see Figure 3.10.8, "PPG Output Timing 3," and Figure 3.10.9, "PPG Output Timing 4."

3.10.4.16 Comparator 8 detection disabled period setting register (P2C8DS)

1) This is a 6-bit register that controls the detection disabled period for comparator 8.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FEA0	HH00 0000	R/W	P2C8DS	-	-	P2C8DS5	P2C8DS4	P2C8DS3	P2C8DS2	P2C8DS1	P2C8DS0

P2C8DS5 to P2C8DS0: Comparator 8 detection disabled period setting

- These bits define the detection disabled period for comparator 8 with respect to the PPG output set timing.

  Comparator 8 detection disabled period = (Set value × 4 + 1) × 1/FmMRC

  (FmMRC: Internal high-speed RC oscillator frequency)

- In addition to the above period, the interval from the generation of the synchronization flag (when a comparator 1 falling edge is detected or when a comparator 1 detection timeout occurs) until the setting of the PPG output is included in the detection disabled period.
- When comparator 8 detection disabled period > pulse on-time, the detection disabled period expires at the timing of the PPG output resetting.
- If "high level comparator 8 output detection" is selected as the capture trigger (P2CPSL=1), once a high level is detected at the comparator 8 output after the expiration of the comparator 8 detection disabled period, the high level of the comparator 8 output is not subsequently detected until the next synchronization flag occurs (the timing of the beginning of the detection disabled period).

  When P2CPSL is set to 0, the high level of the comparator 8 output can be detected any number of times until the next synchronization flag occurs (the timing of the beginning of the detection disabled period). For details, see Figure 3.10.8, "PPG Output Timing 5."

Note:

The setting "comparator 8 detection disabled period>comparator 3 detection disabled period" is inhibited.

3.10.5 Options

The following user options are available:

1) Amplifier 1 gain select: 6×/8×/10×
2) PPG output polarity select: No polarity inversion (low level output in the pulse reset state)/ polarity inversion (high level output in the pulse reset state)
3) Comparator 2 reference voltage: 5/12VD／6/12VDD／7/12VDD
4) Comparator 3 reference voltage: 1/6VDD／2/6VDD／3/6VDD／4/6VDD
5) Comparator 7 reference voltage: 6/12VDD／7/12VDD／8/12VDD
6) PPG pulse on-time value limits: 080h/100h/180h/200h/280h/300h/380h/400h/ 480h/500h/580h/600h/680h/700h/780h/7FFh

4. Control Functions

4.1 Interrupt Function

4.1.1 Overview

This series of microcontrollers has the capability to control three levels of multiple interrupts, i.e., low level (L), high level (H), and highest level (X). The master interrupt enable and interrupt priority control registers are used to enable or disable interrupts and to determine the priority of interrupts.

4.1.2 Functions

1) Interrupt processing
   - Peripheral modules generate an interrupt request to the predetermined vector address when the interrupt request and interrupt request enable flags are set to 1.
   - When the microcontroller receives an interrupt request from a peripheral module, it determines the interrupt level, priority and interrupt enable status. If the interrupt request is legitimate for processing, the microcontroller saves the value of PC in the stack and causes a branch to the predetermined vector address.
   - The return from the interrupt routine is accomplished by the RETI instruction, which restores the old state of the PC and interrupt level.

2) Multilevel interrupt control
   - The interrupt function supports three levels of interrupts, that is, the low level (L), high level (H), and highest level (X). The interrupt function will not accept any interrupt request of the same level or lower level than that of the interrupt that is currently being processed.

3) Interrupt priority
   - When interrupt requests to two or more vector addresses occur at the same time, the interrupt request of the highest level takes precedence over the other interrupt requests. When interrupts of the same level occur at the same time, an interrupt with a lower vector address is given priority.

4) Interrupt request enable control
   - The master interrupt enable register can be used to control the enabling/disabling of H- and L-level interrupt requests.
   - Interrupt requests of the X level cannot be disabled.

5) Interrupt disable period
   - Interrupts are held disabled when a write operation is performed to the IE (FE08H) or IP (FE09H) register, or for a period of 2Tcyc after HOLD mode is released.
   - No interrupt can occur during the interval between the execution of an instruction that loads the PCON (FE07H) register and the execution of the next instruction.
   - No interrupt can occur during the interval between the execution of a RETI instruction and the execution of the next instruction.

6) Interrupt level control
   - Interrupt levels can be selected on a vector address basis.

Table of Interrupts

No.	Vector	Level	Interrupt Source
1	00003H	X or L	CMP2/CMP7
2	0000BH	X or L	CMP3/CMP8
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/base timer
5	00023H	H or L	T0H
6	0002BH	H or L	TIL/TIH
7	00033H	H or L	UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7/CMP1TO
10	0004BH	H or L	CMP6/surge detection

   - Priority level: X > H > L
   - When interrupts of the same level occur at the same time, the interrupt with the lowest vector address is processed first.

7) It is necessary to manipulate the following special function registers to enable interrupts and to specify their priority.
   - IE, IP

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE08	0000 HH00	R/W	IE	IE7	XFLG	HFLG	LFLG	-	-	XCNT1	XCNT0
FE09	0000 0000	R/W	IP	IP4B	IP43	IP3B	IP33	IP2B	IP23	IP1B	IP13

4.1.3 Circuit Configuration

4.1.3.1 Master interrupt enable control register (IE) (6-bit register)

1) This register enables and disables H- and L-level interrupts.
2) The state of the interrupt level flag of the register can be read.
3) The register selects the level (L or X) of interrupts to vector addresses 00003H and 0000BH.

4.1.3.2 Interrupt priority control register (IP) (8-bit register)

1) This register selects the level (H or L) of interrupts to vector addresses 00013H to 0004BH.

4.1.4 Related Registers

4.1.4.1 Master interrupt enable control register (IE)

1) This register is a 6-bit register for controlling the interrupts. Bits 6 to 4 are read only.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE08	0000 HH00	R/W	IE	IE7	XFLG	HFLG	LFLG	-	-	XCNT1	XCNT0

IE7 (bit 7): H-/L-level interrupt enable/disable control

A 1 in this bit enables H- and L-level interrupt requests to be accepted.

A 0 in this bit disables H- and L-level interrupt requests to be accepted.

X-level interrupt requests are always enabled regardless of the state of this bit

XFLG (bit 6): X-level interrupt flag (R/O)

This bit is set when an X-level interrupt is accepted and reset when execution returns from the processing of the X-level interrupt.

This bit is read only. No instruction can rewrite the value of this bit directly.

HFLG (bit 5): H-level interrupt flag (R/O)

This bit is set when an H-level interrupt is accepted and reset when execution returns from the processing of the H-level interrupt.

This bit is read only. No instruction can rewrite the value of this bit directly.

LFLG (bit 4): L-level interrupt flag (R/O)

This bit is set when an L-level interrupt is accepted and reset when execution returns from the processing of the L-level interrupt.

This bit is read only. No instruction can rewrite the value of this bit directly.

(Bits 3, 2): These bits do not exist.

They are always read as 1.

XCNT1 (bit 1): 0000BH interrupt level control flag

A 1 in this bit sets all interrupts to vector address 0000BH to the L-level.

A 0 in this bit sets all interrupts to vector address 0000BH to the X-level.

XCNT0 (bit 0): 00003H interrupt level control flag

A 1 in this bit sets all interrupts to vector address 00003H to the L-level.

A 0 in this bit sets all interrupts to vector address 00003H to the X-level.

4.1.4.2 Interrupt priority control register (IP)

1) This register is an 8-bit register that selects the interrupt level (H/L) to vector addresses 00013H to 0004BH.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE09	0000 0000	R/W	IP	IP4B	IP43	IP3B	IP33	IP2B	IP23	IP1B	IP13

	Interrupt Vector Address	IP Bit	Value	Interrupt Level
7	0004BH	IP4B	0	L
			1	H
6	00043H	IP43	0	L
			1	H
5	0003BH	IP3B	0	L
			1	H
4	00033H	IP33	0	L
			1	H
3	0002BH	IP2B	0	L
			1	H
2	00023H	IP23	0	L
			1	H
1	0001BH	IP1B	0	L
			1	H
0	00013H	IP13	0	L
			1	H

4.2 System Clock Generator Function

4.2.1 Overview

This series of microcontrollers incorporates three systems of oscillator circuits, i.e., a low-speed RC oscillator, a medium-speed RC oscillator, and a high-speed RC oscillator circuits as system clock generator circuits. These oscillator circuits have built-in resistors and capacitors, so that no external circuit is required.

The system clock can be selected from these three types of clock sources under program control.

4.2.2 Functions

1) System clock select
   - Allows the system clock to be selected under program control from three types of clocks generated by the low-speed RC oscillator, medium-speed RC oscillator, and high-speed RC oscillator.

2) System clock frequency division
   - Divides frequency of the oscillator clock selected as the system clock and supplies the resultant clock to the system as the system clock.
   - The frequency divider circuit has two stages:

     The first stage allows the selection of division ratios of $\frac{1}{1}$ and $\frac{1}{2}$.

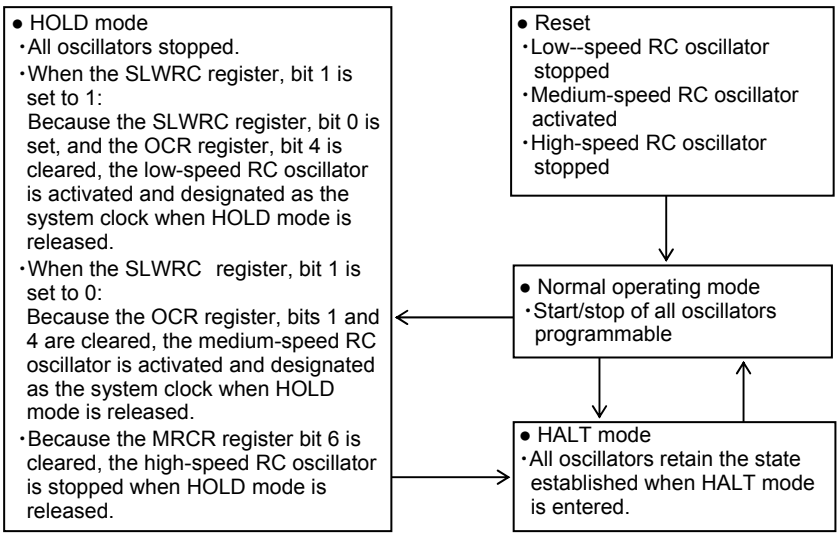
     The second stage allows the selection of division ratios of $\frac{1}{1}$, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$, $\frac{1}{64}$, and $\frac{1}{128}$.

3) Oscillator circuit control
   - Allows the start/stop control of the three systems of oscillators to be executed independently through microcontroller instructions.

4) Oscillator circuit states and operating modes

Mode/Clock	Low-speed RC Oscillator	Medium-speed RC Oscillator	High-speed RC Oscillator	System Clock
Reset	Stopped	Running	Stopped	Medium-speed RC oscillator
Reset released	Stopped	Running	Stopped	Medium-speed RC oscillator
Normal mode	Programmable	Programmable	Programmable	Programmable
HALT	State established at entry time	State established at entry time	State established at entry time	State established at entry time
HOLD	Stopped	Stopped	Stopped	Stopped
Immediately after exit from HOLD mode	Running	Running	Stopped	Low- or medium-speed RC oscillator according to the state that has been defined on entry by bit 1 of the SLWRC register

See Section 4.3," Standby Function," for procedures to enter and exit the microcontroller operating modes.



5) It is necessary to manipulate the following special function registers to control the system clock.
   • PCON, OCR, CLKDIV, MRCR, P1TST, SLWRC

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE07	HHHH HH00	R/W	PCON	-	-	-	-	-	-	PDN	IDLE
FE0C	HHHH H000	R/W	CLKDIV	-	-	-	-	-	CLKDV2	CLKDV1	CLKDV0
FE0D	H0HH HHHH	R/W	MRCR	-	MRCST	-	-	-	-	-	-
FE0E	0HH0 HH0H	R/W	OCR	CLKSGL	-	-	CLKCB4	-	-	RCSTOP	-
FE47	000H HHH0	R/W	P1TST	FIX0	FIX0	FIX0	-	-	-	-	FIX0
FE7C	HHHH HH00	R/W	SLWRC	-	-	-	-	-	-	SLRCSEL	SLRCSTAT

4.2.3 Circuit Configuration

4.2.3.1 Internal low-speed RC oscillator

1) This oscillator oscillates according to the internal resistor and capacitor (at 30 kHz typ).
2) The internal low-speed RC oscillator serves as the system clock to be used for low-power, low-speed operation.

4.2.3.2 Internal medium-speed RC oscillator (conventional RC oscillator)

1) This oscillator oscillates according to the internal resistor and capacitor (at 1 MHz typ).
2) The clock from the medium-speed RC oscillator is designated as the system clock after the reset state is released. After HOLD mode is exited, the clock from the medium- or low-speed RC oscillator that is selected on entry into HOLD mode is designated as the system clock.

4.2.3.3 Internal High-speed RC oscillator circuit

1) This circuit oscillates according to the internal resistor and capacitor (at 24 MHz typ).
2) The 12 MHz clock signal that is obtained by dividing the source clock by 2 is used as the system clock.

4.2.3.4 Power control register (PCON) (2-bit register)

1) This register specifies the operating mode (normal/HALT/HOLD).

4.2.3.5 Oscillation control register (OCR) (3-bit register)

1) This register controls the start/stop operation of the oscillator circuit.
2) This register selects the system clock.
3) The register sets the division ratio of the oscillator clock to be used as the system clock to $\frac{1}{1}$ or $\frac{1}{2}$.

4.2.3.6 Low-speed RC oscillation control register (SLWRC) (2-bit register)

1) This register controls the start/stop operation of the low-/medium-speed RC oscillator circuit.
2) The register switches between the low-speed RC oscillator clock and the medium-speed RC oscillator clock.

4.2.3.7 High-speed RC oscillation control register (MRCR) (6-bit register)

1) This register controls the start/stop operation of the high-speed RC oscillator circuit.

4.2.3.8 System clock divider control register (CLKDIV) (3-bit register)

1) This register controls the operation of the system clock divider circuit. The division ratios of $\frac{1}{1}$, $\frac{1}{2}$, $\frac{1}{4}$, $\frac{1}{8}$, $\frac{1}{16}$, $\frac{1}{32}$, $\frac{1}{64}$, and $\frac{1}{128}$ are available.

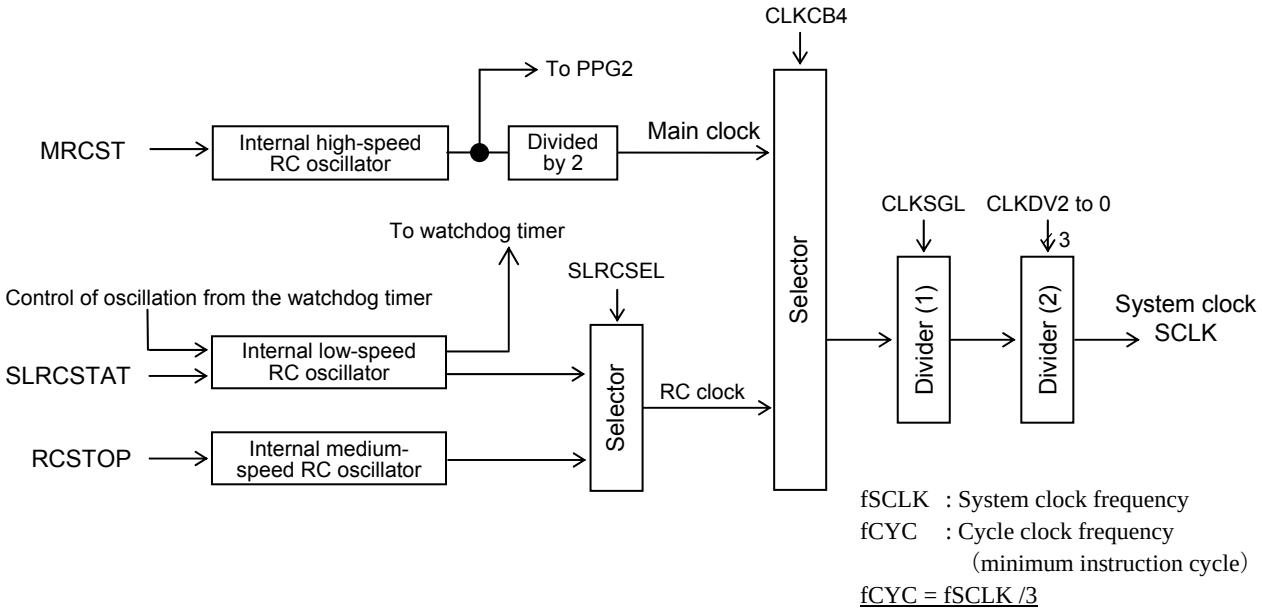


Figure 4.2.1 System Clock Generator Circuit Block Diagram

4.2.4 Related Registers

4.2.4.1 Power control register (PCON) (2-bit register)

1) This register is a 2-bit register used to specify the operating mode (normal/HALT/ HOLD).
   - See Section 4.3, "Standby Function," for the procedures to enter and exit the microcontroller operating modes.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE07	HHHH HH00	R/W	PCON	-	-	-	-	-	-	PDN	IDLE

(Bits 7 to 2): These bits do not exist.

They are always read as 1.

PDN (bit 1): HOLD mode setting flag

PDN	Operating Mode
0	Normal or HALT mode
1	HOLD mode

<1> This bit must be set with an instruction.

- When the microcontroller enters HOLD mode, all oscillators (low-/medium-/high-speed RC oscillators) are suspended and the related registers are placed in the states described below.

  When the SLWRC register, bit 1 is set to 1, the SLWRC register, bit 0 is set and the OCR register, bit 4 is cleared.

  When the SLWRC register, bit 1 is set to 0, the OCR register, bits 1 and 4 are cleared.
- When the microcontroller exits HOLD mode, the low- or medium-speed RC oscillator starts operation and is designated as the system clock source depending on the state of the SLWRC and OCR registers.

<2> PDN is cleared when a HOLD mode release signal (INT2 or INT4) or a reset signal occurs.

<3> Bit 0 is automatically set when PDN is set.

IDLE (bit 0): HALT mode setting flag

<1> Setting this bit places the microcontroller into HALT mode.

<2> This bit is automatically set when bit 1 is set.

<3> This bit is cleared on acceptance of an interrupt request or on receipt of a reset signal.

4.2.4.2 Oscillation control register (OCR) (3-bit register)

1) This register is a 3-bit register that controls the operation of the oscillator circuits and selects the system clock.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0E	0HH0 HH0H	R/W	OCR	CLKSGL	-	-	CLKCB4	-	-	RCSTOP	-

(Bits 6, 5, 3, 2, 0): These bits do not exist.

They are always read as 1.

CLKSGL (bit 7): Clock division ratio select

<1> When this bit is set to 1, the clock selected by bit 4 is used as the system clock as is.

<2> When this bit is set to 0, the clock having a clock rate of $\frac{1}{2}$ of the clock selected by bit 4 is used as the system clock.

CLKCB4 (bit 4): System clock select

<1> CLKCB4 is used to select the system clock.

<2> CLKCB4 is cleared at reset time or when HOLD mode is entered.

CLKCB4	System Clock
0	Internal low-/medium-speed RC oscillator
1	Internal high-speed RC oscillator

RCSTOP (bit 1)): Internal medium-speed RC oscillator circuit control

<1> Setting this bit to 1 stops the oscillation of the internal medium-speed RC oscillator circuit.

<2> Setting this bit to 0 starts the oscillation of the internal medium-speed RC oscillator circuit.

<3> When a reset occurs, this bit is cleared and the oscillator circuit is enabled for oscillation.

<4> When the microcontroller enters HOLD mode, this bit is set as described below according to the state of bit 1 of the SLWRC register.

When the SLWRC register, bit 1 is set to 1, the state of this bit remains unchanged.

When the SLWRC register, bit 1 is set to 0, this bit is cleared and the oscillator starts oscillation and is designated as the system clock source when the microcontroller exits HOLD mode.

4.2.4.3 Low-speed RC oscillation control register (SLWRC) (2-bit register)

1) This register is a 2-bit register that controls the operation of the low-/medium-speed RC oscillator circuits.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7C	HHHH HH00	R/W	SLWRC	-	-	-	-	-	-	SLRCSEL	SLRCSTAT

(Bits 7 to 2): These bits do not exist.

They are always read as 1.

SLRCSEL (bit 1): Internal low-/medium-speed RC oscillator clock select control

<1> A 1 in this bit selects the clock for the internal low-speed RC oscillator.

<2> A 0 in this bit selects the clock for the internal medium-speed RC oscillator.

SLRCSTAT (bit 0): Internal low-speed RC oscillator circuit control

<1> A 1 in this bit starts the internal low-speed RC oscillator circuit.

<2> A 0 in this bit stops the internal low-speed RC oscillator circuit.

<3> This bit is cleared at reset time.

<4> This bit is set as described below according to the state of bit 1 of the SLWRC register when the microcontroller enters HOLD mode.

If the SLWRC register, bit 1 is set to 1, this bit is set and the oscillator starts oscillation and is designated as the system clock source when the microcontroller exits HOLD mode.

If the SLWRC register, bit 1 is set to 0, the state of this bit remains unchanged.

4.2.4.4 High-speed RC oscillation control register (MRCR) (1-bit register)

1) This register is a 1-bit register that controls the operation of the high-speed RC oscillator circuit.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0D	H0HH HHHH	R/W	MRCR	-	MRCST	-	-	-	-	-	-

(Bits 7, 5): These bits do not exist.

They are always read as 1.

MRCST (bit 6): High-speed RC oscillation start control

<1> A 1 in this bit starts the high-sped RC oscillator circuit.

<2> A 0 in this bit stops the high-speed RC oscillator circuit.

<3> This bit is cleared when the microcontroller enters HOLD mode.

Note: When switching the system clock, secure an oscillation stabilization time of 100 µs or longer after the high-speed RC oscillator circuit is switched from the "oscillation stopped" to "oscillation enabled" state.

4.2.4.5 P1TST register (P1TST) (4-bit register)

1) This register is used for testing.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE47	000H HHH0	R/W	P1TST	FIX0	FIX0	FIX0	-	-	-	-	FIX0

FIX0 (bits 7 to 5, 0): These bits are used for testing only.

These bits must always be set to 0.

(Bits 4 to 1): These bits do not exist.

They are always read as 1.

4.2.4.6 System clock divider control register (CLKDIV) (3-bit register)

1) This register controls the frequency division processing of the system clock.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE0C	HHHH H000	R/W	CLKDIV	-	-	-	-	-	CLKDV2	CLKDV1	CLKDV0

(Bits 7 to 3): These bits do not exist.

They are always read as 1.

CLKDV2 (bit 2):
CLKDV1 (bit 1): } **Define the division ratio of the system clock.**
CLKDV0 (bit 0):

CLKDV2	CLKDV1	CLKDV0	Division Ratio
0	0	0	$\frac{1}{1}$
0	0	1	$\frac{1}{2}$
0	1	0	$\frac{1}{4}$
0	1	1	$\frac{1}{8}$
1	0	0	$\frac{1}{16}$
1	0	1	$\frac{1}{32}$
1	1	0	$\frac{1}{64}$
1	1	1	$\frac{1}{128}$

4.3 Standby Function

4.3.1 Overview

This series of microcontrollers supports two standby modes, i.e., HALT and HOLD modes, that are used to reduce current consumption at power-failure time or in program standby mode. In a standby mode, the execution of all instructions is suspended.

4.3.2 Functions

1) HALT mode
   - The microcontroller suspends the execution of instructions but its peripheral circuits continue processing. (Some serial transfer functions are suspended.)
   - HALT mode is entered by setting bit 0 of the PCON register to 1.
   - Bit 0 of the PCON register is cleared and the microcontroller returns to the normal operating mode when a reset occurs or an interrupt request is accepted.

2) HOLD mode
   - All oscillations are suspended. The microcontroller suspends the execution of instructions and its peripheral circuits stop processing.
   - HOLD mode is entered by setting bit 1 of the PCON register to 1 when bit 2 is set to 0. In this case, bit 0 of the PCON register (HALT mode setting flag) is automatically set.
   - When a reset signal or a HOLD mode release signal (INT2 or INT4) occurs, bit 1 of the PCON register is cleared and the microcontroller switches into HALT mode.

Note: Do not allow the microcontroller to enter HALT or HOLD mode while AD conversion is in progress. Make sure that ADSTART is set to 0 before placing the microcontroller into one of the above-mentioned standby modes.

4.3.3 Related Register

4.3.3.1 Power control register (PCON) (2-bit register)

1) This register is a 2-bit register that specifies the operating mode (normal/HALT/HOLD/).

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE07	HHHH HH00	R/W	PCON	-	-	-	-	-	-	PDN	IDLE

(Bits 7 to 2): These bits do not exist.

They are always read as 1.

PDN (bit 1): HOLD mode setting flag

PDN	Operating Mode
0	Normal or HALT mode
1	HOLD mode

<1> This bit must be set with an instruction.

- When the microcontroller enters HOLD mode, all oscillators (low-/medium/high-speed RC) are suspended and the related registers are set as described below.

  When the SLWRC register, bit 1 is set to 1, the SLWRC register, bit 0 is set and the OCR register, bit 4 is cleared.

  When SLWRC register, bit 1 is set to 0, the OCR register bits 1and 4 are cleared.
- When the microcontroller exits HOLD mode, low- or medium-speed RC oscillator resumes oscillation and is designated as the system clock source according to the state of the SLWRC and OCR registers.

<2> PDN is cleared when a HOLD mode release signal (INT2 or INT4) or a reset signal occurs.

<3> Bit 0 is automatically set when PDN is set.

IDLE (bit 0): HALT mode setting flag

<1> Setting this bit places the microcontroller into HALT mode.

<2> When bit 1 is set, this bit is automatically set.

<3> This bit is cleared on acceptance of an interrupt request or on receipt of a reset signal.

Table 4.3.1 Standby Mode Operations

Item/Mode	Reset State	HALT Mode	HOLD Mode
Entry conditions	• $\overline{\text{RES}}$ applied • Reset from watchdog timer	PCON register Bit 1=0 Bit 0=1	PCON register Bit 1=1
Data changed on entry	Initialized as shown in separate table.	• WDTCNT, bit 5 is cleared if the WDTCNT register (FE79), bits 4/3 are set to 0/1.	• WDT, bits 2 to 0 are cleared if the WDT register (FE0F), bit 4 is set. • PCON, bit 0 turns to 1. • If the SLWRC register (FE7C), bit 1 is reset, the OCR register (FE0E), bits 4 and 1 are cleared. • If the SLWRC register (FE7C), bit 1 is set, the SLWRC register (FE7C), bit 0 is set and the OCR register (FE0E), bit 4 is cleared.
Internal low-speed RC oscillation	Stopped	State established at entry time	Stopped
Internal medium-speed RC oscillation	Running	State established at entry time	Stopped
Internal high-speed RC oscillation	Stopped	State established at entry time	Stopped
CPU	Initialized	Stopped	Stopped
I/O pin state	See Table 4.3.2.	←	←
RAM	• $\overline{\text{RES}}$: Undefined • When watchdog timer reset: Data retained	Data retained	Data retained
Base timer	Stopped	State established at entry time	Stopped
PPG2	Stopped	Stopped (Note 3)	Stopped (Note 3)
Peripheral modules except base timer and PPG2	Stopped	State established at entry time (Note 2)	Stopped
Exit conditions	Entry conditions cancelled.	• Interrupt request accepted. • Reset/entry conditions established	• Interrupt request from INT2 or INT4 • Reset/entry conditions established
Returned mode	Normal mode	Normal mode (Note1)	HALT (Note1)
Data changed on exit	None	PCON register, bit 0＝0	PCON register, bit 1＝0

Note 1: The microcontroller switches into the reset state if it exits the current mode on the establishment of reset/entry conditions.

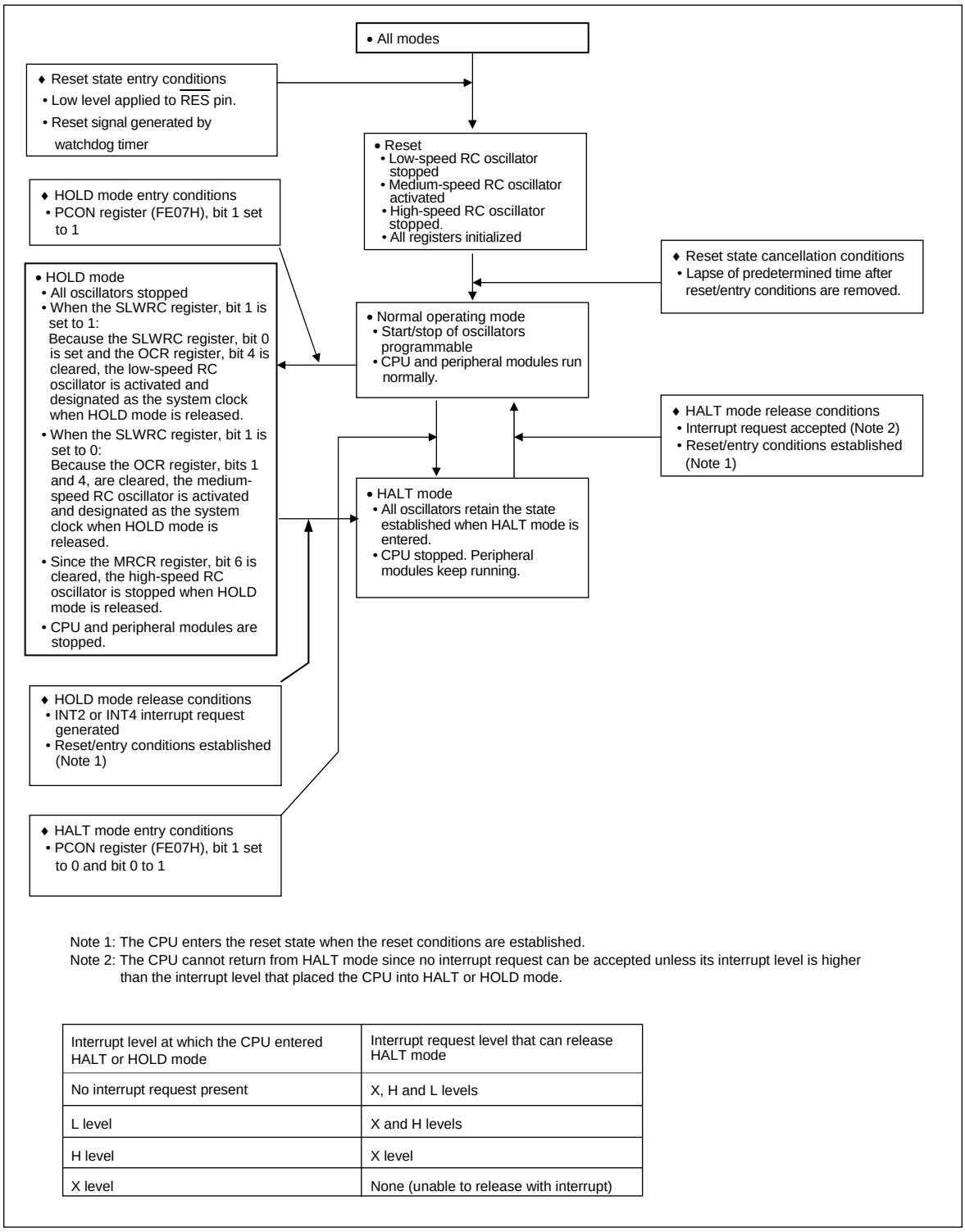
Note 2: Some serial transfer functions are suspended.

Note 3: P2CR1(FE90) must be manipulated to stop operation before placing the microcontroller into the standby state.

Standby

Table 4.3.2 Pin States and Operating Modes (LC870K00 series)

Pin	Reset Time	Normal Mode	HALT Mode	HOLD Mode	On Exit from HOLD Mode
$\overline{\text{RES}}$	• Input	←	←	←	←
P00-P07	• Input mode • Pull-up resistor off	• Input/output/pull-up resistor controlled by a program	←	←	←
P30	• Input mode • Pull-up resistor off	• Input/output/pull-up resistor controlled by a program	←	←	←



Note 1: The CPU enters the reset state when the reset conditions are established.
Note 2: The CPU cannot return from HALT mode since no interrupt request can be accepted unless its interrupt level is higher than the interrupt level that placed the CPU into HALT or HOLD mode.

Interrupt level at which the CPU entered HALT or HOLD mode	Interrupt request level that can release HALT mode
No interrupt request present	X, H and L levels
L level	X and H levels
H level	X level
X level	None (unable to release with interrupt)

Figure 4.3.1 Standby Mode State Transition Diagram

4.4 Reset Function

4.4.1 Overview

The reset function initializes the microcontroller when it is powered on or while it is running.

4.4.2 Functions

This series of microcontrollers provides the following three types of reset function:

1) External reset via the $\overline{\text{RES}}$ pin

   The microcontroller is reset without fail by applying and holding a low level to the $\overline{\text{RES}}$ pin for 200 μs or longer. Note, however, that a low level of a small duration (less than 200 μs) is likely to trigger a reset.

   The $\overline{\text{RES}}$ pin can serve as a power-on reset pin when it is provided with a proper external time constant element.

2) Internal reset

   The internal reset function is available in two types: the power-on reset (POR) that triggers a reset when power is turned on and the low-voltage detection reset (LVD) that triggers a reset when the power voltage falls below a certain level. Options are available to set the power-on reset resetting level, to enable and disable the low-voltage detection reset function, and to set its threshold level.

3) Reset function using a watchdog timer

   The watchdog timer of this series of microcontroller can be used to generate reset, by the internal low-speed RC oscillator, at a predetermined time interval.

   An example of a resetting circuit is shown in Figure 4.4.1. The external circuit connected to the reset pin shows an example that the internal reset function is disabled and an external power-on reset circuit is configured.

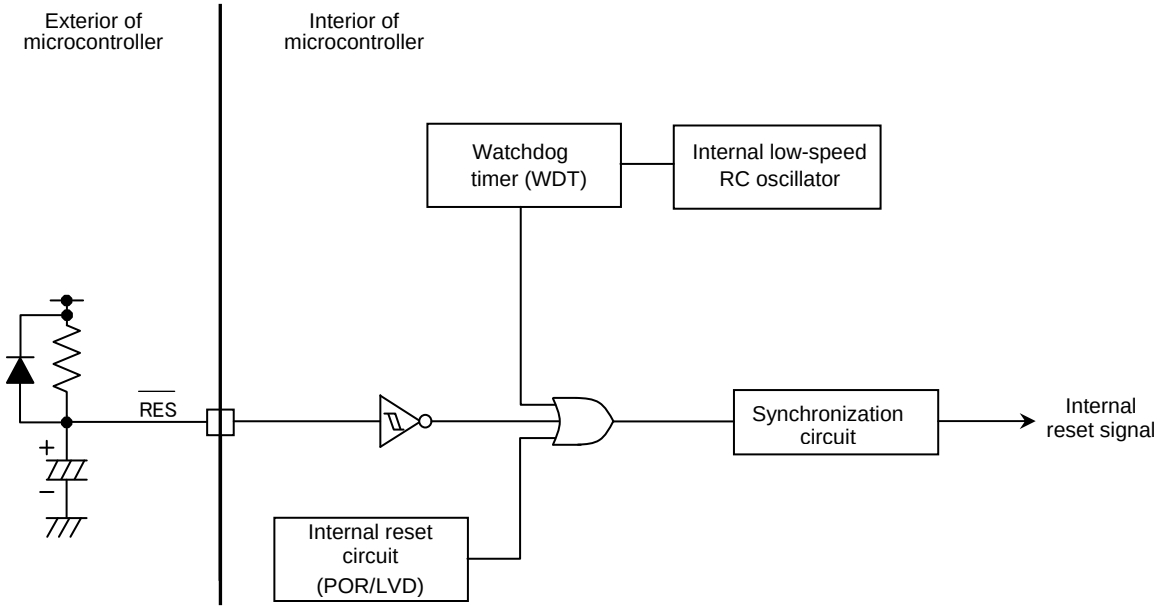


Figure 4.4.1 Sample Reset Circuit Block Diagram

4.4.3 Reset State

When a reset is generated by the $\overline{\text{RES}}$ pin, internal reset circuit, or watchdog timer, the hardware functional blocks of the microcontroller are initialized by a reset signal that is in synchronization with the system clock.

Because the system clock is switched to the internal medium-speed RC oscillator when a reset occurs, hardware initialization is also carried out immediately even at power-on time. The system clock is switched to the main clock when the oscillation stabilization time of the main clock is secured. The program counter is initialized to 0000H on a reset. See Appendix (A-I), Special Function Register (SFR) Map, for the initial values of the special function registers (SFR).

<Notes and precautions>

- *The stack pointer is initialized to 0000H.*
- *Data RAM is never initialized by a reset. Consequently, the contents of RAM are undefined at power-on time.*
- *When using the internal reset function, it is necessary to implement and connect an external circuit to the reset pin according the user's operating environment. Be sure to review and observe the operating specifications, circuit configuration, precautions, and considerations discussed in Section 4.6 "Internal Reset Function."*

4.5 Watchdog Timer (WDT)

4.5.1 Overview

This series of microcontrollers is provided with a watchdog timer (WDT) that has the following functions:

1) Capable of generating an internal reset on an overflow of a timer that runs on an internal low-speed RC oscillator clock.
2) Watchdog timer operation in standby mode can be selected from three modes (continue count operation, suspend operation, and suspend count operation while retaining the count value).

4.5.2 Functions

1) Watchdog timer function
   - The 17-bit up-counter (WDTCT) runs on a low-speed RC oscillator clock. A WDT reset (internal reset signal) is generated when the overflow time (selected from 8 time values) that is selected by the watchdog timer control register (WDTCNT) is reached. At this time, the reset detection flag (RSTFLG) is set.

     Because the WDTCT can be cleared by a program, it is necessary to code the program so that the WDTCT can be cleared at regular intervals.
   - The internal low-speed RC oscillator is controlled by the low-speed RC oscillation control register (SLWRC) and the WDT. Since the oscillator is controlled independently of the system, the WDT continues operation even when the system clock is stopped due to a program runaway, making it possible to detect system runaway conditions.
   - The WDT operation mode on entry into standby mode can be selected from three modes, i.e., "continue count operation," "suspend operation," and " suspend count operation while retaining the count value." If "continue count operation" is selected, an operating current of several μA is always flowing in the IC because the low-speed RC oscillator circuit continues oscillation even in standby mode. (For details, refer to the latest "SANYO Semiconductors Data Sheet.")

2) It is necessary to manipulate the following special function register to control the watchdog timer (WDT).
   - WDTCNT

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE79	0000 0000	R/W	WDTCNT	RSTFLG	FIX0	WDTRUN	IDLOP1	IDLOP0	WDTSL2	WDTSL1	WDTSL0

4.5.3 Circuit Configuration

4.5.3.1 WDT control register (WDTCNT) (8-bit register)

1) This register is used to manipulate the reset detection flag, to select operation in standby mode, to select the overflow time, and to control the operation of the WDT.

Note: The WDTCNT is initialized to 00H when a low-level signal is applied to the external $\overline{RES}$ pin or a reset is triggered by the internal reset (POR/LVD) function. Bits 4 to 0 of the WDTCNT, however, are not initialized, when a WDT-triggered reset occurs.

*Note: The WDTCNT is disabled for writes once the WDT is started (WDTRUN set to 1). If the instruction **MOV #55H, WDTCNT** is executed in this case, the WDTCT is cleared and counting is restarted at a count value of 0. (The WDTCT is not cleared when it is loaded with 55H with any other instruction.)*

Note: The low-speed RC oscillator circuit starts oscillation by setting the WDTRUN (WDTCNT, bit 5) to 1. Once oscillation is started, an operating current of several μA flows at all times (For details, refer to the latest "SANYO Semiconductors Data Sheet"). Note that oscillation is also started when SLRCSTAT (SLWRC, bit 0) is set to 1.

4.5.3.2 WDT counter (WDTCT) (17-bit counter)

1) Start/stop: Stop/start is controlled by the 0/1 value of WDTRUN. When WDTRUN is set to 1 and IDLOP1 and IDLOP0 (WDTCNT, bits 4 and 3) are set to 2, the microcontroller enters standby mode.

2) Count clock: The low-speed RC oscillator clock

3) Overflow: Generated when the WDTCT count value matches the count value selected by WDTSL2 to WDTSL0 (WDTCNT, bits 2 to 0).

* Generates the WDT reset and the WDTRUN clear signals and WDTRSTF (WDTRUN, bit 7) set signal.

4) Reset: When WDTRUN is set to 0, or WDTRUN is set to 1 and instruction **MOV #55H, WDTCNT** is executed.

* See Figure 4.5.2 for details on WDT operation.

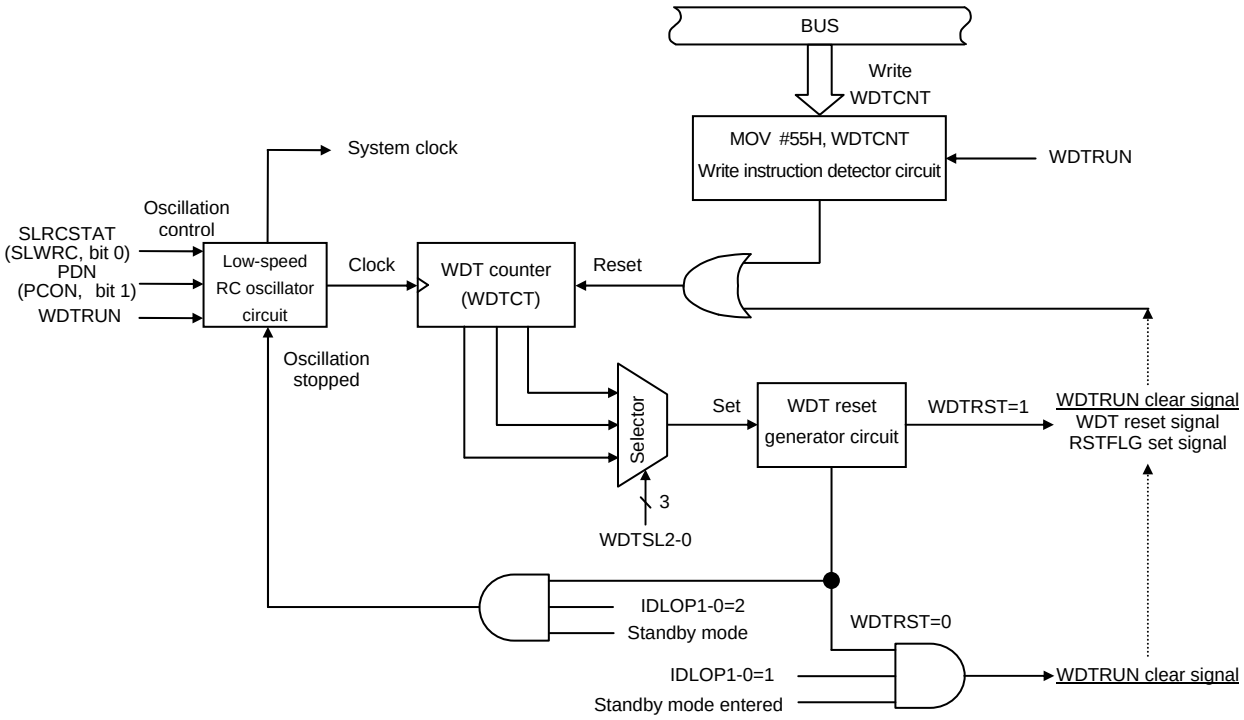


Figure 4.5.1 Watchdog Timer Operation Block Diagram

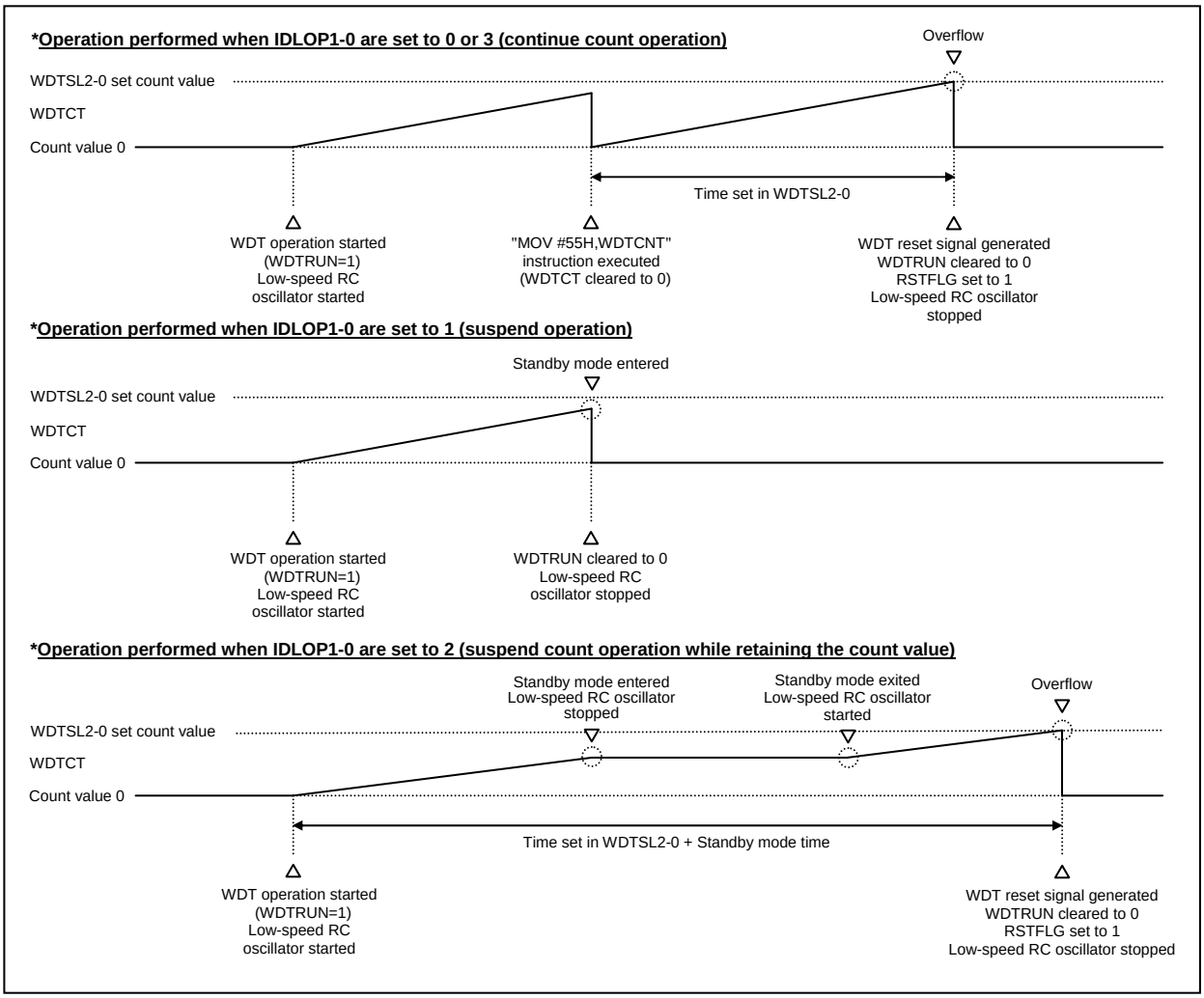


Figure 4.5.2 Sample Watchdog Timer Operation Waveforms

4.5.4 Related Register

4.5.4.1 WDT control register (WDTCNT)

1) This register is used to manipulate the reset detection flag, to select the standby mode operation, to select the overflow time, and to control the operation of the WDT.

Address	Initial Value	R/W	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE79	0000 0000	R/W	WDTCNT	RSTFLG	FIX0	WDTRUN	IDLOP1	IDLOP0	WDTSL2	WDTSL1	WDTSL0

RSTFLG (bit 7): WDT reset detection flag

This bit is cleared when a reset is triggered by applying a low level signal to the external $\overline{\text{RES}}$ pin or by using the internal reset (POR/LVD) function.

This bit is set when a WDT-triggered reset occurs.

This flag can be rewritten with an instruction.

FIX0 (bit 6): Test bit

This bit is used for test purposes. It must always be set to 0.

WDTRUN (bit 5): WDT operation control

Setting this bit to 0 stops the WDT operation.

Setting this bit to 1 starts the WDT operation.

IDLOP1 (bit 4):
IDLOP0 (bit 3): } **WDT standby mode operation select**

IDLOP1	IDLOP0	WDT Standby Mode Operation
0	0	Continue count operation
0	1	Suspend operation
1	0	Suspend count operation while retaining the count value
1	1	Continue count operation

* See Figure 4.5.2 for details of WDT operating modes.

WDTSL2 (bit 2):
WDTSL1 (bit 1): } **Overflow time select**
WDTSL0 (bit 0):

WDTSL2	WDTSL1	WDTSL0	WDTCT Setting Count Number and Overflow Generation Time Example	
			Count Number	Low-speed RC Clock
0	0	0	1024	34.1ms
0	0	1	2048	68.3ms
0	1	0	4096	137ms
0	1	1	8192	273ms
1	0	0	16384	546ms
1	0	1	32768	1.09s
1	1	0	65536	2.18s
1	1	1	131072	4.37s

* Time values in the “Low-speed RC Clock” column of the table refer to the time for a WDTCT overflow to occur when the low-speed RC oscillation frequency is 30 kHz (typical). The low-speed RC oscillation frequency varies from IC to IC. For details, refer to the latest "SANYO Semiconductors Data Sheet."

Note: The WDTCNT is initialized to 00H when a low-level signal is applied to the external $\overline{RES}$ pin or a reset is triggered by the internal reset (POR/LVD) function. Bits 4 to 0 of the WDTCNT are not initialized, however, when a WDT-triggered reset occurs.

*Note: The WDTCNT is disabled for writes once the WDT starts operation (WDTRUN set to 1). If the instruction **MOV #55H, WDTCNT** is executed in this case, WDTCT is cleared and counting is restarted at a count value of 0 (The WDTCT is not cleared when it is loaded with 55H with any other instruction).*

Note: The low-speed RC oscillator circuit is started by setting WDTRUN to 1. Once the oscillator starts oscillation, an operating current of several μA flows at all times (For details, refer to the latest "SANYO Semiconductors Data Sheet"). Note that oscillation is also started when SLRCSTAT (SLWRC, bit 0) is set to 1.

4.5.5 Using the Watchdog Timer

Code a program so that instructions for clearing the watchdog timer periodically are executed.

1) Starting the watchdog timer

<1> Set the time for a WDT reset to occur to WDTSL2 to WDTSL0 (WDTCNT, bits 2 to 0).

<2> Set the WDT standby mode operation (HALT/HOLD) to IDLOP1 and IDLOP0 (WDTCNT, bits 4 and 3).

<3> After <1> and <2>, load WDTRUN (WDTCNT, bit 5) with 1.

The watchdog timer starts functioning when WDTRUN is set to 1. Once the watchdog timer starts operation, WDTCNT is disabled for write; it is only possible to clear WDTCT and read WDTCNT. Consequently, the watchdog timer can never be stopped with an instruction. The function of the watchdog timer is stopped only when a low level signal is applied to the external $\overline{\text{RES}}$ pin, a reset by the internal reset function (POR/LVD) occurs, or standby mode is entered when IDLOP1 and IDLOP0 are set to 1. In this case, WDTRUN is cleared.

2) Clearing the WDTCT

When the watchdog timer starts operation, WDTCT counts up. When this WDTCT overflows, a WDT reset occurs. To run the program in normal mode, it is necessary to periodically clear WDTCT before WDTCT overflows. Execute the following instruction to clear WDTCT while it is running:

MOV #55H, WDTCNT

3) Detecting a runaway condition

Unless the above-mentioned instruction is executed periodically, WDTCT overflows because the watchdog timer is not cleared. If an overflow occurs, the watchdog timer considers that a program runaway has occurred and triggers a WDT reset. In this case, WDTRSTF (WDTCNT, bit 7) is set. After a WDT reset occurs, the program execution restarts at address 0000H. (In the flash ROM version, the program execution restarts at the address selected as an option.)

4.5.6 Notes on the Use of the Watchdog Timer

- SLRCSTAT (SLWRC, bit 0) must be set to 0 when the internal low-speed RC oscillator clock is not to be used as the system clock (The start/stop of the internal low-speed RC oscillator is also controlled by the watchdog timer). When SLRCSTAT (SLWRC, bit 0) is set to 1, the internal low-speed RC oscillator continues oscillation in HALT mode even when the watchdog timer is running controlled by setting IDLOP1 to IDLOP0 to 1 or 2.
- To realize ultra-low-power operation using HOLD mode, it is necessary to disable the watchdog timer from running in HOLD mode by setting IDLOP1 and IDLOP0 to 1 or 2. When setting IDLOP1 and IDLOP0 to 0 or 3, several μA of operating current flows at all times because the internal low-speed RC oscillator circuit continues oscillating even in HOLD mode.
- If standby mode (HALT/HOLD) is entered when the watchdog timer is running with IDLOP1 and IDLOP0 set to 2, the low-speed RC oscillator circuit stops oscillation and the watchdog timer stops counting and retains the count value. When the microcontroller subsequently exits standby mode, the low-speed RC oscillator circuit resumes oscillation and the watchdog timer starts count operation. If the period between release from standby mode and next entry into a standby mode is **less than "low-speed RC oscillator clock × 4,** however, the low-speed RC oscillator circuit may not stop oscillation even when the CPU enters standby mode. In such a case (the standby mode is on), several μA of operating current flows because the low-speed RC oscillator circuit is active though the watchdog timer count operation is suspended.

  To minimize the standby power requirement of the set, code the program so that an interval of **"low-speed RC oscillator clock × 4" or longer** is provided between release from standby mode and entry into the next standby mode. (Note that the oscillation frequency of the low-speed RC oscillator may fluctuate. See the latest "SANYO Semiconductors Data Sheet" for details.)

4.6 Internal Reset Function

4.6.1 Overview

This series of microcontrollers incorporates internal reset functions called the power-on reset (POR) and low voltage detection reset (LVD). The use of these functions contributes to a reduction in the number of externally required reset circuit components (reset IC, etc.).

4.6.2 Functions

1) Power-on reset (POR) function

   POR is a hardware feature that generates a reset to the microcontroller when the power is turned on. This function allows the user to select the POR release level by option only when the disuse of the low voltage detection reset function is selected. It is necessary to use the below-mentioned low voltage detection reset function together with this function, or configure an external reset circuit if there is possibility that that chatter or a momentary power loss may occur when power is turned on.

2) Low voltage detection reset (LVD) function

   This function, when used together with the POR function, can generate a reset when power is turned on and when the power level lowers. As a user option the use or non-use and the detection levels of this function can be specified.

4.6.3 Circuit Configuration

The internal reset circuit consists of the POR, LVD, pulse stretcher circuit, capacitor C_{RES} discharging transistor, external capacitor C_{RES} + pull-up resistor R_{RES} or pull-up resistor R_{RES} alone. The circuit diagram is provided in Figure 4.6.1.

- Pulse stretcher circuit
  This circuit stretches the POR and LVD reset signals. It is used to stretch the internal reset period and discharge the external capacitor C_{RES} connected to the reset pin. The stretching time last from 30μs to 100μs.
- Capacitor C_{RES} discharging transistor
  This is an N-channel transistor used to discharge the external capacitor C_{RES} connected to the reset pin. If the capacitor C_{RES} is not to be connected to the reset pin, it is possible to monitor the internal reset signal by connecting only the external pull-up resistor R_{RES}.
- Option selector circuit
  The option selector circuit is used to configure the LVD options. This circuit selects whether to enable or disable the LVD and selects its detection levels. See Subsection 4.6.4.
- External capacitor C_{RES} + pull-up resistor R_{RES}
  After the reset signal from the internal reset circuit is released, the reset period is further stretched according to the external CR time constant. This enables the microcontroller to avoid repetitive entries and releases of the reset state from occurring when power-on chatter occurs. The circuit configuration shown in Figure 4.6.1, in which the capacitor C_{RES} and pull-up resistor R_{RES} are externally connected, is recommended when both POR and LVD functions are to be used. The recommended constant values are: C_{RES} = 0.022μF and R_{RES} = 510 kΩ. The external pull-up resistor R_{RES} must always be installed even when the set's specifications inhibit the installation of the external capacitor C_{RES}.

Internal Reset

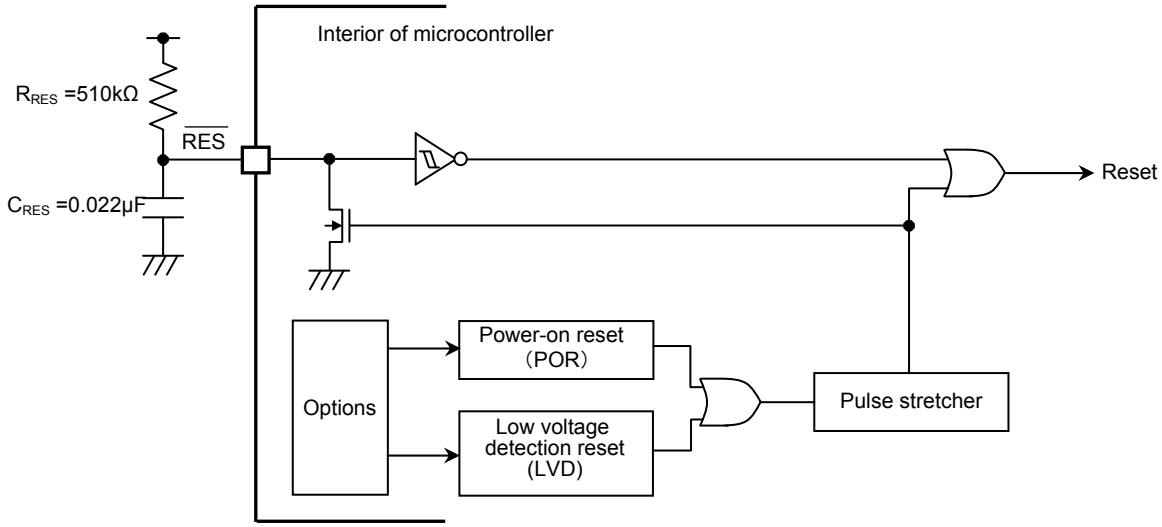


Figure 4.6.1 Internal Reset Circuit Configuration

4.6.4 Options

The POR and LVD options are available for the reset circuit.

1) LVD Reset Function Options			
"Enable": Use		"Disable": Non-use	
2) LVD Reset Level Option		3) POR Release Level Option	
Typical Value of Selected Option	Min. Operating VDD Value (*)	Typical Value of Selected Option	Min. Operating VDD Value (*)
"2.31V"	2.5V –	"2.37V"	2.5V –
"2.51V"	2.7V –	"2.57V"	2.7V –
"2.81V"	3.0V –	"2.87V"	3.0V –
"3.79V"	4.0V –	"3.86V"	4.0V –
"4.28V"	4.5V –	"4.35V"	4.5V –

* The minimum operating VDD value specifies the approximate lower limit of the VDD value beyond which the selected POR release level or LVD reset level cannot be effected without generating a reset.

1) LVD reset function option

When “Enable” is selected, a reset is generated at the voltage that is selected by the LVD reset level option.

Note 1: In this configuration, an operating current of several μA always flows in all modes.

No LVD reset is generated when "Disable" is selected.

Note 2: In this configuration, no operating current will flow in all modes.

* See the sample operating waveforms of the reset circuit shown in Subsection 4.6.5 for details.

2) LVD reset level option

The LVD reset level can be selected from 5 levels only when “Enable” is selected. Select the appropriate detection level according to the user's operating conditions.

3) POR release level option

The POR release level can be selected from 5 levels only when “Disable” is selected. When not using the internal reset circuit, set the POR release level to the lowest level (2.37V) that will not affect the minimum guaranteed operating voltage.

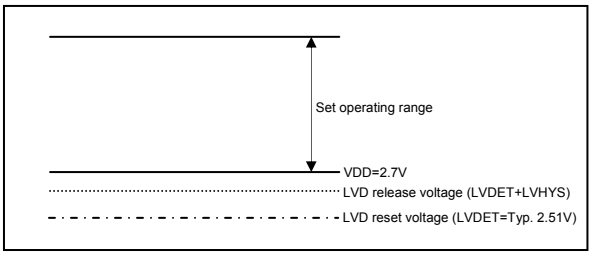
Note 3: No operating current flows when the POR reset state is released.

Note 4: See the notes in paragraph 2) of Subsection 4.6.6 when selecting a POR release level that is lower than the minimum guaranteed operating voltage (2.37V).

- **Selection example 1**

Selecting the optimum LVD reset level to keep the microcontroller running without resetting it until VDD falls below 2.7V according to the set's requirements

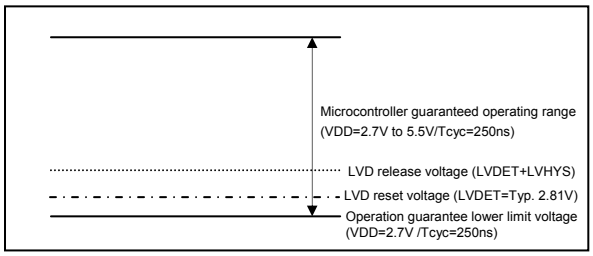
Set the LVD reset function option to "Enable" and select "2.51V" as the LVD reset level.



- **Selection example 2**

Selecting the optimum LVD reset level that meets the guaranteed operating conditions of VDD = 2.7V/Tcyc = 250 ns

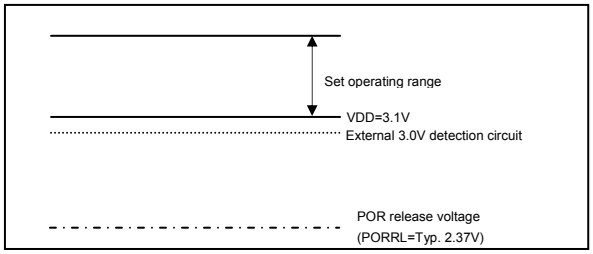
Set the LVD reset function option to "Enable" and select "2.81V" as the LVD reset level option.



- **Selection example 3**

Disabling the internal reset circuit and using an external reset IC that can detect and react at 3.0V (see also paragraph 1) of Subsection 4.6.7)

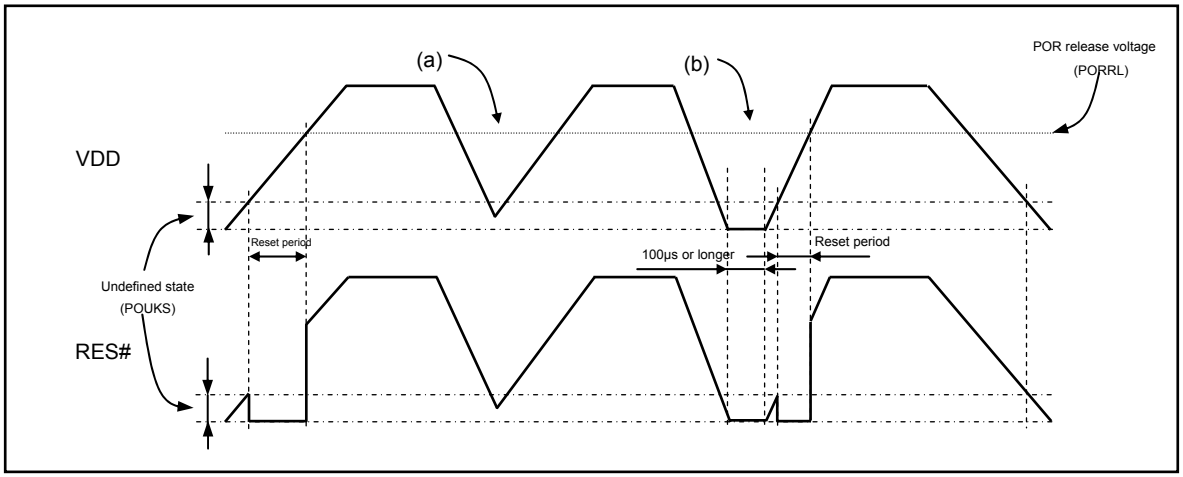
Set the LVD reset function option to "Disable" and select "2.37V" as the POR release level option.



Note 5: The operation guarantee values (voltage/operating frequency) shown in the examples vary with the microcontroller type. Be sure to refer to the latest "SANYO Semiconductors Data Sheet" and select the proper setting level .

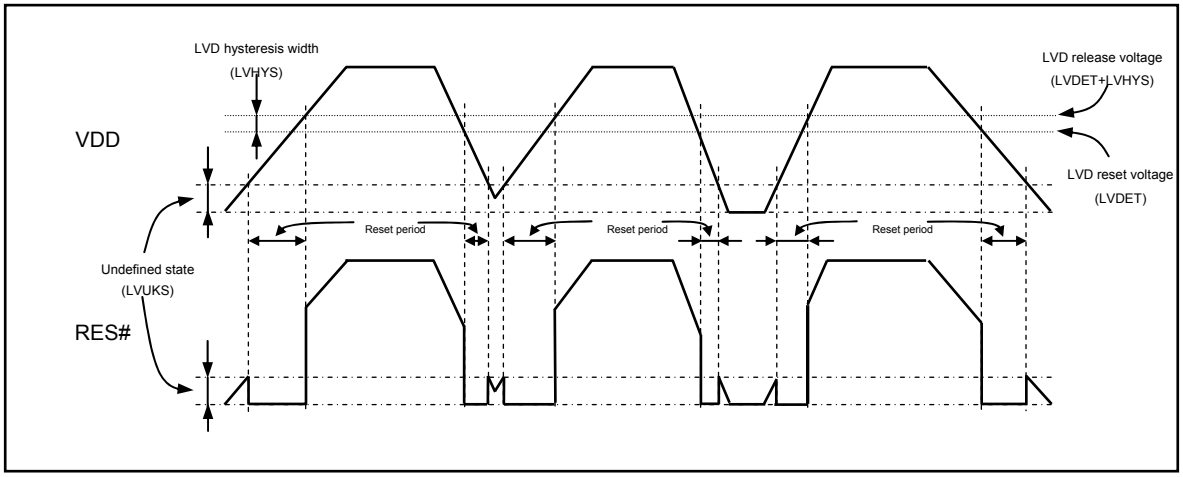
4.6.5 Sample Operating Waveforms of the Internal Reset Circuit

1) Waveform observed when only POR is used (LVD not used)
(Reset pin: Pull-up resistor R_{RES} only)



- There exists an undefined state (POUKS), before the POR transistor starts functioning normally.
- The POR function generates a reset only when the power is turned on starting at the VSS level. The reset release voltage in this case may have some range. Refer to the latest "SANYO Semiconductors Data Sheet" for details.
- No stable reset will be generated if power is turned on again if the power level does not go down to the VSS level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function as explained in 2) or implement an external reset circuit.
- A reset is generated only when the power level goes down to the VSS level as shown in (b) and power is turned on again after this condition continues for 100 µs or longer.

2) Waveform observed when both POR and LVD functions are used
(Reset pin: Pull-up resistor R_{RES} only)



- There also exists an undefined state (LVUKS), before the POR transistor starts functioning normally when both POR and LVD functions are used.
- A reset is generated both when power is turned on and when the power level lowers. The reset release voltage and entry voltage in this case may have some range. Refer to the latest "SANYO Semiconductors Data Sheet" for details.
- A hysteresis width (LVHYS) is provided to prevent repetitions of reset release and entry cycles near the detection level.

4.6.6 Notes on the Use of the Internal Reset Circuit

1) When generating a reset only with the internal POR function

When generating a reset using only the POR function, do not short the reset pin directly to VDD as when using it with the LVD function. Be sure to use an external capacitor C_{RES} of an appropriate capacitance and a pull-up resistor R_{RES} or the pull-up resistor R_{RES} alone. Test the circuit extensively under the anticipated power supply conditions to verify that a reset is reliably generated.

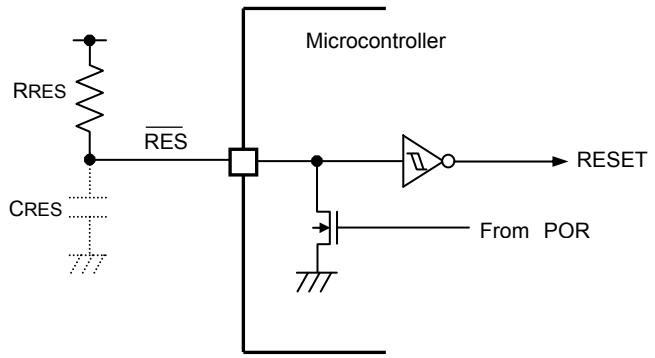


Figure 4.6.2 Reset Circuit Configuration Using only the Internal POR Function

2) When selecting a release voltage level of 2.37V only with the internal POR function

When selecting an internal POR release level of 2.37V, connect the external capacitor C_{RES} and pull-up resistor R_{RES} of the values that match the power supply rise time to the reset pin and make necessary adjustments so that the reset state is released after the release voltage exceeds the minimum guaranteed operating voltage. Alternatively, set and hold the voltage level of the reset pin at the low level until the release voltage exceeds the minimum guaranteed operating voltage.

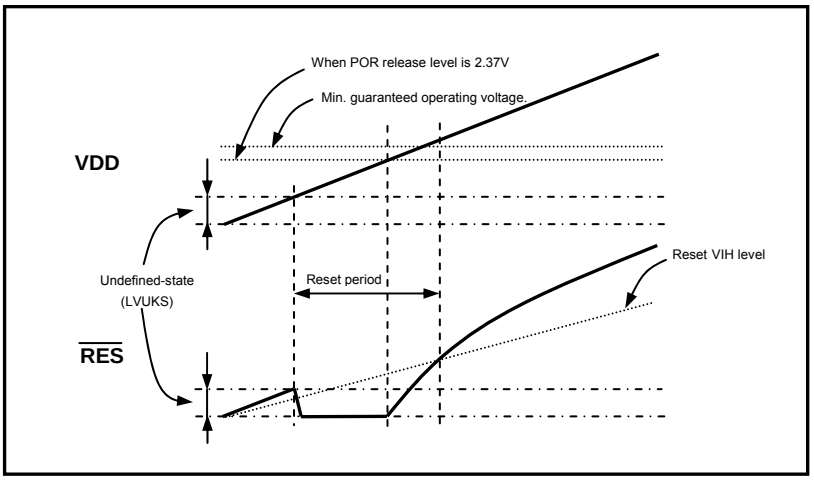


Figure 4.6.3 Sample Release Level Waveform in Internal POR Only Configuration

3) When momentary power loss or voltage fluctuations shorter than several hundred μs are anticipated

The response time measured from the time the LVD detects a power voltage drop at the option-selected level until it generates a reset signal is defined as the minimum low-voltage detection width T_{LVDW} shown in Figure 4.6.4 (see "SANYO Semiconductors Data Sheet"). If momentary power loss or power voltage fluctuations shorter than this minimum low-voltage detection width are anticipated, be sure to take the preventive measures shown in Figure 4.6.5 or other necessary measures.

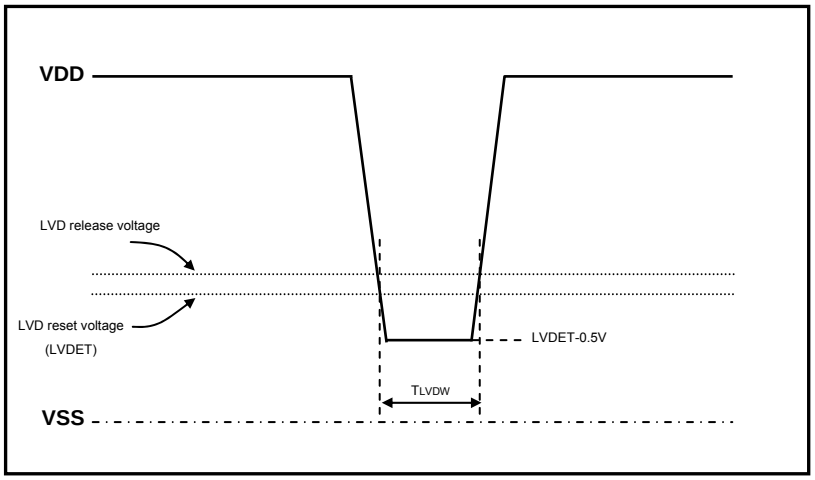


Figure 4.6.4 Example of Momentary Power Loss or Voltage Fluctuation Waveform

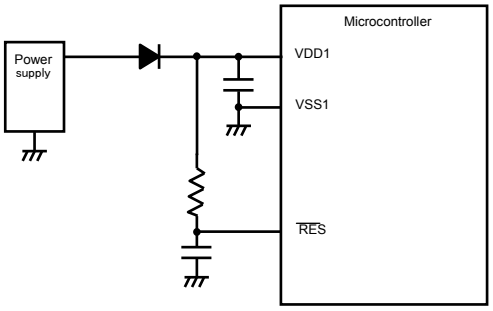


Figure 4.6.5 Example of Momentary Power Loss/Voltage Fluctuation Countermeasures

4.6.7 Notes to be Taken When Not Using the Internal Reset Circuit

1) When configuring an external reset IC without using the internal reset circuit

The POR function is activated and the capacitor C_{RES} discharging N-channel transistor connected to the reset pin turns on when power is turned on even if the internal reset circuit is not used. For this reason, when connecting an external reset IC, adopt a reset IC of a type whose detection level is not lower than the minimum guaranteed operating voltage level, and select the lowest POR release level (1.67V) that does not affect the minimum guaranteed operating voltage. The figures provided below show sample reset circuit configurations that use reset ICs of N-channel open drain and CMOS types, respectively.

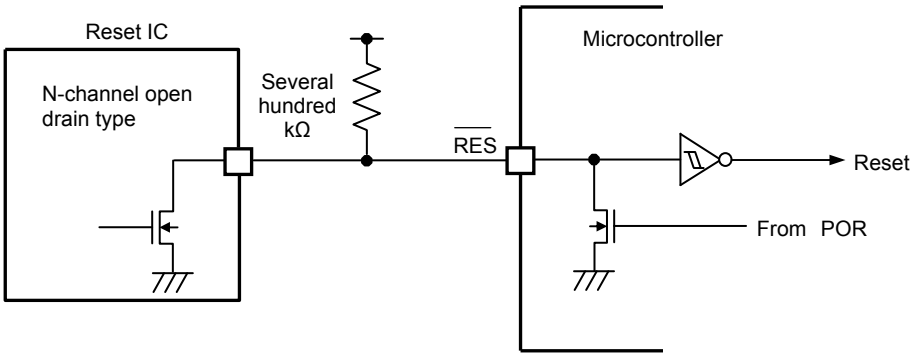


Figure 4.6.6 Sample Reset Circuit Configuration Using an N-channel Open Drain Type Reset IC

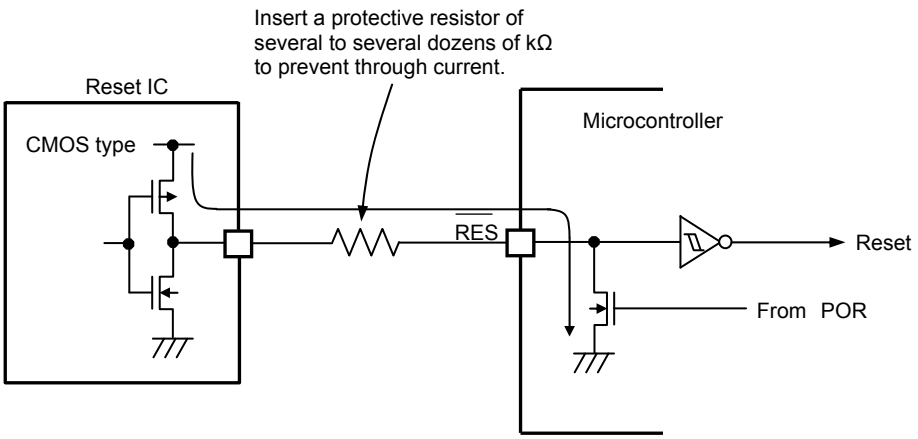


Figure 4.6.7 Sample Reset Circuit Configuration Using a CMOS Type Reset IC

2) When configuring the external POR circuit without using the internal reset circuit

The internal POR is active when power is turned on even if the internal reset circuit is not used as in case 1) in Subsection 4.6.7. When configuring an external POR circuit with a C_{RES} value of 0.1µF or larger to obtain a longer reset period than with the internal POR, however, be sure to connect an external diode D_{RES} as shown in Figure 4.6.8.

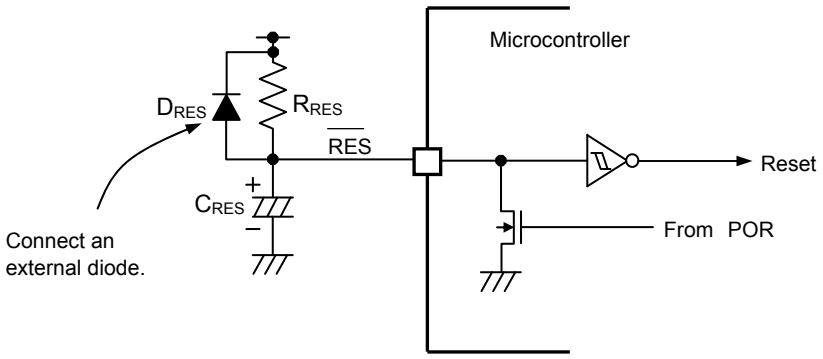


Figure 4.6.8 Sample External POR Circuit Configuration

Appendixes

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Appendix-II

Address	Initial value	R/W	LC870K00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0-017F	XXXX XXXX	R/W	RAM384B	9 bits long									
FE00	0000 0000	R/W	AREG		-	AREG7	AREG6	AREG5	AREG4	AREG3	AREG2	AREG1	AREG0
FE01	0000 0000	R/W	BREG		-	BREG7	BREG6	BREG5	BREG4	BREG3	BREG2	BREG1	BREG0
FE02	0000 0000	R/W	CREG		-	CREG7	CREG6	CREG5	CREG4	CREG3	CREG2	CREG1	CREG0
FE03													
FE04													
FE05													
FE06	0000 0000	R/W	PSW		-	CY	AC	PSWB5	PSWB4	LDCBNK	OV	P1	PARITY
FE07	HHHH HH00	R/W	PCON		-	-	-	-	-	-	-	PDN	IDLE
FE08	0000 HH00	R/W	IE		-	IE7	XFLG	HFLG	LFLG	-	-	XCNT1	XCNT0
FE09	0000 0000	R/W	IP		-	IP4B	IP43	IP3B	IP33	IP2B	IP23	IP1B	IP13
FE0A	0000 0000	R/W	SPL		-	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0
FE0B	0000 0000	R/W	SPH		-	SP15	SP14	SP13	SP12	SP11	SP10	SP9	SP
FE0C	HHHH H000	R/W	CLKDIV		-	-	-	-	-	-	CLKDV2	CLKDV1	CLKDV0
FE0D	H0HH HHHH	R/W	MRCR		-	-	MRCST	-	-	-	-	-	-
FE0E	0HH0 HH0H	R/W	OCR	XT1 and XT2 read at bits 2 and 3	-	CLKSGL	-	-	CLKCB4	-	-	RCSTOP	-
FE0F													
FE10	0000 0000	R/W	T0CNT		-	T0HRUN	T0LRUN	T0LONG	T0LEXT	T0HCMP	T0HIE	T0LCMP	T0LIE
FE11	0000 0000	R/W	T0PRR	Prescaler is 8 bits long. (max. 256 Tcyc).	-	T0PRR7	T0PRR6	T0PRR5	T0PRR4	T0PRR3	T0PRR2	T0PRR1	T0PRR0
FE12	0000 0000	R	T0L		-	T0L7	T0L6	T0L5	T0L4	T0L3	T0L2	T0L1	T0L0
FE13	0000 0000	R	T0H		-	T0H7	T0H6	T0H5	T0H4	T0H3	T0H2	T0H1	T0H0
FE14	0000 0000	R/W	T0LR		-	T0LR7	T0LR6	T0LR5	T0LR4	T0LR3	T0LR2	T0LR1	T0LR0
FE15	0000 0000	R/W	T0HR		-	T0HR7	T0HR6	T0HR5	T0HR4	T0HR3	T0HR2	T0HR1	T0HR0
FE16	XXXX XXXX	R	T0CAL	Timer 0 capture register L	-	T0CAL7	T0CAL6	T0CAL5	T0CAL4	T0CAL3	T0CAL2	T0CAL1	T0CAL0
FE17	XXXX XXXX	R	T0CAH	Timer 0 capture register H	-	T0CAH7	T0CAH6	T0CAH5	T0CAH4	T0CAH3	T0CAH2	T0CAH1	T0CAH0
FE18	0000 0000	R/W	T1CNT		-	T1HRUN	T1LRUN	T1LONG	T1PWM	T1HCMP	T1HIE	T1LCMP	T1LIE
FE19	0000 0000	R/W	T1PRR		-	T1HPRE	T1HPRC2	T1HPRC1	T1HPRC0	T1LPRE	T1LPRC2	T1LPRC1	T1LPRC0
FE1A	0000 0000	R	T1L		-	T1L7	T1L6	T1L5	T1L4	T1L3	T1L2	T1L1	T1L0
FE1B	0000 0000	R	T1H		-	T1H7	T1H6	T1H5	T1H4	T1H3	T1H2	T1H1	T1H0
FE1C	0000 0000	R/W	T1LR		-	T1LR7	T1LR6	T1LR5	T1LR4	T1LR3	T1LR2	T1LR1	T1LR0
FE1D	0000 0000	R/W	T1HR		-	T1HR7	T1HR6	T1HR5	T1HR4	T1HR3	T1HR2	T1HR1	T1HR0

Address	Initial value	R/W	LC870K00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE1E													
FE1F													
FE20													
FE21													
FE22													
FE23													
FE24													
FE25													
FE26													
FE27													
FE28													
FE29													
FE2A													
FE2B													
FE2C													
FE2D													
FE2E													
FE2F													
FE30													
FE31													
FE32													
FE33													
FE34	0000 0000	R/W	SCON1		-	SI1M1	SI1M0	SI1RUN	SI1REC	SI1DIR	SI1OVR	SI1END	SI1IE
FE35	00000 0000	R/W	SBUF1	9bit REG	SBUF18	SBUF17	SBUF16	SBUF15	SBUF14	SBUF13	SBUF12	SBUF11	SBUF10
FE36	0000 0000	R/W	SBR1		-	SBRG17	SBRG16	SBRG15	SBRG14	SBRG13	SBRG12	SBRG11	SBRG10
FE37													
FE38													
FE39													
FE3A													
FE3B													
FE3C													
FE3D													

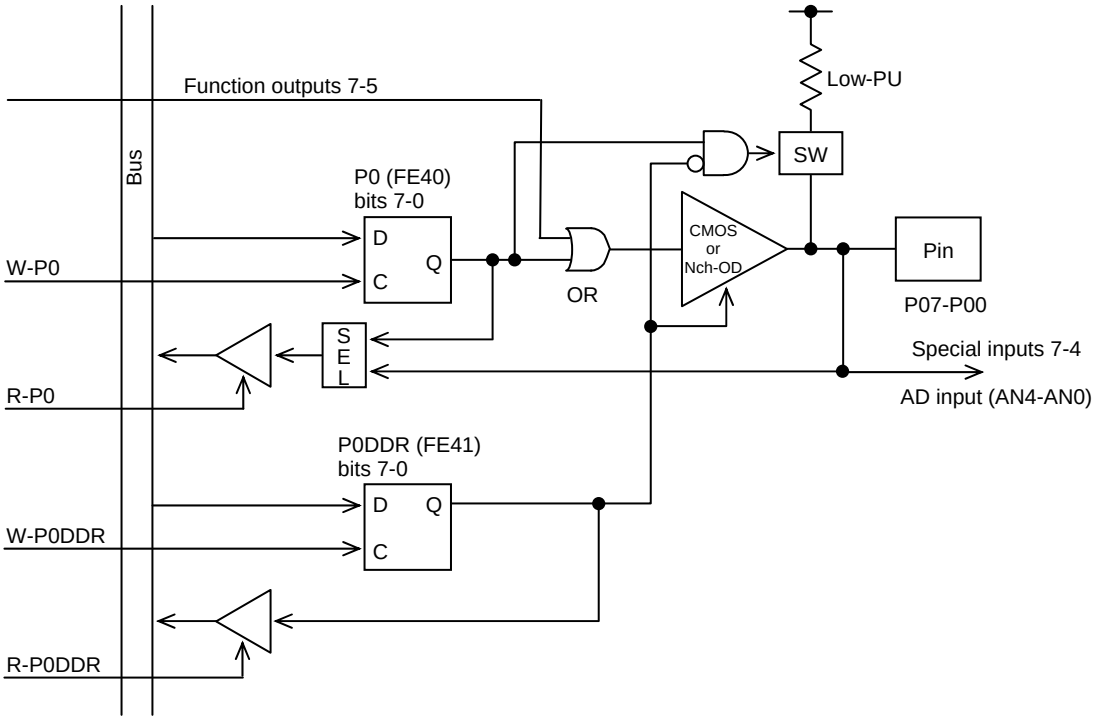
Address	Initial value	R/W	LC870K00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE3E													
FE3F													
FE40	0000 0000	R/W	P0		-	P07	P06	P05	P04	P03	P02	P01	P00
FE41	0000 0000	R/W	P0DDR		-	P07DDR	P06DDR	P05DDR	P04DDR	P03DDR	P02DDR	P01DDR	P00DDR
FE42	00HH 0000	R/W	P0FCR		-	T70E	T60E	-	-	CLKOEN	CKODV2	CKODV1	CKODV0
FE43													
FE44													
FE45													
FE46													
FE47	000H HHH0	R/W	P1TST		-	FIX0	FIX0	FIX0	-	-	-	-	FIX0
FE48													
FE49													
FE4A	HHHH 0000	R/W	I45CR		-	-	-	-	-	INT4HEG	INT4LEG	INT4IF	INT4IE
FE4B	HHHH HH00	R/W	I45SL		-	-	-	-	-	-	-	I4SL1	I4SL0
FE4C	HHHH HHH0	R/W	P3		-	-	-	-	-	-	-	-	P30
FE4D	HHHH HHH0	R/W	P3DDR		-	-	-	-	-	-	-	-	P30DDR
FE4E													
FE4F													
FE50													
FE51													
FE52													
FE53													
FE54													
FE55													
FE56													
FE57													
FE58	0000 0000	R/W	ADCRC	12-bit AD control	-	ADCHSEL3	ADCHSEL2	ADCHSEL1	ADCHSEL0	ADCR3	ADSTART	ADENDF	ADIE
FE59	0000 0000	R/W	ADMRC	12-bit AD mode	-	ADMD4	ADMD3	ADMD2	ADMD1	ADMD0	ADMR2	ADTM1	ADTM0
FE5A	0000 0000	R/W	ADRLC	12-bit AD conversion results L	-	DATAL3	DATAL2	DATAL1	DATAL0	ADRL3	ADRL2	ADRL1	ADTM2
FE5B	0000 0000	R/W	ADRHC	12-bit AD conversion results H	-	DATA7	DATA6	DATA5	DATA4	DATA3	DATA2	DATA1	DATA0
FE5C													
FE5D													

Address	Initial value	R/W	LC870K00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE5E	0000 0000	R/W	I23CR		-	INT3HEG	INT3LEG	INT3IF	INT3IE	INT2HEG	INT2LEG	INT2IF	INT2IE
FE5F	0000 0000	R/W	ISL	Bits 2, 6, and 7 added	-	STOHCP	STOLCP	BTIMC1	BTIMC0	BUZON	NFSEL	NFON	STOIN
FE60													
FE61													
FE62													
FE63													
FE64													
FE65													
FE66													
FE67													
FE68													
FE69													
FE6A													
FE6B													
FE6C													
FE6D													
FE6E													
FE6F													
FE70													
FE71													
FE72													
FE73													
FE74													
FE75													
FE76													
FE77	H00H HHHH	R/W	P0FCNT		-	-	P06FCNT	P05FCNT	-	-	-	-	-
FE78	0000 0000	R/W	T67CNT		-	T7C1	T7C0	T6C1	T6C0	T7OV	T7IE	T6OV	T6IE
FE79	0000 0000	R/W	WDTCNT	Watchdog timer control	-	RSTFLG	FIX0	WDTRUN	IDLOP1	IDLOP0	WDTSL2	WDTSL1	WDTSL0
FE7A	0000 0000	R/W	T6R		-	T6R7	T6R6	T6R5	T6R4	T6R3	T6R2	T6R1	T6R0
FE7B	0000 0000	R/W	T7R		-	T7R7	T7R6	T7R5	T7R4	T7R3	T7R2	T7R1	T7R0
FE7C	HHHH HH00	R/W	SLWRC		-	-	-	-	-	-	-	SLRCSEL	SLRCSTAT

Address	Initial value	R/W	LC870K00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE7D													
FE7E	0000 0000	R/W	FSR0	FLASH control (Bit 4 is R/0.)	-	FSR0B7 Fix to 0	FSR0B6 Fix to 0	FSAERR	FSWOK	INTHIGH	FSLDAT	FSPGL	FSWREQ
FE7F	0000 0000	R/W	BTCR	Base timer control	-	BTFST	BTON	BTC11	BTC10	BTIF1	BTIE1	BTIF0	BTIE0
FE80													
FE81													
FE82													
FE83													
FE84													
FE85													
FE86													
FE87													
FE88													
FE89													
FE8A													
FE8B													
FE8C													
FE8D													
FE8E													
FE8F													
FE90	0000 0000	R/W	P2CR1		-	P2EN	P2ON	P2MD	P2SEN	P2SLPE	P2C2FG	P2SIRQ	P2SIEN
FE91	H000 0000	R/W	P2CR2		-	-	P2C0SL2	P2C0SL1	P2C0SL0	P2P0EN	P2C0EN	P2A2C1	P2A2C0
FE92	0000 0000	R/W	P2DLY		-	P2DL7	P2DL6	P2DL5	P2DL4	P2DL3	P2DL2	P2DL1	P2DL0
FE93													
FE94	0000 0000	R/W	P2EAL		-	P2EA7	P2EA6	P2EA5	P2EA4	P2EA3	P2EA2	P2EA1	P2EA0
FE95	HHHH H000	R/W	P2EAH		-	-	-	-	-	-	P2EAA	P2EA9	P2EA8
FE96	0000 0000	R/W	P2EBL		-	P2EB7	P2EB6	P2EB5	P2EB4	P2EB3	P2EB2	P2EB1	P2EB0
FE97	HHHH H000	R/W	P2EBH		-	-	-	-	-	-	P2EBA	P2EB9	P2EB8
FE98	0000 0000	R	P2CPL		-	P2CP7	P2CP6	P2CP5	P2CP4	P2CP3	P2CP2	P2CP1	P2CP0
FE99	0HHH H000	R/W	P2CPH	(Bits 2,1,0 are R/0.)	-	P2CPSL	-	-	-	-	P2CPA	P2CP9	P2CP8
FE9A	HH00 0000	R/W	P2CR3		-	-	-	P2C3IRQ	P2C3IEN	P2C2IRQ	P2C2IEN	P2T0IRQ	P2T0IEN
FE9B	HH00 0000	R/W	P2CR4		-	-	-	P2C6VR1	P2C6VR0	P2C6HEG	P2C6LEG	P2C6IRQ	P2C6IEN

Address	Initial value	R/W	LC870K00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FE9C	HH00 0000	R/W	P2CR5		-	-	-	P2C8VR1	P2C8VR0	P2C8IRQ	P2C8IEN	P2C7IRQ	P2C7IEN
FE9D	0000 0000	R/W	P2C1DS		-	P2C1DS7	P2C1DS6	P2C1DS5	P2C1DS4	P2C1DS3	P2C1DS2	P2C1DS1	P2C1DS0
FE9E	0000 0000	R/W	P2T0T		-	P2T0T7	P2T0T6	P2T0T5	P2T0T4	P2T0T3	P2T0T2	P2T0T1	P2T0T0
FE9F	HH00 0000	R/W	P2C3DS		-	-	-	P2C3DS5	P2C3DS4	P2C3DS3	P2C3DS2	P2C3DS1	P2C3DS0
FEA0	HH00 0000	R/W	P2C8DS		-	-	-	P2C8DS5	P2C8DS4	P2C8DS3	P2C8DS2	P2C8DS1	P2C8DS0
FEA1													
FEA2													
FEA3													
FEA4													
FEA5													
FEA6													
FEA7													
FEA8													
FEA9													
FEAA													
FEAB													
FEAC													
FEAD													
FEAE													
FEAF													
FEB0													
FEB1													
FEB2													
FEB3													
FEB4													
FEB5													
FEB6													
FEB7													
FEB8													
FEB9													
FEBA													
FEBB													

Address	Initial value	R/W	LC870K00	Remarks	BIT8	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
FEBC													
FEBD													
FEBE													
FEBF													
FEC0													
FEC1													
FEC2													
FEC3													
FEC4													
FEC5													
FEC6													
FEC7													
FEC8													
FEC9													
FECA													
FECB													
FECC													
FECD													
FECE													
FECF													
FED0	0000 0000	R/W	UCON0		-	UBRSEL	STRDET	RECRUN	STPERR	U0B3	RBIT8	RECEND	RECIE
FED1	0000 0000	R/W	UCON1		-	TRUN	8/9BIT	TDDR	TCMOS	8/7BIT	TBIT8	TEPTY	TRNSIE
FED2	0000 0000	R/W	UBR		-	UBRG7	UBRG6	UBRG5	UBRG4	UBRG3	UBRG2	UBRG1	UBRG0
FED3	0000 0000	R/W	TBUF		-	T1BUF7	T1BUF6	T1BUF5	T1BUF4	T1BUF3	T1BUF2	T1BUF1	T1BUF0
FED4	0000 0000	R/W	RBUF		-	R1BUF7	R1BUF6	R1BUF5	R1BUF4	R1BUF3	R1BUF2	R1BUF1	R1BUF0
FED5													
FED6													
FED7													
FED8													
FED9													
FEDA													
FEDB													



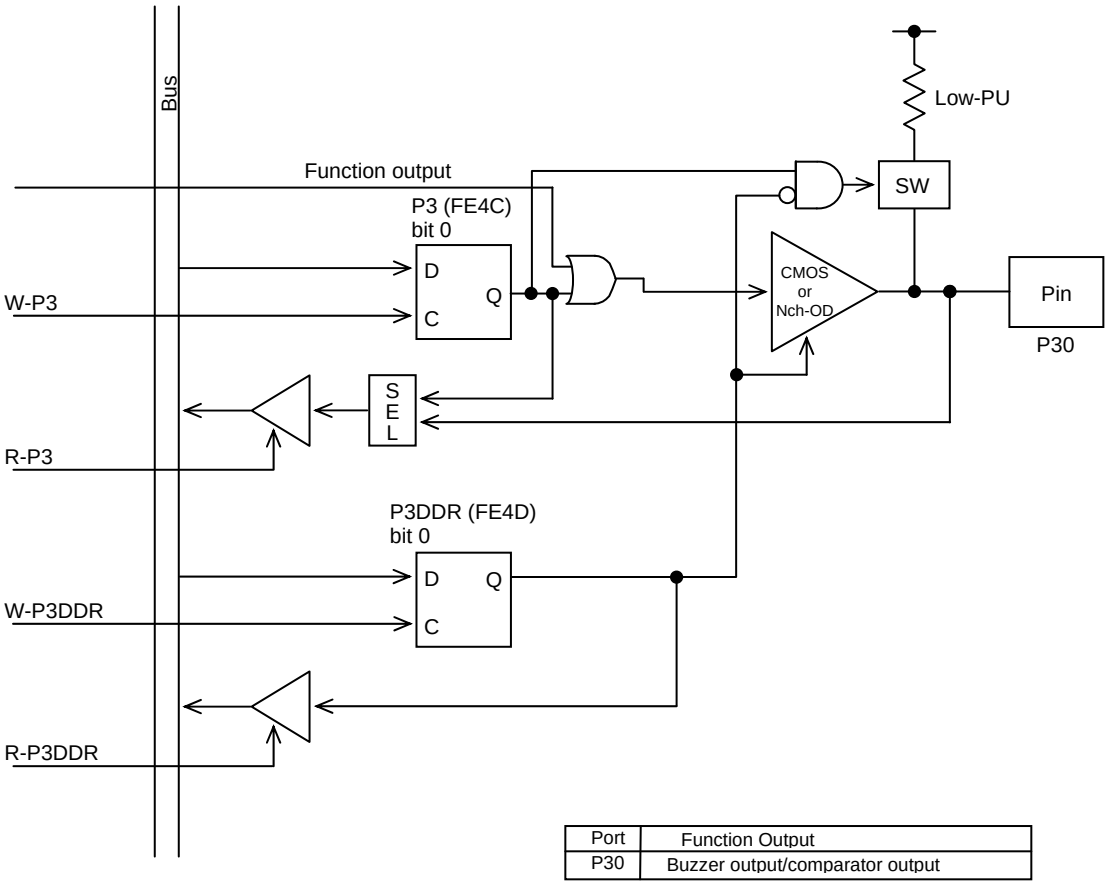
Port	Special Input	Function Output
P07	INT3 input	Timer 7 toggle output/PPG output for monitoring signals
P06	SIO1 clock input/ UART1data input	SIO1 clock output/ timer 6 toggle output
P05	SIO1 data input	SIO1 data output/ UART1data output/system clock output
P04	INT4 input/AD analog 4 input	None
P03	AD analog 3 input	None
P02	AD analog 2 input	None
P01	AD analog 1 input	None
P00	AD analog 0 input	None

Table of Port 0 Multiplexed Pin Functions

Port 0 Block Diagram

Option: Output type (CMOS or N-channel OD) selectable in 1-bit units.

Port Block Diagrams

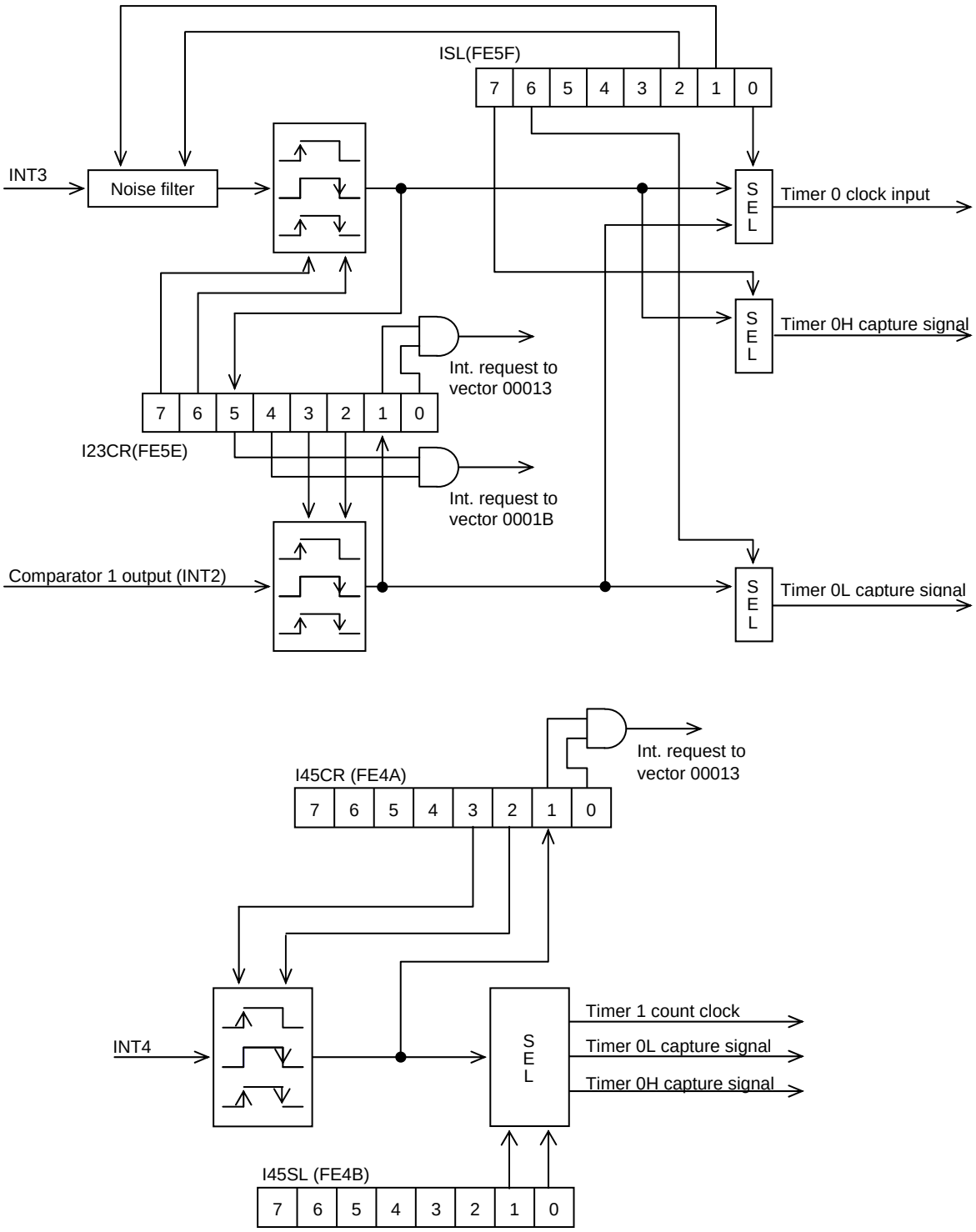


Port	Function Output
P30	Buzzer output/comparator output

Table of Port 3 Multiplexed Pin Functions

Port 3 Block Diagram

Option: Output type (CMOS or N-channel OD) selectable in 1-bit units.



Interrupt Block Diagram

Port Block Diagrams

Important Note

This document is designed to provide the reader with accurate information in easily understandable form regarding the device features and the correct device implementation procedures.
The sample configurations included in the various descriptions are intended for reference only and should not be directly incorporated in user product configurations.
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LC870K00 SERIES
USER'S MANUAL
Rev. 0 May, 2016
Microcontroller Business Unit
ON Semiconductor