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AND9296/D

A 65 W Adaptor with NCP1239 Fixed Frequency Controller

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APPLICATION NOTE

The NCP1239 is a fixed-frequency current-mode controller featuring a high-voltage start-up current source to provide a quick and lossless power-on sequence.

With a supply range up to 35 V, the controller hosts a jittered 65 or 100 kHz switching circuitry operated in peak current mode control. When the power on the secondary side starts to decrease, the controller automatically folds back its switching frequency down to minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while limiting the peak current that insures excellent efficiency in light load condition.

It features a timer-based fault detection circuitry that ensures a quasi-flat overload detection, independent of the input voltage.

This application note focuses on the experimental results of a 65 W adaptor driven by the NCP1239 and on the general behavior of this controller.

Table 1. EVALUATION BOARD SPECIFICATION

Parameter	Value
Minimum Input Voltage	85 Vrms
Maximum Input Voltage	265 Vrms
Output Voltage	19 V
Nominal Output Power	65 W

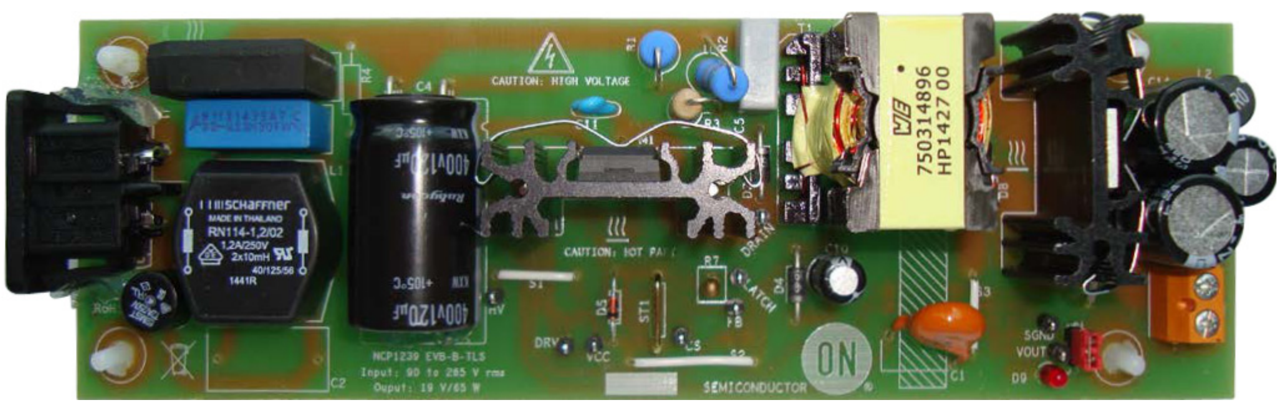

Figure 1. EVB Picture (Top View)

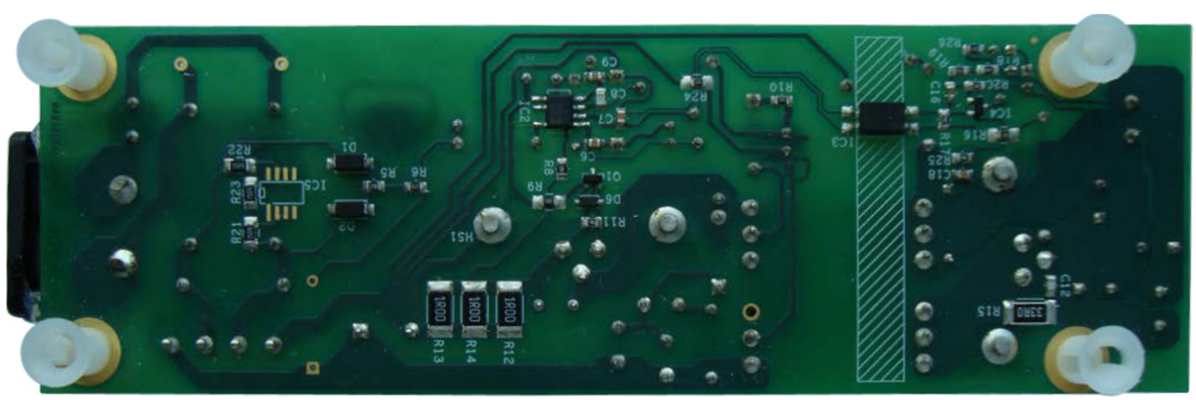

Figure 2. EVB Picture (Bottom View)

Board Schematic

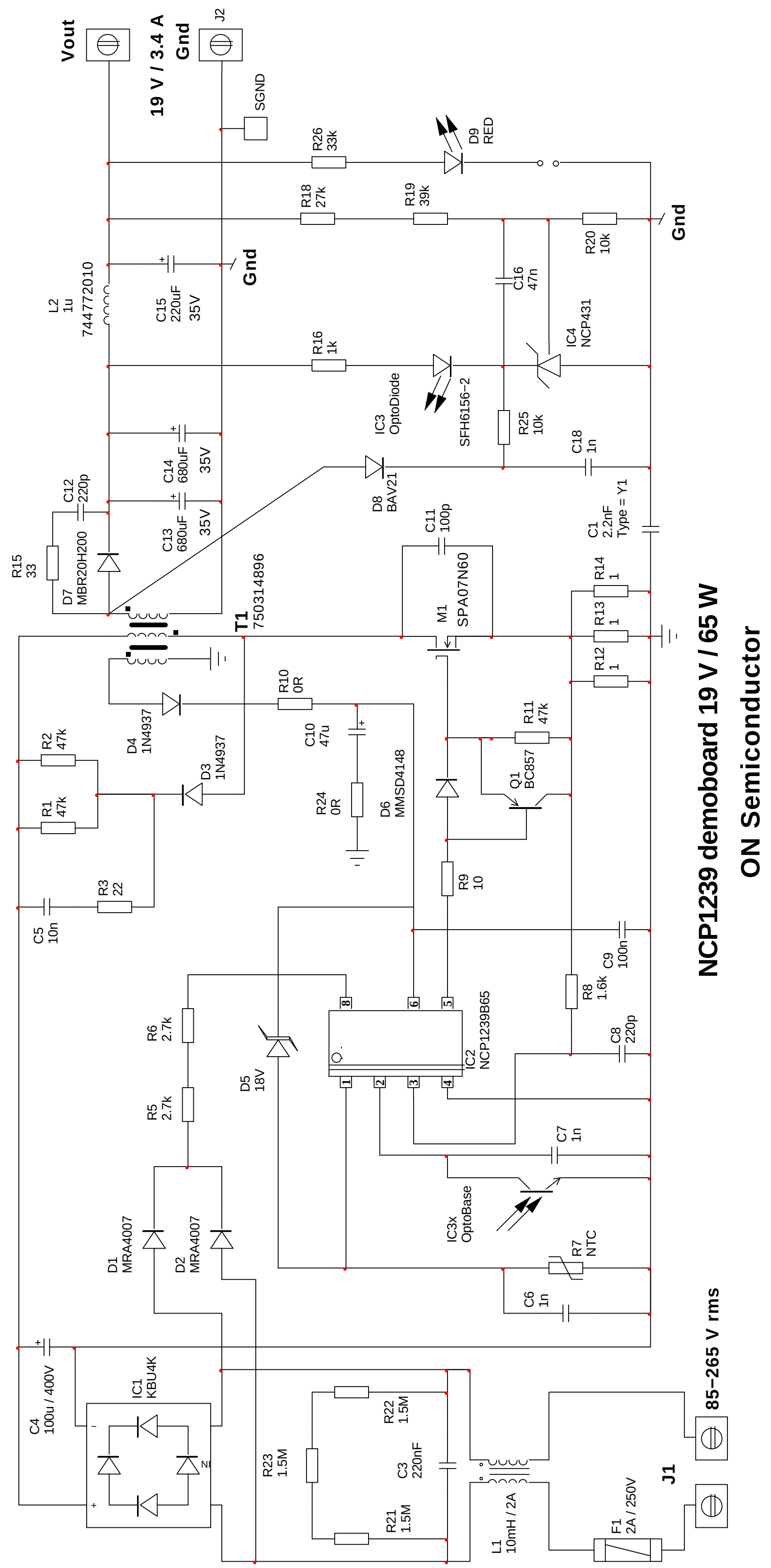

Figure 3. Evaluation Board Schematic

Start-up

The start-up sequence is performed with an internal high voltage current source in order to reduce standby power consumption. The start-up time is directly linked to the V_{CC} capacitor value. Also, this capacitor has to be large enough to maintain the V_{CC} voltage above $V_{CC(off)}$ level in no load condition. Indeed, in light load or no load condition, the controller enters in deep skip cycle mode and the dead time between two cycles can be larger than 15 ms and V_{CC} voltage has to be kept above $V_{CC(off)}$. Finally, the last constraints regarding the V_{CC} capacitor is the start-up time. Generally, the power supply has to start in less than 3 s. Taking in account these parameters, in ours application board, we have successfully tested (Figure 4) a 47 μF value for C_{10}.

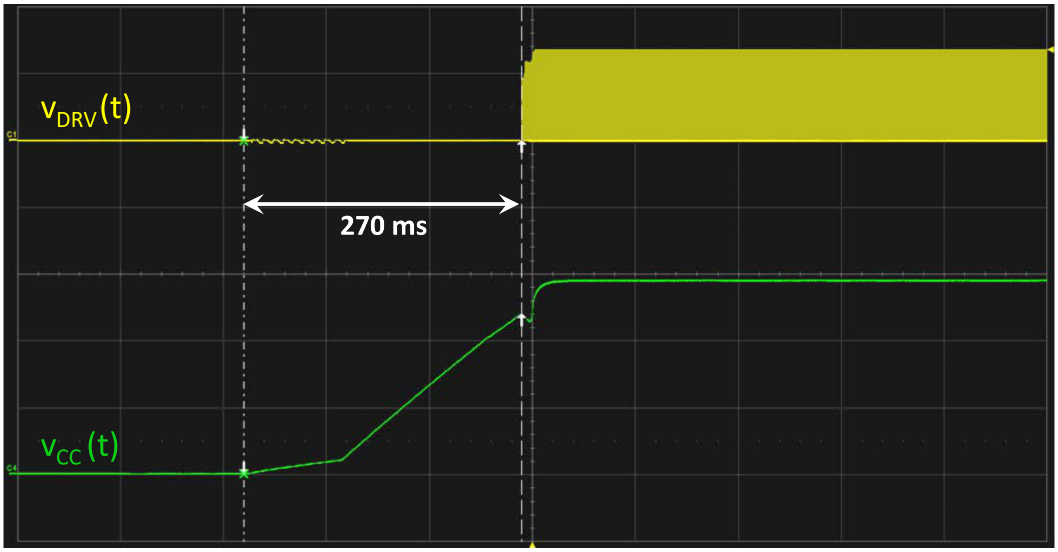

Figure 4. The Start-up Sequence is below 3 s

The start-up sequence also involves the internal 8-ms soft-start depicted in Figure 5. During this time, the peak current setpoint is linearly increased from a very low value up to the allowable maximum. This soft-start circuitry is activated upon a fresh start-up but also every time a restart is attempted, e.g. in an auto-recovery fault mode.

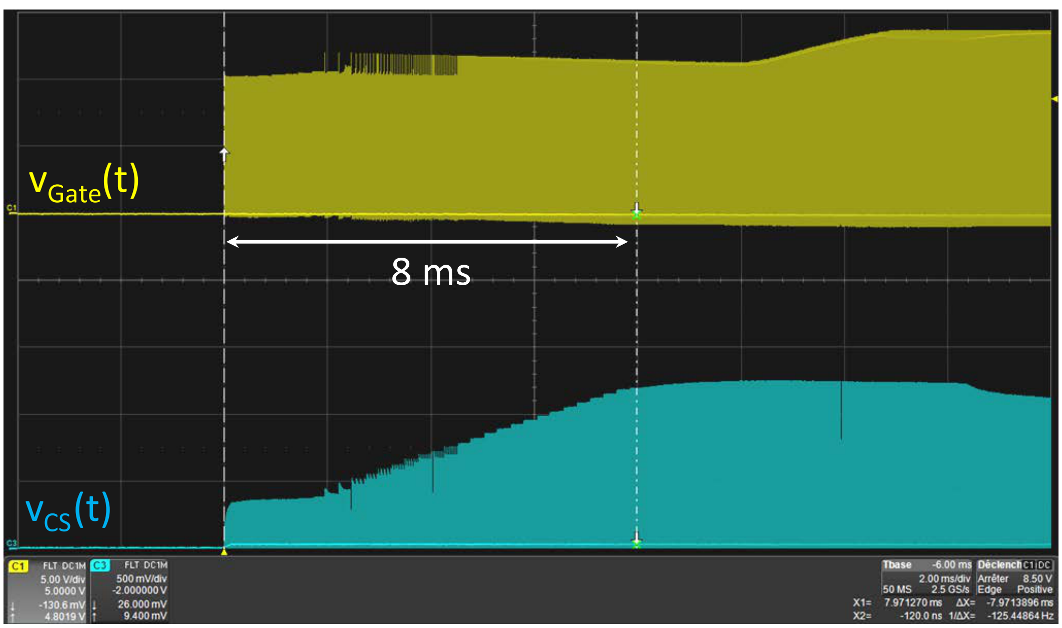

Figure 5. The Soft-start Sequence

Protections

The NCP1239 embeds several needed protections required by ac-dc adapters. They are listed below:

1. **Short Circuit Protection, SCP:** the adapter must sustain a short circuit or an overload on the output voltage without any damages. When short circuit is removed, the power supply must be able to restart and work normally.
2. **Over Voltage Protection, OVP:** when a component on feedback loop like optocoupler is damaged, the output voltage can dramatically grow up and the controller must be turn off immediately to protect devices that can be connected to the adapter.
3. **Over Temperature Protection, OTP:** if the temperature of the adapter exceeds a certain ambient value, there is a risk of destruction. To avoid this from happening, a thermal sensor permanently monitors the temperature and in case it exceeds the limit set by the designer, the adapter shuts down permanently. The adapter is reset when the user cycles the input power and the temperature has decreased.
4. **Over Power Protection, OPP:** for some power supplies, it is important that the maximum output current stays in control in worse case conditions, e.g. when the load is drawing more current that what it should, without being a real short-circuit. In our design, the nominal output current is 3.4 A and must stay below 4.5 A in all input voltage conditions.
5. **Brown-out, BO:** when the adapter is unplugged or if there is a default on the main input, to avoid damages when bulk voltage is too low, the controller has to stop operation and waits the input voltage recovers a normal level before initiate a new start-up sequence.

Let us know check how each requirement has been separately addressed.

Short Circuit Protection

The protection is ensured by monitoring the current sense (CS) signal on pin 3. When this voltage exceeds the maximum internal current setpoint (i.e. 0.8 V), an internal error flag is raised and starts a timer. If the flag is asserted longer than its programmed value (64 ms typical), the driving pulses are stopped. The timer is reset if the CS voltage goes back below the maximum current sense threshold for 8 consecutive pulses. When the fault is validated, the IC consumption is reduced to 500 μA. Thanks to this consumption, V_{CC} decreases and touches the 10 V $V_{CC(min)}$ level. Here, the HV current source is activated to build up the voltage to $V_{CC(on)}$ (12 V). At this moment, depending of the controller option, there are two possible configurations:

- **Auto-recovery:** when the 64 ms timer elapses, the 1 s auto-recovery timer starts. If the 1 s timer is not finished when V_{CC} crosses $V_{CC(on)}$, HV current source is disabled, controller stays off and V_{CC} decays due to IC consumption. Once auto-recovery timer elapses, the controller initiates a new fresh sequence with soft-start at next $V_{CC(on)}$ as shown in Figure 6 and Figure 7.
- **Latching Off:** when the 64 ms timer elapses, the controller enters in endless hiccup mode meaning that V_{CC} will be charged and discharged between $V_{CC(on)}$ and $V_{CC(min)}$ thanks to the HV current source (Figure 8). The only ways to reset the controller and have a new start-up sequence is to unplug to PSU ($V_{CC(reset)}$ or BO even will be detected).

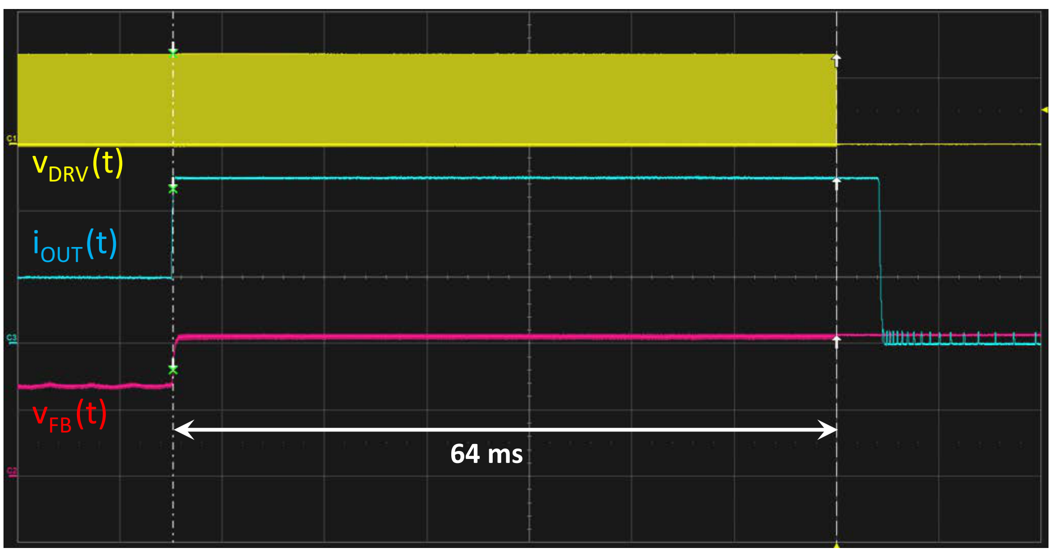

Figure 6. 64-ms Over-current Timer

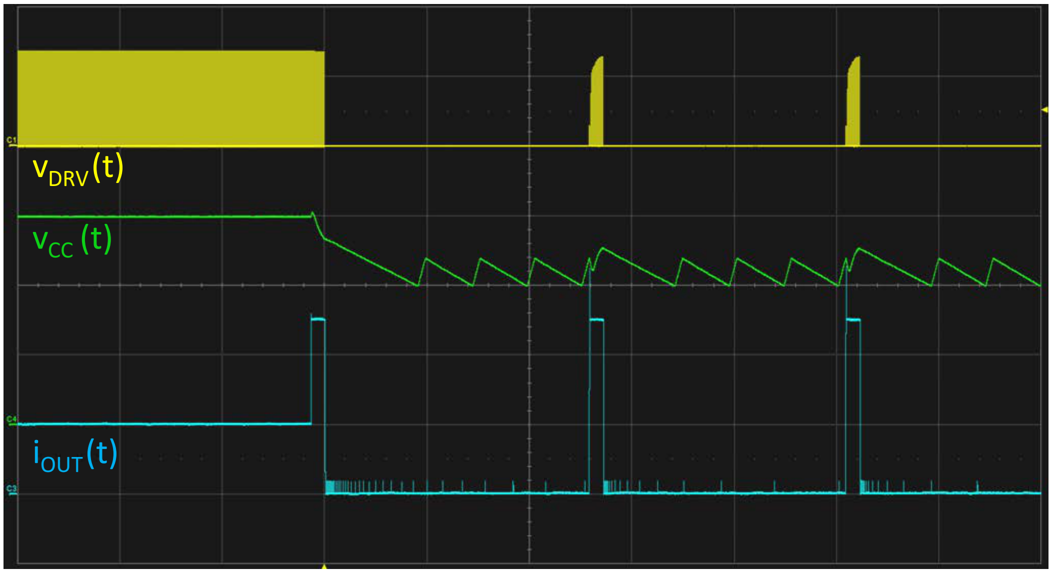

Figure 7. Auto-recovery Mode

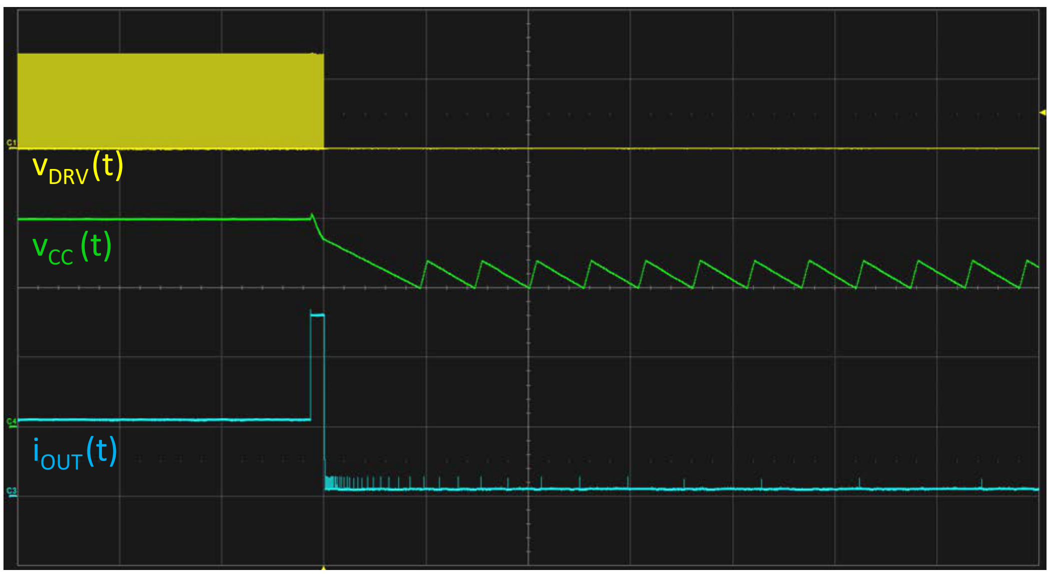

Figure 8. Latching Mode

Over Voltage Protection

When the optocoupler is broken or when the TL431 divider network is affected by a severe drift (or one of its resistor is missing or features a wrong value), then the output voltage can escape from the limits imposed by the specifications: this is an over voltage condition. To protect the converter, the controller has a dedicated fault pin (pin 1) that combines the OVP detection and also the Over Temperature Protection (see next section). The OVP detection is made when the fault pin voltage exceeds 3 V during 4 consecutives pulses, the controller is latched off. To perform this function, a Zener diode is usually connected between the V_{CC} pin (pin 5) and fault pin. The level is given by $V_{AUX(OVP)} = V_Z + V_{Fault(OVP)}$ where $V_{AUX(OVP)}$ is the voltage on Auxilary winding during the off time and $V_{Fault(OVP)}$ is the 3-V threshold. Also, Auxiliary voltage is linked to the output voltage with the transformer turns ratio: $V_{AUX} = (N_{Aux} / N_{Sec}) * V_{OUT}$. We can deduct from these equations the needed Zener diode value following the wanted maximum output voltage in fault mode. Typical waveforms are shown on Figure 9 and Figure 10.

Figure 9. 4 Consecutives Pulses to Validate the OVP Fault

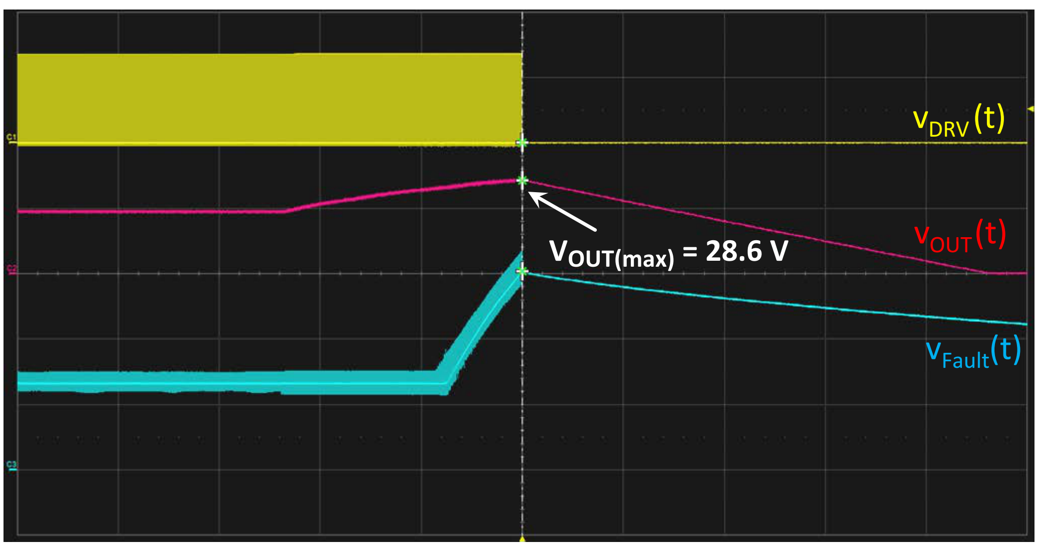

Figure 10. OVP Event on Fault Pin

Finally, if the OVP function on the fault pin is not used, this protection can be implemented on the V_{CC} pin with a fixed threshold (25.5 V). The level protected the controller itself. The Figure 11 depicts this function. This protection can be auto-recovery or latched depending of the controller version.

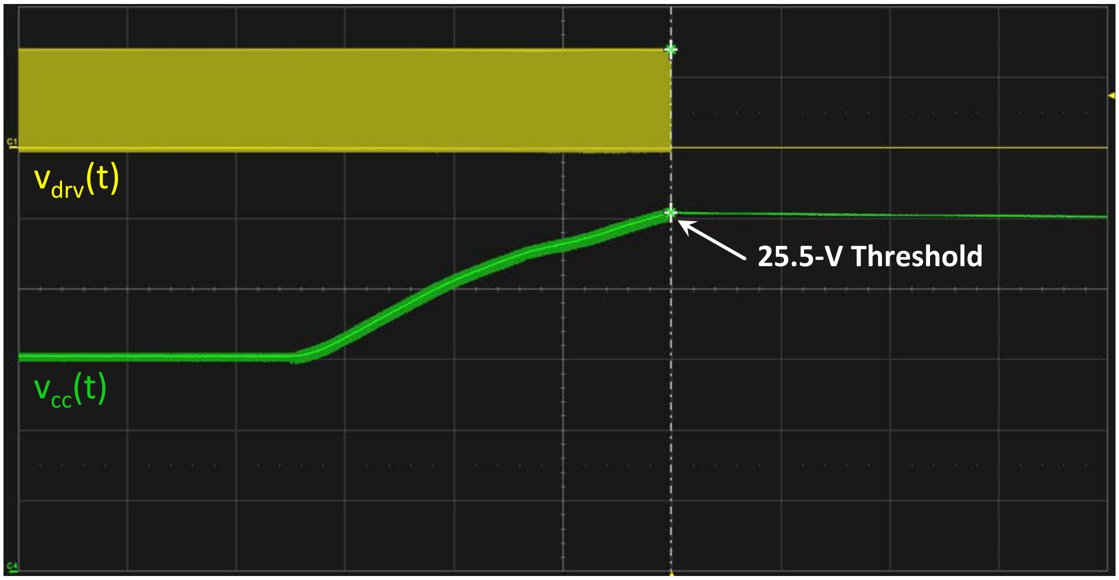

Figure 11. OVP Event on V_{CC} Pin

Over Temperature Protection

Due to the confined environment for adapter application, a protection against run away temperature is highly recommended. The fault pin has another lower threshold (0.4 V) in order to connect a Negative Temperature Coefficient resistance (NTC) with ground reference. In this position, when the temperature increases, the NTC resistance starts to decrease and lifts down the pin 1 voltage. When the level reaches 0.4 V, the part simply latches off and requires a reset before restart. Reset occurs when the user cycles the input voltage.

Since we would like the adapter to enter over temperature protection when ambient reaches 90°C, what will be the needed pull down resistor the trigged the 0.4 V threshold? Assuming the 45 μA internal OTP current source and 0.4 V OTP detection level, at 90°C, NTC resistor should be .

$$R_{NTC\_100} = \frac{0.4\ V}{45\ \mu A} = 8.89\ k\Omega$$

Vishay NTC (NTCLE100E3104JB0W) matches pretty well with the above calculation. The maximum ambient temperature allowed by the demonstration board is around 87°C, so close to the expectation.

Over Power Protection

A current-mode power supply works by setting the inductor peak current according to the output power demand. The inductor current is transformed into a voltage by a sense resistor, R_{12}, R_{13} and R_{14} in our adapter. The peak current setpoint depends on the error voltage delivered on the feedback loop pin. In our adapter, this is the current forced by the TL431 on the secondary side and reflected to the primary over pin 2 of the NCP1239. As detailed in the datasheet, the current setpoint inside the circuit depends on pin 2 level divided by 4. In fault conditions, when the loop is lost, the feedback level can go up to 4.3 V. To avoid any current runaway, the maximum voltage setpoint is safely clamped to 0.8 V. In that case, the maximum peak current in the inductor cannot exceed:

$$I_{pk\_max} = \frac{V_{Limit}}{R_{12}//R_{13}//R_{14}} \quad \text{(eq. 1)}$$

With three paralleled 1 Ω resistances, we expect a maximum peak current to be:

$$I_{pk\_max} = \frac{0.8}{0.33} = 2.4\ A \quad \text{(eq. 2)}$$

The combination of two factors affects the maximum output power delivery: the total propagation delay plays an important role on the primary peak current and the operating mode change between high line and low line.

The propagation delay t_{prop} is the total time taken by the control loop to bring the MOSFET gate down when the peak current limit on CS pin (i.e. 0.8 V) has been reached.

$$I_{pk\_max} = \frac{V_{Limit}}{R_{12}//R_{13}//R_{14}} + \frac{V_{bulk}}{L_p} t_{prop} \quad \text{(eq. 3)}$$

The control chip, alone, is rather fast: 50 ns typically. However, the drive capability and the series drive resistance naturally hamper the turn-off time. Typical total propagation delays are therefore in the vicinity of 250−300 ns. Back to Equation 3 and considering a rectified voltage V_{bulk} of 375 V dc (265 V rms input), the inductor peak current becomes:

$$I_{pk\_max} = \frac{0.8}{0.33} + \frac{375}{600\mu}300n = 2.6\text{ A} \qquad \text{(eq. 4)}$$

This 200 mA difference represents a theoretical 15% output power increase compared to the original calculation.

As said above, the other parameter that plays a role on the maximum power delivery is the operating mode. At low line, the power supply operates in deep Continuous Conduction Mode (CCM) and the energy store in the transformer is:

$$E_p = \frac{1}{2}L_p\left(I_{pk\_max}{}^2 - I_{valley}{}^2\right) \qquad \text{(eq. 5)}$$

However, at high line, the peak current is indeed slightly increased due to the propagation delay but because the off-time has expanded, the valley current I_{valley} is much smaller than at low line: we are going into the Discontinuous Conduction Mode (DCM). If $I_{valley}{}^2$ also goes down in Equation 5, you naturally store more energy into the inductor and the output power runs away. This situation is obviously not acceptable and NCP1239 has a dedication function to fight again this derivation.

NCP1239 senses the input voltage via HV pin. This line voltage is transformed into a current information further applied to the current sense pin. A resistor placed in series from the sense resistance to the CS pin will create an offset voltage proportional to the input voltage variation. Assume we need to reduce the maximum peak current setpoint by 210 mV to reduce the maximum power at the 260 V input. In that case, we will need to generate a 210 mV offset across R_{OPP}. With a 130 μA I_{OPP} current, R_{OPP} should be equal to:

$$R_{OPP} = \frac{210m}{130\mu} = 1.6\text{ k}\Omega \qquad \text{(eq. 6)}$$

With this OPP resistor, the over current limits from 85 V rms to 265 V rms is between 3.9 A and 4.5 A. The maximum output current evolution depending of the input voltage is described in Figure 12.

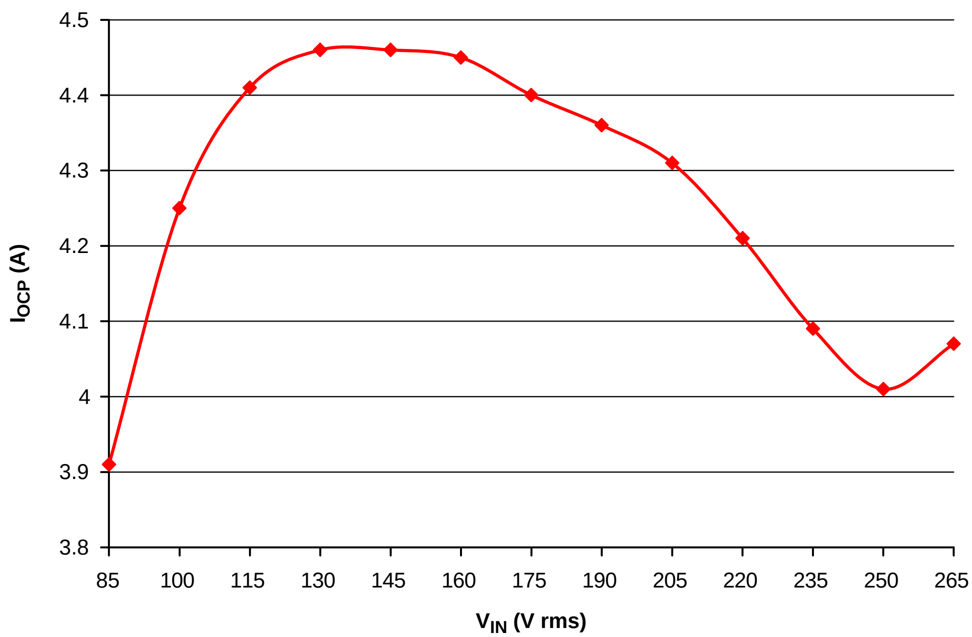

Figure 12. OCP Current vs Input Voltage

Brown-out Protection

The brown-out function is highly recommended to protect the adapter against the low input voltage. Thanks to the HV pin, we have an easy and no-consuming way to implement this function. The brown-out thresholds are fixed:

- Line increasing, $V_{BO(on)}$: the controller is enable when HV pin reaches 110 V dc
- Line decreasing, $V_{BO(off)}$: the controller is disable when HV pin drops below 101 V dc

Please note that different BO level options are available upon request. Please contact sales to have more information.

There are two difference cases where BO event can be detected. The first one is before start-up. The controller starts to wake-up when V_{CC} crosses $V_{CC(min)}$. At this moment, the HV pin level is monitored. If, for any reason, the input voltage is abnormally low, below $V_{BO(on)}$ threshold, the controller do not turn-on the DRV pin and V_{CC} enters in hiccup mode until HV pin recovers a normal level. This typical behavior is described on Figure 13.

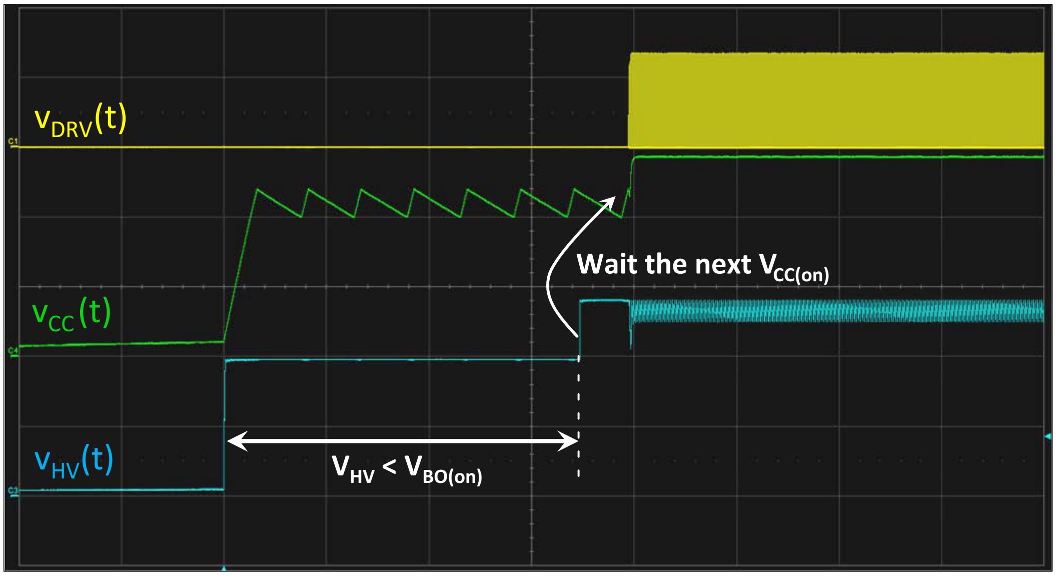

Figure 13. BO Event before Start-up

The second case is when there is a line dropout. Assume the converter operates normally. At a moment, the input voltage drops below the $V_{BO(off)}$ level. A 68 ms timer starts. During timer counting, the controller continues to work. If the line comes back above $V_{BO(on)}$ level, the timer is reset and PSU works normally. This behavior is depicted in Figure 14. If BO timer elapses, DRV pulses are stopped, and V_{CC} enters in hiccup mode thanks to the HV current source. In hiccup mode, when the line recovers its normal level, the controller waits the next $V_{CC(on)}$ to initiate a fresh start-up sequence with soft-start like shown in Figure 15.

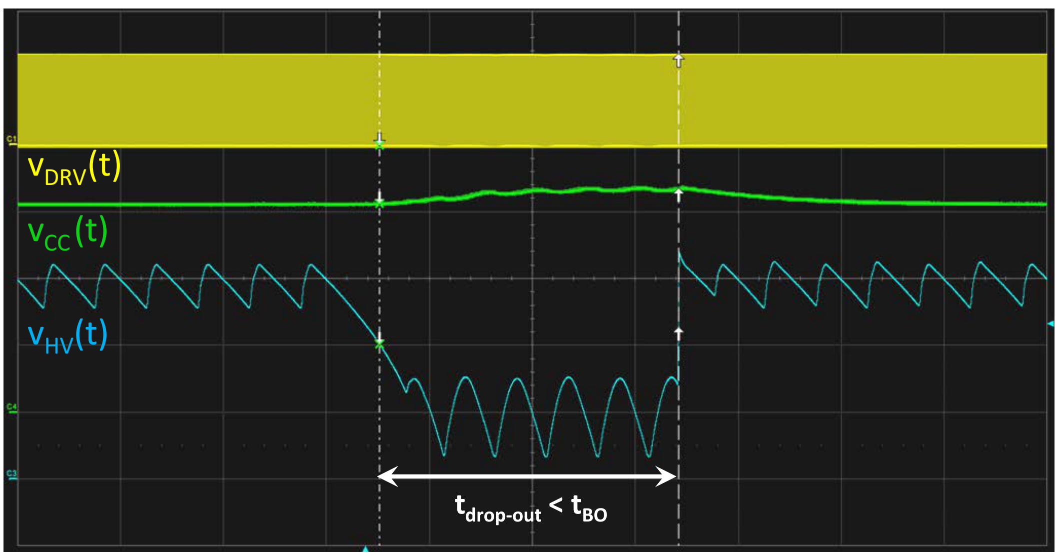

Figure 14. Line Drop-out Duration Shorter than BO Timer

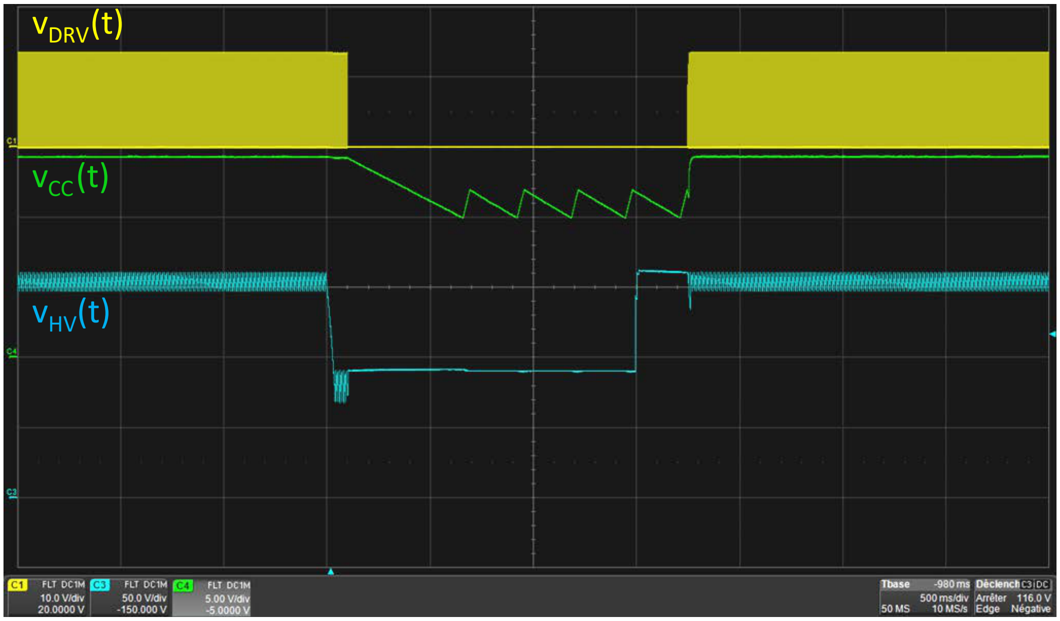

Figure 15. BO Event During Operation

Efficiency Results

All measurements have been done after a 30 min warm-up phase at full load and an additional 5 min at the load under consideration.

The input power was measured with the power meter 66202 from Chroma.

The output voltage and output current were measured using digital multimeter embedded on dc electronic load 66103 from Chroma.

The average efficiency was calculated from the efficiency measurements at 25%, 50%, 75% and 100% of the nominal output power.

Table 2. EFFICIENCY @ 115 V RMS AND 230 V RMS

Input Voltage	Pout (%)	Pout (W)	Pin (W)	Efficiency (%)
115 V rms	100	64.72	72.48	89.29
	75	48.55	54.06	89.82
	50	32.41	35.99	90.05
	25	16.25	18.15	89.52
	Average	–	–	89.67
	No Load*	–	32 m	–
230 V rms	100	64.73	71.62	90.38
	75	48.59	53.88	90.19
	50	32.43	36.12	89.78
	25	16.27	18.24	89.18
	Average	–	–	89.88
	No Load*	–	44 m	–

*Without the LED D9 and with 4.5 MΩ for X2 discharge resistor.

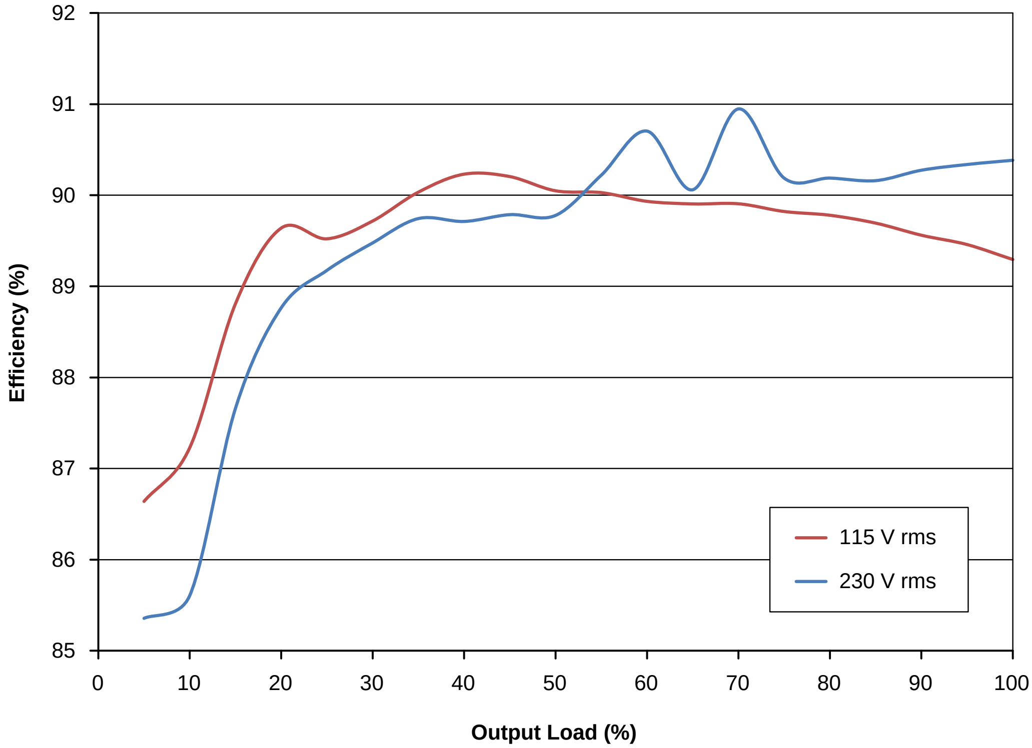

Figure 16. Efficiency (%) vs Output Power (% of max) at 115 V rms and 230 V rms

Please note that the efficiency variation at 230 V rms around 60−70% of the load is due to the DCM mode. Indeed, if the MOSFET is turned on when the drain voltage is in the valley, the efficiency will be better.

If we expand our view on the light-load power consumption, in the range of 1 W output power, we can see that we can deliver more than 0.78 W on the output and keep the input consumption below 1 W.

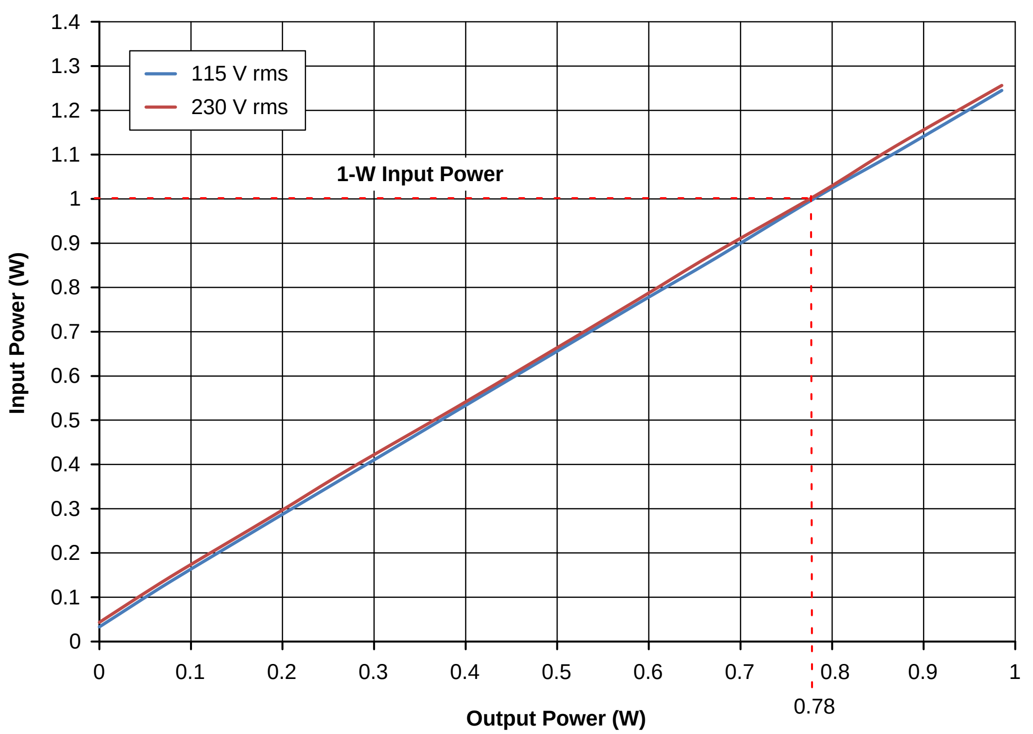

Figure 17. Low Power Consumption

Stand-by Performance

The stand-by consumption is a key parameter for this kind of application. Thanks to the HV startup current, the resistance needed to build up the V_{CC} voltage can be saved and so the power dissipation. Moreover, the input power in no load condition is highly impacted by the IC consumption itself so this parameter has been optimized for the NCP1239 controller.

Thanks to these two points, the standby consumption is below 50 mW regardless the input voltage like shown in the Table 3. Also, if we consider a LED connected on the output voltage through a 33 kΩ resistance, the input power is still below 60 mW @ 230 V rms.

Table 3. STAND-BY CONSUMPTION

Input Voltage	Without LED D9	With LED D9
85 Vrms	30 mW	43 mW
115 Vrms	32 mW	44 mW
230 Vrms	44 mW	55 mW
265 Vrms	49 mW	61 mW

We can improve even more the standby performance by playing with some components like the optocoupler or the bridge divider on the NCP431 reference pin. These all methods are explained and tested around the NCP1256 controller on the AND9208 application note.

Typical Waveforms

The feedback voltage on the primary side is an image of the load on the secondary side. Depending on the FB level, the NCP1239 controller can operate in several modes. From fixed frequency to skip mode passing by the frequency foldback or frequency clamp mode, all these modes are explained and illustrated in the following section. Also, the NCP1239 operation can be illustrated versus the FB pin voltage (Figure 18).

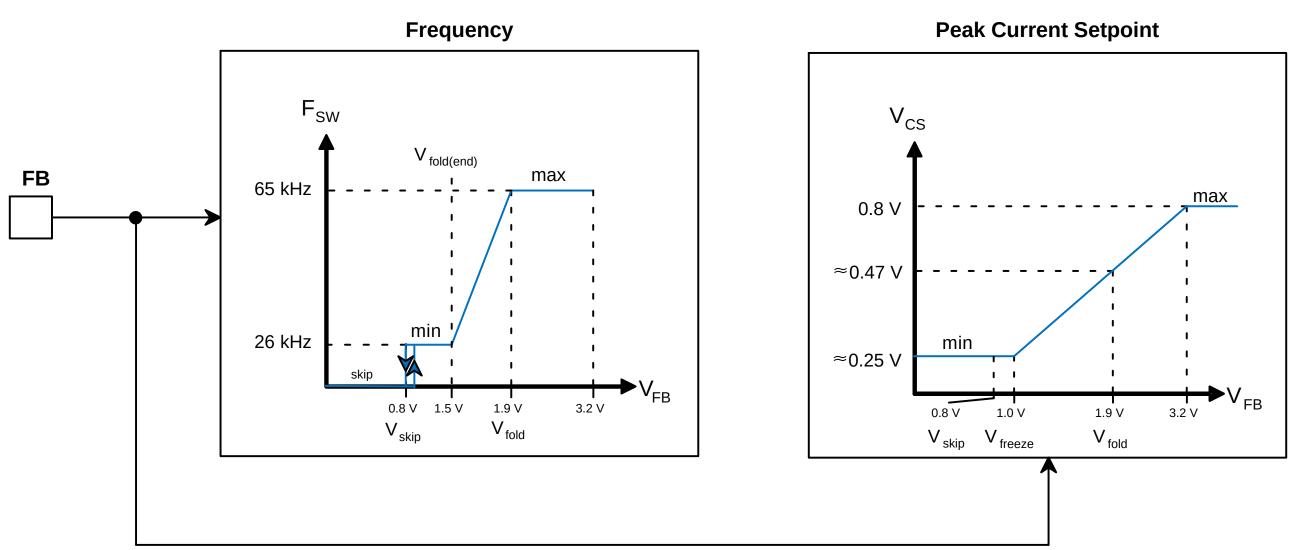

Figure 18. By Observing the Voltage on the Feedback Pin, the Controller Reduces its Switching Frequency

Fixed Frequency Mode

When the output load is close to the maximum, the controller operates in fixed frequency mode. If the load decreased, the frequency will remain unchanged, 65 kHz here, but the primary peak current will be reduced to transfer less energy on the secondary side.

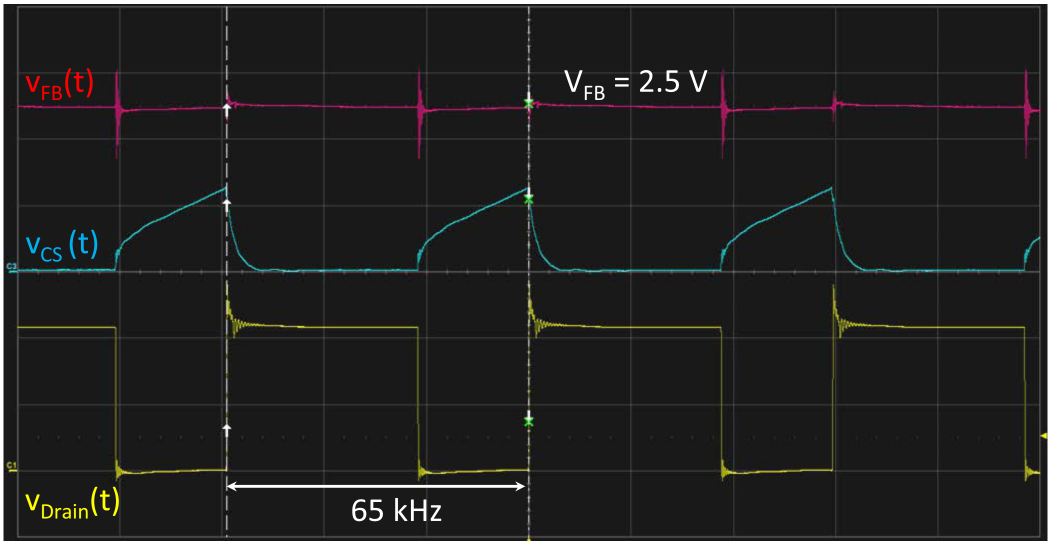

Figure 19. Fixed Frequency Operation @ 65 W/140 V dc

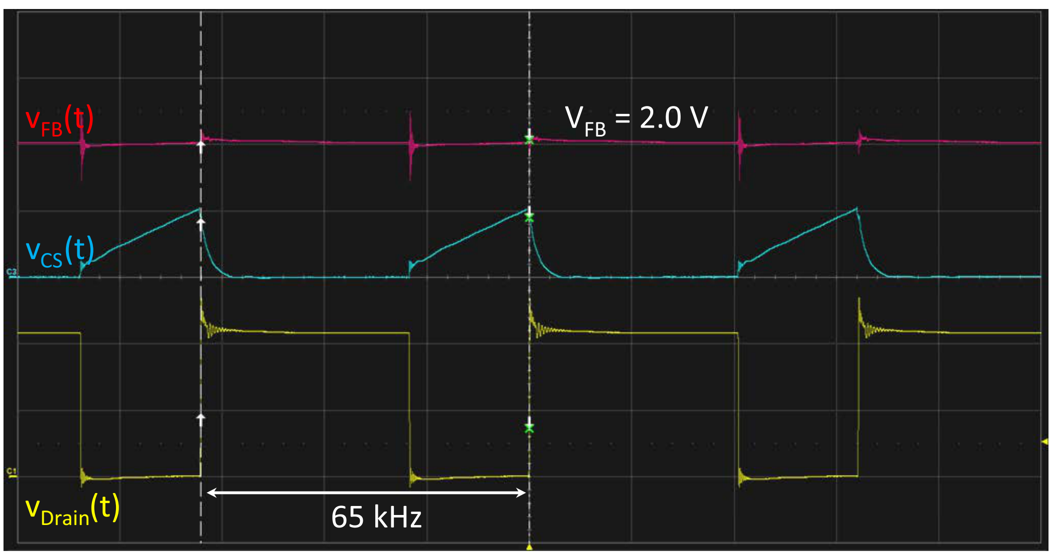

Figure 20. Fixed Frequency Operation @ 47 W/140 V dc

Frequency Foldback mode

If while operating in fixed frequency, the load further decreases, the NCP1239 will operate in Frequency Foldback (FF) mode. Practically, the circuit enters in FF mode when FB voltage drops below 1.9 V. In this mode, both frequency and primary peak current vary according to the feedback voltage as shown in Figure 21 and Figure 22.

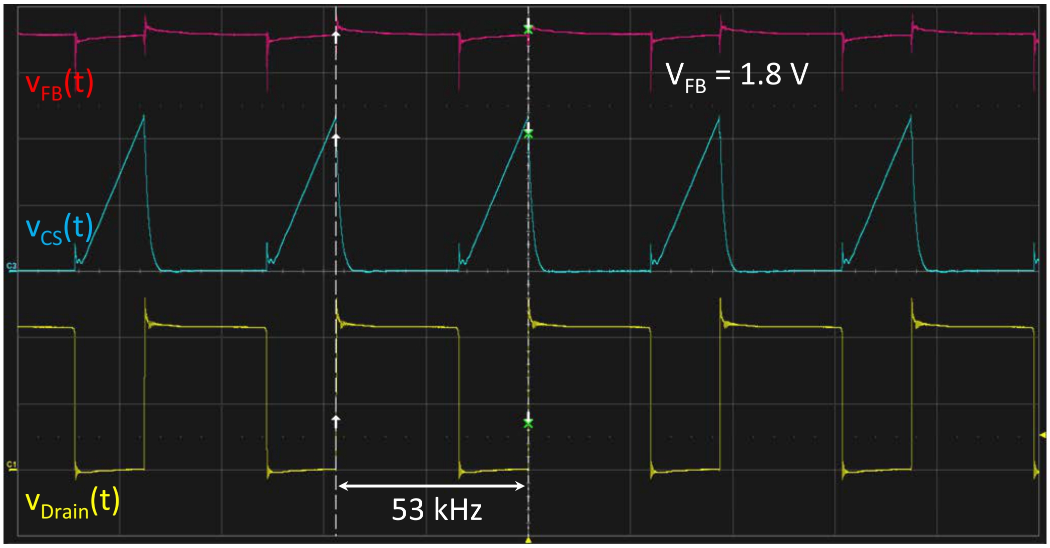

Figure 21. Frequency Foldback Operation @ 34 W/140 V dc

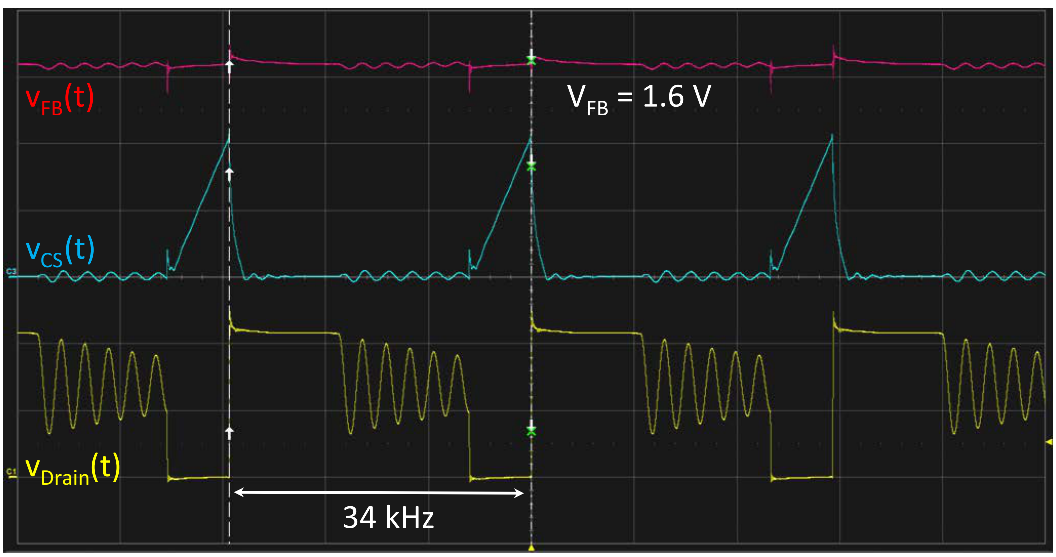

Figure 22. Frequency Foldback Operation @ 18 W/140 V dc

Frequency Clamp Mode

The switching frequency is clamped to 26 kHz in order to avoid acoustic noise frequency range. The regulation is made by varying the primary peak current (I_{peak} reduces if the power demand diminishes). This operation mode is depicted at two different output powers in Figure 23 and Figure 24.

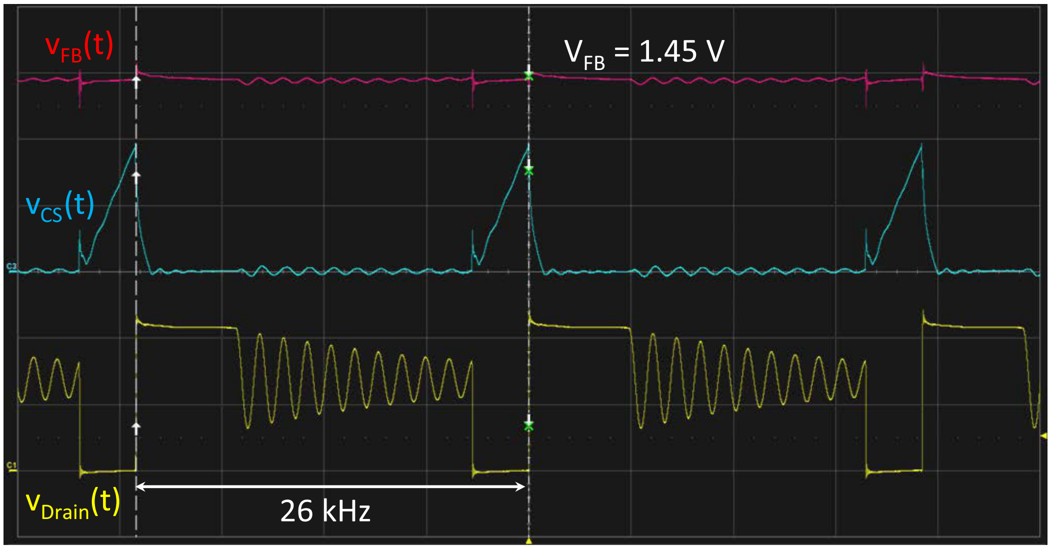

Figure 23. Frequency Clamp Mode @ 11.6 W/140 V dc

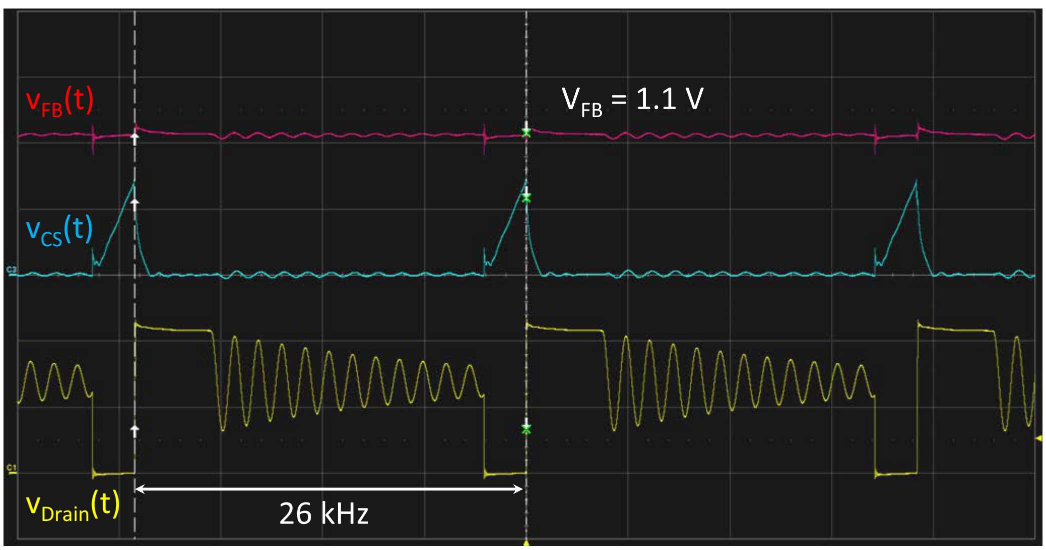

Figure 24. Frequency Clamp Mode @ 6 W/140 V dc

Skip Mode

If the load continues to decrease and FB voltage drops below 1 V, the primary peak current will be frozen to 31.25% of its maximum value. Since the NCP1239 forces a minimum peak current and a minimum frequency (26 kHz typically), the power delivery cannot be continuously controlled down to zero. Instead, the circuit stops pulsing when the FB voltage drops below 800 mV and recovers operation when V_{FB} exceeds 830 mV (30 mV hysteresis). Figure 25 shows controller operation this skip mode.

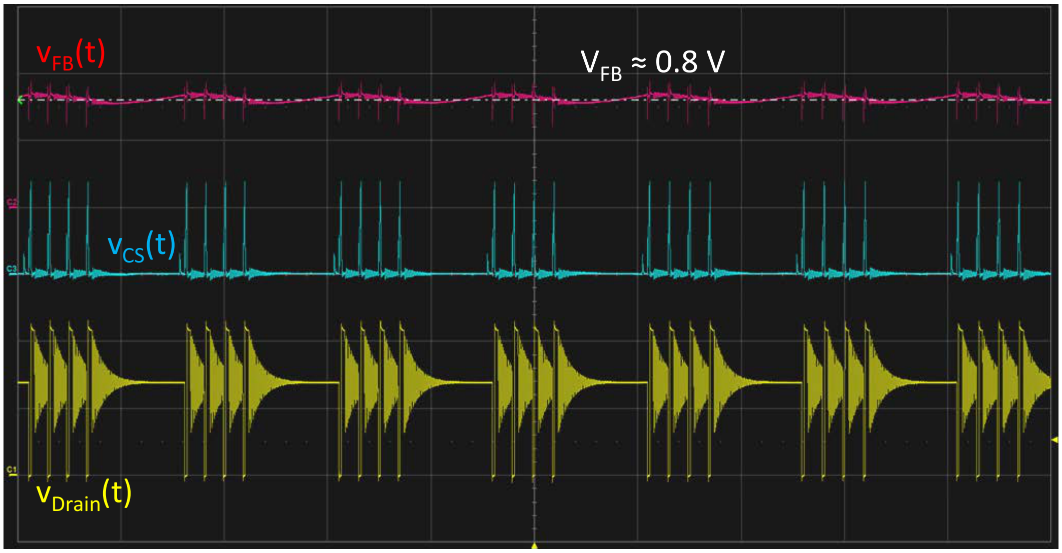

Figure 25. Skip Cycle Mode in Light Load (3 W @ 140 V dc)

Transient Load

Figure 26 and Figure 27 show an output transient load step from 10% to 100% of the maximum output power at low line and high line. The slew rate is 1 A/μs and the frequency is 20 Hz.

The step load response is ±220 mV or ±1.2% of the output voltage.

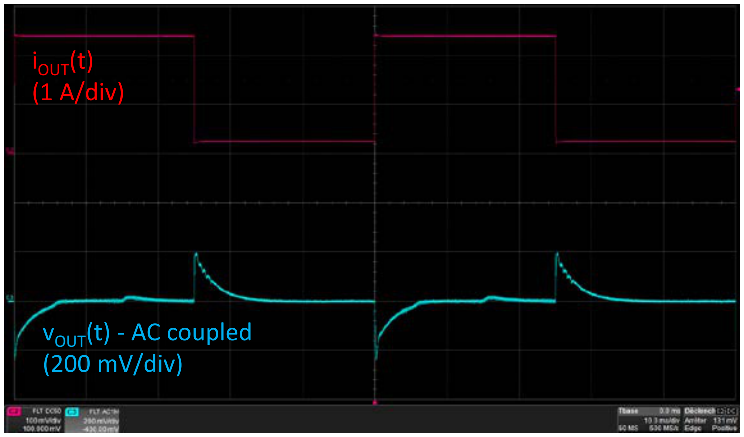

Figure 26. Step Load Response between 10% to 100% @ 115 V rms

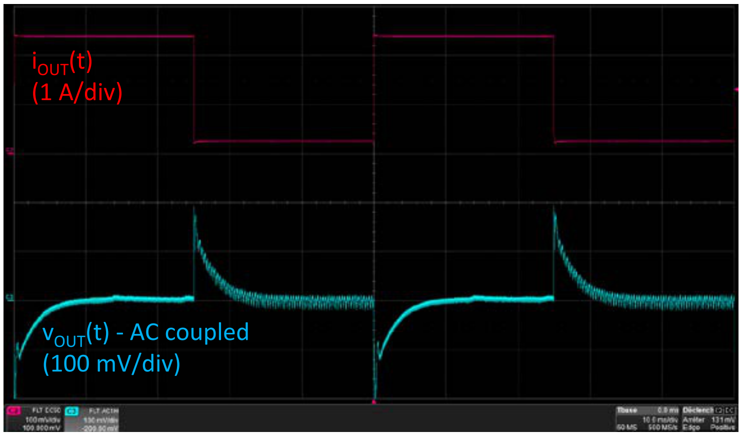

Figure 27. Step Load Response between 10% to 100% @ 230 V rms

Table 4. BILL OF MATERIAL (BOM)

Designator	Quantity	Description	Value	Tolerance	Manufacturer Part Number
C1	1	Y1 Capacitor, 250 V	2.2 nF	250 V	440LD22
C3	1	X2 Capacitor, 305 V	220 nF	305 V	B32922C3224M289
C4	1	Electrolytic Capacitor, 400 V	100 μF	400 V	400TXW100MEFC18X30
C5	1	Film Capacitor, 200 V	10 nF	200 V	Standard
C6, C7, C18	3	Ceramic Capacitor, SMD, 50 V	1 nF	10%, 50 V	Standard
C8	1	Ceramic Capacitor, SMD, 50 V	220 pF	10%, 50 V	Standard
C9	1	Ceramic Capacitor, SMD, 50 V	100 nF	10%, 50 V	Standard
C10	1	Electrolytic Capacitor, 35 V	47 μF	20%, 35 V	Standard
C11	1	Ceramic Capacitor, Axial, 1000 V	100 pF	10%, 1000 V	DEBB33A101KC1B
C12	1	Ceramic Capacitor, SMD, 50 V	220 pF	10%, 50 V	Standard
C13, C14	2	Electrolytic Capacitor, 35 V	680 μF	35 V	35ZL680M12.5X20
C15	1	Electrolytic Capacitor, 35 V	220 μF	35 V	Standard
C16	1	Ceramic Capacitor, SMD, 50 V	47 nF	10%, 50 V	Standard
D1, D2	2	Diode, Axial, 1 A, 1000 V	MRA4007	1 A, 1000 V, SMA	MRA4007T3G
D3, D4	2	Fast Recovery Diode, Axial, 1 A, 600 V	D1N4937	1 A, 600 V, DO−35	1N4937G
D5	1	18 V Zener Diode, Axial	Zener	18 V, DO−35	Standard
D6	1	Diode, SMD, 100 V	D1N4148	100 V	MMSD4148
D7	1	Schottky Diode, TO−220, 20 A, 150 V	MBR20H200	20 A, 200 V, TO−220	MBR20200CTG
D8	1	Diode, Axial, 200 mA, 250 V	BAV21	200 mA, 250 V, DO−35	Standard
D9	1	LED Rouge			Standard
HS1, HS2	2	Heatsink, 13°C/W, For M1 & D7		13°C/W	SW25−2
HSC1, HSC2	2	Heatsink Clip for TO−220, For M1 & D7			5901
IC1	1	Diode Bridge, 4 A, 800 V	KBU4K		KBU4K
IC2	1	QR Controller	NCP1239B65		NCP1239B65
IC3	1	Optocoupler SFH6156−2, SMD	SFH6156−2		SFH6156−2T
IC4	1	Shunt Regulator, 2.5−36 V, 1−100 mA	NCP431		NCP431AVSNT1G
F1	1	Fuse, 2 A, 250 V	2 A, 250 V		.0034.6618
J1	1	Input Connector, 2.5 A, 260 V		2.5 A, 260 V	JR−201S(PCB)
J2	1	Output Connector		10 A, 300 V	PM5.08/2/90
Jumper	1				
L1	1	Common Mode Choke, 2*10 mH, 1.2 A	10 mH	1.2 A	RN114−1.2/02
L2	1	Radial Coil, 1 μH, 7.5 A, 20%	1 μH	7.5 A, 20%	744772010
M1	1	MOSFET, 650 V, 8 A	IPA65R190	8 A, 650 V	IPA65R190C7
Q1	1	PNP Transistor, SMD	BC857		BC857ALT1G
R1, R2	2	Resistor, Axial, 3 W, 5%	47 kΩ	3 W, 5%	Standard
R3	1	Resistor, Axial, 1 W, 1%	22 Ω	1%	Standard
R5, R6	2	Ceramic Resistor, SMD, 0.25 W, 50 V	2.7 kΩ	5%	Standard

Table 4. BILL OF MATERIAL (BOM) (continued)

Designator	Quantity	Description	Value	Tolerance	Manufacturer Part Number
R7	1	NTC, 100 kΩ at 25°C, Beta = 4190	100 kΩ @ 25°C	0.05	NTCLE100E3104JB0
R8	1	Ceramic Resistor, SMD, 0.25 W, 200 V	1.6 kΩ	5%	Standard
R9	1	Ceramic Resistor, SMD, 0.25 W, 200 V	10 Ω	5%	Standard
R10, R24	2	Ceramic Resistor, SMD, 0.25 W, 200 V	0 Ω	5%	Standard
R11	1	Ceramic Resistor, SMD, 0.25 W, 200 V	47 kΩ	5%	Standard
R12, R13, R14	3	Ceramic Resistor, SMD, 1 W, 1%, 50 V	1 Ω	1 W, 1%	Standard
R15	1	Ceramic Resistor, SMD, 0.25 W, 200 V	33 Ω	5%	Standard
R16	1	Ceramic Resistor, SMD, 0.25 W, 200 V	1 kΩ	5%	Standard
R18	1	Ceramic Resistor, SMD, 0.25 W, 50 V	27 kΩ	5%	Standard
R19	1	Ceramic Resistor, SMD, 0.25 W, 50 V	39 kΩ	5%	Standard
R20, R25	2	Ceramic Resistor, SMD, 0.25 W, 50 V	10 kΩ	5%	Standard
R21, R22, R23	3	Ceramic Resistor, SMD, 0.25 W, 200 V	1.5 MΩ	5%	Standard
R26	1	Ceramic Resistor, SMD, 0.25 W, 50 V	33 kΩ	5%	Standard
S1, S3	2	Strap	400		Standard
S2, S4	2	Strap	700		Standard
SP1	1	Jumper400h			D3082F05
T1	1	Transformer, PQ26/25			750314896
TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	9	Test Point			5010
X1, X2, X3, X4	4	Support à riveter			SFCBS−M4−12M−01

Conclusion

This application note has described the results obtained for a 65 W Fixed Frequency flyback topology with NCP1239 controller. Thanks to the frequency foldback mode, the middle and light load consumption have been improved. The controller offers all necessary protections needed to safe power supply.

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